**Résumé Jörg Henkel**

CES – Chair for Embedded Systems

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**Working Positions**

**1991- 1996** PhD (“Summa cum Laude”) at Institute for Computer Engineering University of Braunschweig, Germany.

**1997- 2004** Senior Research Staff Member at Computer and Communication Research Laboratories CCRL (now NEC Laboratories America NECLA), NEC in Princeton, NJ, USA.

**2001** Visiting Professor, University of Notre Dame, IN, USA.

**2004 – present** Full Professor, Chair for Embedded Systems, Computer Science Department, Karlsruhe Institute of Technology, Germany.

**Five Most Relevant Publications**

* S. Rehman, M. Shafique, F. Kriebel, J. Henkel, “Reliable Software for Unreliable Hardware: Embedded Code Generation aiming at Reliability Coding”, [IEEE International Conference on Hardware-Software Codesign and System Synthesis](http://www.codes-isss.org/) [(CODES+ISSS’11)](http://www.codes-isss.org/), Taipei, Taiwan, pp. 237-246, October 2011. **Received the Codes+ISSS Best paper Award**.
* T. Ebi, M. Al Faruque, J. Henkel, “TAPE: Thermal-Aware Agent-Based Power Economy for Multi/Many-Core Architectures”, IEEE/ACM 27th International Conference on Computer-Aided Design (ICCAD’09), San Jose, CA, USA, pp. 302-309, Nov. 2009, **Received the IEEE/ACM William J. McCalla ICCAD Best Paper Award**.
* L. Bauer, M. Shafique, S. Kreutz, J. Henkel, “Run-time System for an Extensible Embedded Processor with Dynamic Instruction Set”, Proc. of IEEE/ACM Design Automation and Test in Europe Conference (DATE’08), pp. 752-757, Munich, Germany, 2008. **Received a DATE Best Paper Award**.
* M. A. Al Faruque, R. Krist, J. Henkel, “ADAM: run-time agent-based distributed application mapping for on-chip communication”, IEEE/ACM 45th Design Automation Conference (DAC’08), pp. 760-765, 2008.
* Y. Li, J. Henkel, “A Framework for Estimating and Minimizing Energy Dissipation of Embedded HW/SW Systems”, IEEE/ACM 35th Design Automation Conference (DAC’98), pp.188-193, 1998.

**Service**

* **Editor-in-Chief**
  + ACM Transaction on Embedded Computing Systems (ACM TECS)
    - Jan. 2008 – Dec. 2013 (two periods of three years)
* **Chairman:**
  + IEEE Computer Society, Germany Section (www.ieee.de/computer)
    - since 2005
* **DFG Fachkollegium:**
  + Elected Board Member of the German Research Foundation (DFG) on “Computer Architecture and Embedded Systems”
    - since 2012
* **General Chair:**
  + 2014 General Co-Chair 20th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)
  + 2013 General Chair IEEE/ACM International Conference on CAD (ICCAD)
  + 2012 General Chair IEEE ESTIMedia Symposium (part of the Embedded Systems Week)
  + 2009 General Co-Chair IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)
  + 2008 (Vice General Chair) IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)
  + 2002 IEEE/ACM 10th Symposium on Hardware/Software Co-Design, Estes Park, Colorado.
* **Program Chair:**
  + 2014 8th International Symposium on Networks-on-Chip (NOCS)
  + 2013 International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)
  + 2012 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
  + 2012 IEEE International Conference on VLSI Design
  + 2010 IEEE ESTIMedia Workshop (part of the Embedded Systems Week)
  + 2009 IEEE/ACM Int'l Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
  + 2008 IEEE Workshop on Signal Processing Systems (SiPS www.sips08.org), Washington D.C. Metropolitan Area, Oct. 2008.
  + 2006 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)
  + 2002 IEEE/ACM Rapid System Prototyping Workshop, Darmstadt, Germany.
  + 2001 IEEE/ACM 9th. Symposium on Hardware/Software Co-Design (CODES), Copenhagen, Denmark.
* **Associate Editor:**
  + IEEE Transactions on Computer-Aided Design of Integrated Circuits (TCAD). Since 2012.
  + IEEE Transaction on VLSI Systems (TVLSI). 2006-2010.
  + Journal of Low Power Electronics (JOLPE). Since 2003.
* **Guest Editorials:**
  + 2012 IEEE Transaction on Industrial Informatics on “Power-Aware Design for Embedded Systems”.
  + 2010 ACM Transaction on Design Automation for Embedded Systems (TODAES), Special Section on Low Power Electronics and Design.
  + 2008 IEEE Transaction on VLSI Systems (TVLSI), Special Issue on Low Power Electronics and Design.
  + 2003 IEEE Computer Magazine, Vol. 36, No. 4: Special Issue on Hardware/Software Co-Design, April 2003.
  + 2003 Kluwer, Journal on Design Automation for Embedded Systems, Vol. 8, Issue 4: Special Issue on Rapid System Prototyping, Dec 2003.
* **Steering/Executive Committees:**
  + Chair of the ACM/IEEE CASES Conference (Compiler, Architecture and Synthesis for Embedded Systems)
    - since 2010
  + Steering Committee Member of the ACM/IEEE Embedded Systems Week www.eswork.org
    - since 2010
  + Steering Committee Member IEEE/ACM International Conference on Computer Aided Design (ICCAD)
    - 2014, 2013, 2012, 2011, 2009, 2008
  + Editorial Board Member of the “Journal for Embedded Computing” by Cambridge International Science Publishing:
    - since 2003
  + Steering Committee Member IEEE/ACM Codes+ISSS Conference
    - since 2004
* **Other Chair Position:**
  + Workshop Chair CASA (Compiler Assisted SoC Assembly) 2008 at ESWeek
  + Chair EDAA/DATE PhD Forum 2007
  + Co-Chair EDAA/DATE PhD Forum 2006
* **Organizing Committees:**
  + 2013 Track Chair CODES+ISSS, “Track 7: Power-aware Systems”
  + 2012, 2011 “Sub-Committee Chair on Embedded Systems Platforms and Case Studies”, IEEE/ACM Design Automation Conference (DAC).
  + 2012 Publicity Chair 7th IEEE International Symposium on Industrial Embedded Systems
  + 2010, 2009 “Sub-Committee Chair on Low Power”. IEEE/ACM International Conf. on Computer Aided Design (ICCAD)
  + 2011, 2010, 2009 “Sub-Committee Chair on Power Estimation and Optimization”, IEEE/ACM Design Automation and Test in Europe Conference (DATE).
  + 2008 “Sub-Committee Chair on System-level Communication” IEEE/ACM Design Automation Conference (DAC).
  + 2008 “Topic Chair on Low Power Design”, Codes+ISSS 2008.
  + 2010, 2009, 2008, 2007, “Publicity Co-Chair” IEEE/ACM ESWeek.
  + 2004 "Topic Chair on System Synthesis" at IEEE/ACM ICCAD Conference.
  + 2004 "Special Session Chair" at IEEE/ACM Codes-ISSS Conference.
  + 2003 "Topic Chair on System Synthesis" at IEEE/ACM ICCAD Conference.
  + 2002 "Tutorial Chair" at IEEE/ACM CASES Conference.
* **Program Committees:**
  + DAC (IEEE/ACM Design Automation Conference)
    - 2012, 2011, 2008, 2007, 2006
  + ICCAD (IEEE/ACM Int’l. Conf on Computer Aided Design)
    - 2010, 2009, 2008, 2004, 2003, 2002
  + DATE (IEEE/ACM Design Automation & Test in Europe Conf.)
    - 2014, 2013, 2012, 2011, 2010, 2009, 2008, 2007, 2006, 2005, 2004, 2003, 2002, 2001
  + ISLPED (IEEE/ACM Int’l Symposium on Low Power Electronics and Design)
    - 2012, 2011, 2010, 2009, 2008, 2007, 2005, 2004, 2003, 2002, 2001, 2000
  + ICCD (IEEE Int’l Conf. on Computer Design)
    - 2009, 2008
  + ASPDAC (IEEE/ACM Asia & South Pacific Design Automation Conf.):
    - 2009, 2004
  + Codes and Codes+ISSS (IEEE/ACM Hardware/Software Co-design Symposium):
    - 2014, 2013, 2012, 2011, 2010, 2009, 2008, 2007, 2005, 2004, 2003, 2002, 2001, 2000, 1999
  + NoCS (IEEE International Symposium on Networks-on-Chip)
    - 2014, 2013, 2012, 2011, 2010, 2009
  + CASES (IEEE/ACM Conf. on Compilers, Architectures and Synthesis for Embedded Systems):
    - 2013, 2012, 2011, 2010, 2009, 2002
  + RTSS (IEEE/ACM Real Time System Symposium):
    - 2007, 2004, 2003
  + ASAP (IEEE International Conference on Application-specific Systems, Architectures and Processors)
    - 2014
  + ECRTS (IEEE European Micro Conference on Real-Time Systems)
    - 2007
  + ISVLSI (IEEE/ACM International Symposium on VLSI)
    - 2011, 2010, 2009, 2008, 2007, 2006
  + RSP (IEEE/ACM Rapid System Prototyping Workshop):
    - 2010, 2009, 2008, 2007, 2006, 2005, 2004, 2003, 2002
  + ESTIMedia Workshop:
    - 2010, 2009, 2008, 2007, 2005, 2004, 2003
  + Scopes Workshop
    - 2014, 2013, 2011, 2010, 2009, 2008, 2007
  + Samos Conference
    - 2009, 2008, 2007
* **Other Committees**
  + Best Paper Award Committee IEEE/ACM DAC, 2014
  + Best Paper Award Committee IEEE/ACM ICCAD Conference 2007
  + EDAA/DATE Best PhD Award Committee 2014, 2007, 2006
* **Other Memberships**
  + Member HiPEAC European Network of Excellence on High Performance and Embedded Architecture and Compilation.

**Awards**

* Embedded Systems Week, IEEE International Conference on Hardware-Software Co-design and System Synthesis (CODES+ISSS'11) **Best Paper Award** for “Reliable Software for Unreliable Hardware: Embedded Code Generation aiming at Reliability”, 2011.
* MaXentric Technologies **AHS** **Best Paper Award** for “Concepts, Architectures, and Run-time Systems for Efficient and Adaptive Reconfigurable Processors”, 2011.
* William J. McCalla **Best Paper Award ICCAD 2009** (IEEE/ACM Int'l Conference on Computer Aided Design) for ”TAPE: Thermal-Aware Agent-Based Power Economy for Multi/Many-Core Architectures“
* **Best Paper Award DATE 2008** Conference for **”Run-time System for an Extensible Embedded Processor with Dynamic Instruction Set**“ (announced in April 2009).
* Best Paper Nomination at ICCAD 2010 for "Selective Instruction Set Muting for Energy-Aware Adaptive Processors"
* Best Paper Nomination at ICCAD 2010 for "SETS: Stochastic Execution Time Scheduling for Multicore Systems by Joint State Space and Monte Carlo".
* Six HiPEAC (European Network of Excellence on High Performance and Embedded Architecture and Compilation) Paper Awards between 2008-2011.
* “Summa cum Laude” for PhD Thesis, 1996.

**Student Awards** (received by Master and PhD students under my supervision):

* European Design and Automation Association (EDAA) Outstanding Dissertations Award for the Ph.D. Thesis by Dr. Lars Bauer entitled “RISPP: A Run-time Adaptive Reconfigurable Embedded Processor”, 2011.
* Hermann Billing Price for the Master Thesis of Florian Kriebel entitled “Analysis and Design of Hybrid Hardware/Software Reliability Techniques for Embedded Processors”, 2011.
* FZI (Research Center Computer Science) Best Dissertation Award for the Ph.D. Thesis by Dr. Lars Bauer entitled “RISPP: A Run-time Adaptive Reconfigurable Embedded Processor”, 2011.
* FZI (Research Center Computer Science) 2008 **Best Master Thesis Award** for the Master Thesis by Bastian Molkenthin entitled “Development of a Power-Aware Rate Controller for H.264 Video Encoder”.

**Delivered Keynotes**

* “Embedded On-Chip Reliability – It’s a Thermal Challenge”, M-Scopes, Schloss Rheinfels, June 20th, 2013.
* “Embedded On-Chip Reliability - It's a Thermal Challenge” at “Chip in Brasilia” (SBCCI / SBMicro), Brasilia, Brazil, September 1st., 2012
* “Dependable Software for Undependable Hardware” at 7th IEEE International Symposium on Industrial Embedded Systems (SIES'12), Karlsruhe, Germany, June 20th, 2012.
* “i-Core: A run-time adaptive processor for embedded multi-core systems”, by Jörg Henkel at International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'11), Las Vegas, Nevada, July 20th. 2011.
* “Reliability of On-Chip Systems – A Thermal Perspective”, by Jörg Henkel at ISVLSI 2011 Conference, Chennai, India, July 4th. 2011.
* “Embedded Systems and the Reliability Challenge”, by Jörg Henkel at the 2008 World Computing Congress (WCC’08) at DIPES’08, Milano, Sept. 8th. 2008.

**Patents**

* H. Lekatsas, J. Henkel, S. Chakradhar, V. Jakkula, "Dynamic content-aware memory compression and encryption architecture", issued January 6th., 2009, US Patent No. 7,474,750
* H. Lekatsas, J. Henkel, S. Chakradhar, V. Jakkula, "Compressed memory architecture for embedded systems", issued November 27th., 2007, US Patent No. 7,302,543
* S. Chakradhar, J. Henkel, V. Jakkula, H. Lekatsas, S. Murugan: "Hardware/software platform for rapid prototyping of code compression technologies", issued April 10th, 2007; US Patent No.7,203,935
* J. Henkel, H. Lekatsas, V. Jakkula: ”Apparatus for one-cycle decompression of compressed data and methods of operation thereof”, issued May 10th, 2005; US Patent No. 6,892,292
* J. Henkel, F. Vahid, T. Givargis, "Method for core-based system-level power modeling using object-oriented techniques", issued March 8th, 2005, US Patent No. 6,865,526
* J. Henkel, H. Lekatsas: "Method and apparatus for adaptive bus coding for low power deep submicron designs", issued May 25th., 2004, US Patent No. 6,741,190
* J. Henkel, W. Wolf, H. Lekatsas, "Method and apparatus for object code compression and decompression for computer systems", issued May 4th., 2004, US Patent No. 6,732,256
* J. Henkel, W. Wolf, H. Lekatsas, "Object code compression using different schemes for different instruction types", issued Feb. 10th., 2004, US Patent No. 6,691,305
* J. Henkel, “Low power hardware/software partitioning approach for core-based embedded systems", issued Sept. 16, 2003, US Patent No. 6, 622, 287
* J. Henkel, H. Lekatsas, "Method and apparatus for adaptive bus coding for low power deep submicron designs", issued June 24, 2003, US Patent No. 6, 583, 735.

**Panel Invitations**

* "Reset Microprocessor Hardware and Software Roadmaps for the next 30 Years?", Panel at IEEE International Conference for Computer Design (ICCD'08), Moderator: Georgi Gaydadjiev, TU Delft. Panelists: Jörg Henkel, University of Karlsruhe, Edward Grochowski, Intel Corp., Tom Conte, Georgia Institute of Technology, Brian Flachs, IBM, Lake Tahoe, CA, Oct. 14th. 2008.
* "GP vs. ASP:  Are ASIPS just a short-term transition in computing?", Panel at IEEE Symposium on Application Specific Processor (SASP’08) , Moderator: Grant Martin, Tensilica. Panelists: Eric Collins, Novelics; Tim Kogel, CoWare; Nigel Topham, University of Edinburgh and ARC; Nader Bagherzadeh, University of Irvine; Jörg Henkel, University of Karlsruhe. Anaheim June 9th. 2008.
* “Best Ways to Use Billions of Devices on a Chip”, Panel at IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC’08), Moderator: Grant Martin, Tensilica, Panelists: Deming Chen, Nikil Dutt, Jörg Henkel, Kyungho Kim, Kazutoshi Kobayashi, Seoul, Jan. 24th. 2008.

**Tutorials held (honorarium provided)**

* 2013 “Temperature- and Process Variation-Aware Dependable Embedded Systems” at ASP-DAC, Yokohama, Japan, January 22nd, 2013.
* 2009 “Security and Dependability of Embedded Systems: Computer Architects’ Perspective”, at IEEE VLSI Design Conf., Jan. 8th. 2009 in Delhi.
* 2003 Full-day tutorial on “Specification & Design of Multi-million gate SOCs”,   
  held at IEEE VLSI Conference, New Delhi, Jan 5th. 2003.
* 2002 Full-day tutorial on “Specification & Design of Multi-million gate SOCs”,   
  held at IEEE/ACM Int’l Conf. on CAD (ICCAD), San Jose, California, Nov. 2002.
* 2002 Full-day tutorial on “New Computing Platforms for Embedded Systems”,   
  held at IEEE/ACM Design Automation Conference (DAC), New Orleans, June 2002.
* 2001 Half-day tutorial on “Platform-based Design for Systems-on-Chips”,   
  held at IEEE/ACM DATE Conference, Munich, March 2001.
* 1998 Half-day tutorial on “Core based design of systems on a chip”,   
  held at IEEE 11th. Int’l ASIC Conf., Ann Arbor, Michigan, Sept. 1998.
* 1995 Full-day tutorial on “Hardware/Software Co-Design of Embedded Systems”,   
  held at IEEE/ACM Int’l Conf. on CAD (ICCAD), San Jose, California, Nov. 1995.

**Embedded Tutorials held**

* 2004 on “Quo Vadis Multimedia? From Desktop Multimedia to Distributed Multimedia Systems”, held at IEEE/ACM DATE Conference, Paris, Feb. 19th. 2004.
* 2004 on “On-chip networks: a scalable, communication-centric embedded system design paradigm”, held at 17th. IEEE VLSI Conference, Mumbai, India, Jan. 9th. 2004.

**Publications**

**Book / Book Contributions**

* Zatt, B., Shafique, M., Bampi, S., Henkel, J.: “**3D Video Coding for Embedded Devices - Energy Efficient Algorithms and Architectures“,** Springer 2013, Science+Business Media, LLC,   
  ISBN 978-1-4614-6758-8 (Book).
* Shafique, M., Henkel, J.: “Hardware/Software Architectures for Low-Power Embedded Multimedia Systems[”, Springer 2011](http://www.springer.com/engineering/circuits+&+systems/book/978-1-4419-9691-6), ISBN 978-1-4419-9691-6 (Book).
* Bauer, L., Henkel, J., “Run-time Adaptation for Reconfigurable Embedded Processors”, [Springer](http://www.springer.com/engineering/circuits+%26+systems/book/978-1-4419-7411-2) 2007, ISBN 978-1-4419-7411-2 (Book).
* Henkel, J., Parameswaran, S. (Eds.), “Designing Embedded Processors - A low power perspective“, Springer 2007, ISBN 978-1-4020-5868-4 (Book).
* Henkel, J., Parameswaran, S., Cheung, N., „Application-Specific Embedded Processors“ in "Designing Embedded Processors", J. Henkel and S. Parameswaran (Eds.), Springer, pp. 3-23, 2007.
* Parameswaran, S., Henkel, J., Janapsatya, A., Bonny, T.,Ignjatovic, A., „Design and Run Time Code Compression for Embedded Systems“ in "Designing Embedded Processors", J. Henkel and S. Parameswaran (Eds.), Springer, pp. 97-128, 2007.
* Cheung, N., Henkel, J., Parameswaran, S., „Instruction Matching and Modelling“ in: "Customizable and Configurable Embedded Processors", Publisher: Lenne, P.; Leupers, R.; Elsevier: Morgan Kaufmann, pp. 257-277, 2006.
* P. Ashar, S. Chakradhar, A. Gupta, J. Henkel, A. Raghunathan, K. Wakabayashi, “NEC and ICCAD-EDA Partners in Success”, Proc. of "The Best of ICCAD: 20 Years of Excellence in Computer-Aided Design", A. Kuehlmann (ed.), Kluwer, pp.663-674, Feb. 2003.
* “Readings in Hardware/Software Co-Design” , Ed.: G. De Micheli, R. Ernst, W. Wolf, MORGAN KAUFMAN Publishers, Our contribution: Y. Li, J. Henkel, “A Framework for Estimating and Minimizing Energy Dissipation of Embedded HW/SW Systems”, to appear Spring 2001.
* J. Henkel, "Automated hardware/software partitioning in the design of integrated real-time systems", (published Ph.D. dissertation in German language), Shaker Publishing House, ISBN: 3-8265-2038-6, 1996.

**Journals/Magazins**

* H. Javaid, M. Shafique, J. Henkel, S. Parameswaran, „**Energy-Efficient Adaptive Pipelined MPSoCs for Multimedia Applications“,** IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), (to appear).
* H. Amrouch, T. Ebi, J. Henkel, „**RESI: Register-Embedded Self-Immunity for Reliability Enhancement“,** IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), (to appear).
* M. Shafique, L. Bauer, J. Henkel, „**Adaptive Energy Management for Dynamically Reconfigurable Processors“,** IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 33, Issue 1, pp. 50-63, Januar 2014.
* A. Herkersdorf, H. Aliee, M. Engel, M. Glaß, C. Gimmler-Dumont, J. Henkel, V. B. Kleeberger, M. A. Kochte, J. M. Kühn, D. Mueller-Gritschneder, S. R. Nassif, H. Rauchfuss, W. Rosenstielf, U. Schlichtmann, M. Shafique, M. B. Tahoori, J. Teich, N. Wehn, C. Weis, H.-J. Wunderlich, „**Resilience Articulation Point (RAP): Cross-layer Dependability Modeling for Nanometer System-on-chip Resilience“,** Elsevier Microelectronics Reliability Journal (to appear).
* B.B. Vizzotto, B. Zatt, M. Shafique, S. Bampi, J. Henkel, „**Model Predictive Hierarchical Rate Control with Markov Decision Process for Multiview Video Coding“,** IEEE Transactions on Circuits and Systems for Video Technology (TCSVT), vol. 23, no. 12, pp. 2090-2104, December 2013.
* L. Bauer, C. Braun, M.E. Imhof, M.A. Kochte, E. Schneider, H. Zhang, J. Henkel, H.-J. Wunderlich, „**Test Strategies for Reliable Runtime Reconfigurable Architectures“,** IEEE Transactions on Computers, vol. 62, no. 8, pp. 1494-1507, August 2013.
* M.A. Al Faruque, T. Ebi, J. Henkel, “AdNoC: Runtime Adaptive Network-on-Chip Architecture”, IEEE Transaction on Very Large Scale Integration Systems, Vol. 20 (2): pp. 257-269, 2012.
* J. Teich, J. Henkel, A. Herkersdorf, D. Schmitt-Landsiedel, W. Schröder-Preikschat, G. Snelting, ”Invasive Computing: An Overview ", Multiprocessor System-on-Chip -- Hardware Design and Tool Integration, M. Hübner and J. Becker (Eds.), pp. 241-268, Springer, 2011.
* N. Chang, J. Henkel, " Current Trends in Low Power Design ( Guest Editorial )", ACM Transactions on Design Automation of Electronic Systems (ACM TODAES), Vol. 16, No. 1, pp. 1-8, November 2010 .
* M.A. Al Faruque, J. Jahn, T. Ebi, J. Henkel, "Runtime Thermal Management Using Software Agents for Multi/Many-Core Architectures", EEE Design & Test (IEEE D&T), Special Issue on Post-Silicon Calibration and Repair for Yield and Reliability Improvement, Vol. 27, No. 6, pp. 58-68, Nov/Dec 2010.
* T. Bonny, J. Henkel, "Huffman-based code compression technique for embedded processors", ACM Trans. Design Autom. Electr. Syst. (TOADES), Vol. 15, No. 4, 2010.
* J. Henkel, S. Parameswaran, " CASES 2009 Guest Editorial", Design Automation for Embedded Systems (Springer), Vol. 14, No. 3, pp. 285-286, 2010.
* M. Shafique, L. Bauer, J. Henkel, "Optimizing the H.264/AVC Video Encoder Application Structure for Reconfigurable and Application-Specific Platforms", Journal of Signal Processing Systems (JSPS), Special Issue on Estimedia, Volume 60, Issue 2, pp. 183-210, August 2010.
* G. Frantz, J. Henkel, J. Rabaey, T. Schneider, M. Wolf, U. Batur, "Ultra-Low Power Signal Processing", IEEE Signal Processing Magazine, Volume 27, Issue 2, pp. 149-154, March 2010.
* L. Bauer, M. Shafique, J. Henkel, "Efficient Resource Utilization for an Extensible Processor through Dynamic Instruction Set Adaptation", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Special Section on Application-Specific Processors, Volume 16, Issue 10, pp. 1295-1308, Oct. 2008.
* T. Bonny, J. Henkel, "Efficient Code Compression for Embedded Processors", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume 16, Issue 12, pp. 1696-1707, December 2008.
* P. Kalla, X. S. Hu, J. Henkel, "A Flexible Framework for Communication Evaluation in SoC Design", International Journal of Parallel Programming, Volume 36, Number 5, pp. 457-477, October 2008.
* D. Serpanos, J. Henkel, "Dependability and Security Will Change Embedded Computing", IEEE Computer Magazine, pp. 82-84, Jan. 2008.
* Al Faruque, M.A., Henkel, J., „QoS-Supported On-chip Communication for Multi-Processors“, International Journal of Parallel Programming (IJPP '08), Volume 36, Number 1, pp. 114-139, February 2008.
* Kalla, P., Hu, X.S., Henkel, J., „Distance-based recent use (DRU): an enhancement to instruction cache replacement policies for transition energy reduction“, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume: 14, Issue: 1, pp. 69-80, 2006.
* Lekatsas, H., Henkel, J., Wolf, W., „Approximate arithmetic coding for bus transition reduction in low power designs“, IEEE Transactions on VLSI Systems, Volume: 13, Issue: 6, pp. 696–707, June 2005
* Bhattacharyya, S.S., Henkel, J., Hu, Xiaobo S., „Hardware/software codesign for DSP“, IEEE Signal Processing Magazine, Volume: 22, Issue: 3, pp. 11-12, May 2005.
* Parameswaran, S., Henkel, J., „Instruction Code Mapping for Performance Increase and Energy Reduction in Embedded Computer Systems“, IEEE Transactions on VLSI Systems, Volume: 13, Issue: 4, pp. 498-502, April 2005.
* Lv, T., Jiang Xu, Wolf, W., Ozer, I.B., Henkel, J., Chakradhar, S.T., „A Methodology for Architectural Design of Multimedia Multiprocessor SoCs“, IEEE Design & Test of Computers, Volume: 22, Issue: 1, pp. 18-26, Jan. 2005.
* Lekatsas, H., Henkel, J., Chakradhar, S., Jakkula, V., „Cypress: Compression and Encryption of Data and Code for Embedded Multimedia Systems“, IEEE Proceedings of the Design & Test of Computers, Volume: 21, Issue: 5, pp. 406 - 415, May 2004.
* F. Kordon, J. Henkel, “An Overview of Rapid System Prototyping Today”, Kluwer Journal on Design Automation for Embedded Systems (DAES), Volume 8, Issue 4, pp. 275-282, Dec. 2003.
* T. Lv, J. Henkel, H. Lekatsas, W. Wolf, “A dictionary-based en/decoding scheme for low-power data buses”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 11, Issue 5, pp. 943-951, Oct. 2003.
* J. Henkel, “Closing the SoC design gap”, IEEE Computer Magazine, Volume 36 , Issue 9, pp. 119-121, Sept. 2003.
* J. Henkel, X.S. Hu, S. Bhattacharyya, “Taking on the embedded system design challenge”, IEEE Computer Magazine ,Volume 36, Issue 4, pp. 35-37, April 2003.
* T. Givargis, F. Vahid, J. Henkel, “Instruction-based system-level power evaluation of system-on-a-chip peripheral cores”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 10, Issue 6, pp.856-863, Dec. 2002.
* J. Henkel, Y. Li, "Avalanche: An Environment for Design Space Exploration and Optimization of Low Power Embedded Systems”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 4, pp. 454-468, August 2002.
* T. Givargis, F. Vahid, J. Henkel, “System-Level Exploration for Pareto-Optimal Configurations in Parameterized System-on-a-Chip”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 4, pp. 216-222, August 2002.
* J. Henkel, R. Ernst, “An Approach to Automated Hardware/Software Partitioning using a flexible Granularity that is driven by High-Level Estimation Techniques”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 9, No. 2, pp. 271-289, April 2001.
* T. Givargis, F. Vahid, J. Henkel, “Evaluating Power Consumption of Parameterized Cache and Bus Architectures in System-on-a-Chip Designs”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 9, No. 4, pp. 500-508, Aug. 2001.
* J. Henkel, “Automatisierte Hardware/Software-Partitionierung im Entwurf integrierter Echtzeitsysteme”, PhD Dissertation at Technical University of Braunschweig, Braunschweig, Shaker Publishing House, 1996.
* R. Ernst, J. Henkel, Th. Benner, W. Ye, U. Holtmann, D. Herrmann, M. Trawny, “The COSYMA Environment for Hardware/Software Cosynthesis”, Elsevier, Microprocessors and Mircosystems, Vol. 20, No. 3, pp. 159-166, 1996.
* J. Henkel, R. Ernst, W. Ye, M. Trawny, Th. Benner, COSYMA: Ein System zur Hardware/Software Co-Synthese, GME Fachbericht Nr. 15 Mikroelektronik, pp. 167-172, 1995.
* J. Henkel, Th. Benner, R. Ernst, W. Ye, N. Serafimov and G. Glawe, “COSYMA: A Software-Oriented Approach to Hardware/Software Codesign”, The Journal of Computer and Software Engineering, Vol. 2, No. 3, pp. 293-314, 1994.
* W. Ye, R. Ernst, Th. Benner, J. Henkel, “Fast Timing Analysis for Hardware-Software Co-Synthesis”, IEEE/ACM Proc. of ICCD 1993, pp. 452-457, 1993.
* R. Ernst, J. Henkel and Th. Benner, “Hardware/Software Co-Synthesis for Microcontrollers”, IEEE Design & Test Magazine, Vol 10, No. 4, pp. 64-75, 1993.
* J. Henkel, R. Ernst, “Ein softwareorientierter Ansatz zum Hardware/Software Co-Entwurf”, ITG-Fachbericht 122, VDE-Verlag, 1992.

**Conferences/Symposia/Workshops**

* M.S. Srouji, T. Bonny, J. Henkel, „**High-speed Encoding/Decoding Technique for Reliable Data Transmission in Wireless Sensor Networks“,** IEEE 11th International Conference on Sensing, Communication, and Networking (SECON '14), Singapore, 30 June - 3 July, 2014, (accepted).
* M. Shafique, S. Garg, D. Marculescu, J. Henkel, „**The EDA Challenges in the Dark Silicon Era“,** IEEE/ACM Design Automation Conference (DAC'14), San Francisco, CA, USA, June 2014, (accepted).
* F. Hameed, L. Bauer, J. Henkel, „**Reducing Latency in an SRAM/DRAM Cache Hierarchy via a Novel Tag-Cache Architecture“,** IEEE/ACM Design Automation Conference (DAC'14), San Francisco, CA, USA, June 2014, (accepted).
* H. Zhang, M. Kochte, M. Imhof, L. Bauer, H.-J. Wunderlich, J. Henkel, „**GUARD: GUAranteed Reliability in Dynamically Reconfigurable Systems“,** IEEE/ACM Design Automation Conference (DAC'14), San Francisco, CA, USA, June 2014, (accepted).
* S. Rehman, F. Kriebel, D. Sun, M. Shafique, J. Henkel, „**dTune: Leveraging Reliable Code Generation for Adaptive Dependability Tuning under Process Variation and Aging-Induced Effects“,** IEEE/ACM Design Automation Conference (DAC'14), San Francisco, CA, USA, June 2014, (accepted).
* F. Kriebel, S. Rehman, D.Sun, M. Shafique, J. Henkel, „**ASER: Adaptive Soft Error Resilience for Reliability-Heterogeneous Processors in the Dark Silicon Era“,** IEEE/ACM Design Automation Conference (DAC'14), San Francisco, CA, USA, June 2014, (accepted).
* H. Bokhari, H. Javaid, M. Shafique, J. Henkel, S. Parameswaran, „**darkNoC: Designing Energy Efficient Network-on-Chip with Multi-Vt Cells for Dark Silicon“,** IEEE/ACM Design Automation Conference (DAC'14), San Francisco, CA, USA, June 2014, (accepted).
* J. Heisswolf, A. Zaib, A. Zwinkau, S. Kobbe, A. Weichslgartner, J. Teich, J. Henkel, G. Snelting, A. Herkersdorf, J. Becker, “**CAP: Communication Aware Programming“,** IEEE/ACM Design Automation Conference (DAC'14), San Francisco, CA, USA, June 2014, (accepted).
* J. Henkel, L. Bauer, H. Zhang, S. Rehman, M. Shafique, „**Multi-Layer Dependability: From Microarchitecture to Application Level**“ (Invited Paper for the Special Session: "Embedded Resiliency: Approaches for the Next Decade"), IEEE/ACM Design Automation Conference (DAC'14), San Francisco, CA, USA, June 2014, (accepted).
* H. Khdr, T. Ebi, M. Shafique, H. Amrouch, J. Henkel, „**mDTM: Multi-Objective Dynamic Thermal Management for On-Chip Systems“,** IEEE/ACM 17th Design Automation and Test in Europe Conference (DATE´14), Dresden, Germany, March 2014, (accepted).
* M.U.K. Khan, M. Shafique, J. Henkel, „**Software Architecture of High Efficiency Video Coding for Many-Core Systems with Power-Efficient Workload Balancing“,** IEEE/ACM 17th Design Automation and Test in Europe Conference (DATE´14), Dresden, Germany, March 2014, (accepted).
* S. Rehman, F. Kriebel, M. Shafique, J. Henkel, „**Compiler-Driven Dynamic Reliability Management for On-Chip Systems under Variabilities“,** IEEE/ACM 17th Design Automation and Test in Europe Conference (DATE´14), Dresden, Germany, March 2014, (accepted IP).
* D. Palomino, M. Shafique, H. Amrouch, A. Susin, J. Henkel, „**hevcDTM: Application-Driven Dynamic Thermal Management for High Efficiency Video Coding“,** IEEE/ACM 17th Design Automation and Test in Europe Conference (DATE´14), Dresden, Germany, March 2014, (accepted IP).
* F. Sampaio, M. Shafique, B. Zatt, S. Bampi, J. Henkel, „**dSVM: Energy-Efficient Distributed Scratchpad Video Memory Architecture for the Next-Generation High Efficiency Video Coding”,** IEEE/ACM 17th Design Automation and Test in Europe Conference (DATE´14), Dresden, Germany, March 2014, (accepted).
* A. Grudnitsky, L. Bauer, J. Henkel, „**MORP: Makespan Optimization for Processors with an Embedded Reconfigurable Fabric“,** 22nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), Monterey, California, USA, February 2014, pp. 127-136.
* M. Shafique, J. Henkel, „**Low Power Design of the Next-Generation High Efficiency Video Coding**“  
  (Invited Special Session Paper, Special Session: “Design Automation Methods for Highly-Complex Multimedia Systems”), 19th Asia and South Pacific Design Automation Conference (ASP-DAC´14), Singapore, January 2014, (accepted).
* D. Palomino, E. Cavichioli, L. Agostini, M. Shafique, J. Henkel, A. Susin, “**Fast HEVC Intra Mode Decision Algorithm Based on New Evaluation Order in the Coding Tree Block“,** 30th Picture Coding Symposium (PCS´13), San Jose, CA, USA, December 2013, (accepted).
* M. Shafique, J. Henkel, „**Agent-Based Distributed Power Management for Kilo-Core Processors**“  
  (Invited Special Session Paper, Special Session: “Keeping Kilo-core Chips Cool: New Directions and Emerging Solutions”), IEEE/ACM International Conference on  Computer-Aided Design (ICCAD'13), San Jose, CA, USA, November 2013, pp. 153-160.
* J. Jahn, S. Pagani, J.-J. Chen, J. Henkel, „**MOMA: Mapping of Memory-intensive Software-pipelined Applications for Systems with Multiple Memory Controllers“,** IEEE/ACM International Conference on  Computer-Aided Design (ICCAD'13), San Jose, CA, USA, November 2013, pp. 508-515.
* M.U.K. Khan, M. Shafique, J. Henkel, „**AMBER: Adaptive Energy Management for On-Chip Hybrid Video Memories“,** IEEE/ACM International Conference on Computer-Aided Design (ICCAD'13), San Jose, CA, USA, November 2013, pp. 405-412.
* R.M. Bilal, R. Hafiz, M. Shafique, S. Shoaib, A. Munawar, J. Henkel, “**ISOMER: Integrated Selection, Partitioning and Placement Methodology for Reconfigurable Architectures“,** IEEE/ACM International Conference on  Computer-Aided Design (ICCAD'13), San Jose, CA, USA, November 2013, pp. 755-762.
* T. Li, M. Shafique, S. Rehman, J.A. Ambrose, J. Henkel, S. Parameswaran, „**DHASER: Dynamic Heterogeneous Adaptation for Soft-Error Resiliency in ASIP-based Multi-core Systems“,** IEEE/ACM International Conference on  Computer-Aided Design (ICCAD'13), San Jose, CA, USA, November 2013, pp. 646-653.
* M. Ismail, O. Hasan, T. Ebi, M. Shafique, J. Henkel, „**Formal Verification of Distributed Dynamic Thermal Management“,** IEEE/ACM International Conference on  Computer-Aided Design (ICCAD'13), San Jose, CA, USA, November 2013, pp. 248-255.
* F. Hameed, L. Bauer, J. Henkel, „**Reducing Inter-Core Cache Contention with an Adaptive Bank Mapping Policy in DRAM Cache“,** IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'13), Montreal, Canada, September - October 2013.
* F. Hameed, L. Bauer, J. Henkel, „**Simultaneously Optimizing DRAM Cache Hit Latency and Miss Rate via Novel Set Mapping Policies“,** International Conference on Compilers Architecture and Synthesis for Embedded Systems (CASES'13), Montreal, Canada, September - October 2013.
* M. Mohr, A. Grudnitsky, T. Modschiedler, L. Bauer, S. Hack, J. Henkel, „**Hardware Acceleration for Programs in SSA Form“,** International Conference on Compilers Architecture and Synthesis for Embedded Systems (CASES'13), Montreal, Canada, September - October 2013.
* C.M. Diniz, M. Shafique, S. Bampi, J. Henkel, „**High-Throughput Interpolation Hardware Architecture with Coarse-Grained Reconfigurable Datapaths for HEVC“,** 20th IEEE International Conference on Image Processing (ICIP), Melbourne, Australia, September 2013, pp. 2091-2095.
* M.U.K. Khan, M. Shafique, J. Henkel, „**An Adaptive Complexity Reduction Scheme with Fast Prediction Unit Decision for HEVC Intra Encoding“,** 20th IEEE International Conference on Image Processing (ICIP), Melbourne, Australia, September 2013, pp. 1578-1582.
* M. Grellert, M. Shafique, M.U.K. Khan, L. Agostini, J.C.B. Mattos, J. Henkel, „**An Adaptive Workload Management Scheme for HEVC“,** 20th IEEE International Conference on Image Processing (ICIP), Melbourne, Australia, September 2013, pp. 1850-1854.
* F. Sampaio, B. Zatt, M. Shafique, L. Agostini, J. Henkel, S. Bampi, „**Content-Adaptive Reference Frame Compression Based On Intra-Frame Prediction for Multiview Video Coding“,** 20th IEEE International Conference on Image Processing (ICIP), Melbourne, Australia, September 2013, pp. 1831-1835.
* H. Zhang, L. Bauer, M.A. Kochte, E. Schneider, C. Braun, M.E. Imhof, H.-J. Wunderlich, J. Henkel. „**Module Diversification: Fault Tolerance and Aging Mitigation for Runtime Reconfigurable Architectures“,** 2013 IEEE International Test Conference (ITC), Anaheim, California, USA, September 2013, pp. 1-10.
* M. Shafique, M.U.K. Khan, J. Henkel, „**Content-Driven Adaptive Computation Offloading for Energy-Aware Hybrid Distributed Video Coding“,** International Symposium on Low Power Electronics and Design (ISLPED'13), Beijing, China, September 2013, pp. 106-113.
* H. Amrouch, T. Ebi, J. Schneider, S. Parameswaran, J. Henkel, „**Analyzing the Thermal Hotspots in FPGA-based Embedded Systems“,** 23rd International Conference on Field Programmable Logic and Applications (FPL), Porto, Portugal, September 2013, pp. 1-4.
* H. Amrouch, T. Ebi, J. Henkel, „**Stress Balancing to Mitigate NBTI Effects in Register Files”,** The 43rd Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN'13), Budapest, Hungary, June 2013, pp. 1-10.
* J. Henkel, L. Bauer, N. Dutt, P. Gupta, S. Nassif, M. Shafique, M. Tahoori, N. Wehn, „**Reliable On-Chip Systems in the Nano-Era: Lessons Learnt and Future Trends“,** IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2013.
* J. Jahn, S. Pagani, S. Kobbe, J.-J. Chen, J. Henkel, „**Optimizations for Configuring and Mapping Software Pipelines in Many Core“,** IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2013.
* A. Singh, M. Shafique, A. Kumar, J. Henkel, „**Mapping on Multi/Many Core Systems: Survey of Current and Emerging Trends“,** IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2013.
* T. Li, M. Shafique, J.A. Ambrose, S. Rehman, J. Henkel, S. Parameswaran, „**RASTER: Runtime Adaptive Spatial/Temporal Error Resiliency for Embedded Processors“,** IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2013.
* M. Shafique, S. Rehman, P.V. Aceituno, J. Henkel, „**Exploiting Program-Level Masking and Error Propagation for Constrained Reliability Optimization“,** IEEE/ACM Design Automation Conference (DAC), Austin, TX, USA, June 2013.
* A. Amouri, H. Amrouch, T. Ebi, J. Henkel, M. Tahoori, „**Accurate Thermal-Profile Estimation and Validation for FPGA-Mapped Circuits“,** The 21st IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM'13), Seattle, Washington, USA, April 2013, pp. 57 - 60.
* S. Rehman, A. Toma, F. Kriebel, M. Shafique, J.-J. Chen, J. Henkel, „**Reliable Code Generation and Execution on Unreliable Hardware under Joint Functional and Timing Reliability Considerations“,** 19th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Philadelphia, USA, April 2013, pp. 273-282.
* A. Herkersdorf, M. Engel, M. Glaß, J. Henkel, V.B. Kleeberger, M.A. Kochte, J.M.  Kühn, S.R. Nassif, H. Rauchfuss, W. Rosenstiel, U. Schlichtmann, M. Shafique, M.B. Tahoori, J. Teich, N. Wehn, C. Weis, H.-J. Wunderlich, „**Cross-Layer Dependability Modeling and Abstraction in System on Chip“,** The 9th Workshop on Silicon Errors in Logic - System Effects (SELSE), Stanford, USA, March 2013.
* J. Jahn, J. Henkel, „**Pipelets: Self-Organizing Software Pipelines for Many Core Systems“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 1516-1521.
* F. Hameed, L. Bauer, J. Henkel, „**Adaptive Cache Management for a combined SRAM and DRAM Cache Hierarchy for Multi-Cores“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 77-82.
* Z.Wang, J. Henkel, „**Fast and accurate data cache modeling in source-level simulation of embedded software“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 587-592.
* C.-M. Hsieh, Z. Wang, J. Henkel, “**DANCE: Distributed Application-aware Node Configuration Engine in Shared Reconfigurable“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp.839-842.
* T. Li, M. Shafique, S. Rehman, S. Radhakrishnan, R. Ragel, J.A. Ambrose, J. Henkel, S. Parameswaran, “**CSER: HW/SW Configurable Soft-Error Resiliency for Application Specific Instruction-Set Processors”,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 707-712.
* S. Rehman, M. Shafique, P.V. Aceituno, F. Kriebel, J.-J. Chen, J. Henkel, “**Leveraging Variable Function Resilience for Selective Software Reliability on Unreliable Hardware“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 1759-1764.
* M. Shafique, B. Vogel, J. Henkel, „**Self-Adaptive Hybrid Dynamic Power Management for Many-Core Systems“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 51-56.
* F. Sampaio, B. Zatt, M. Shafique, L. Agostini, S. Bampi, J. Henkel, “**Energy-Efficient Memory Hierarchy for Motion and Disparity Estimation in Multiview Video Coding“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 665-670.
* M.U.K. Khan, J.M. Borrmann, L. Bauer, M. Shafique, J. Henkel, „**An H.264 Quad-FullHD Low-Latency Intra Video Encoder“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 115-120.
* M.U.K. Khan, M. Shafique, M. Grellert da Silva, J. Henkel, „**Hardware-Software Collaborative Complexity Reduction Scheme for the Emerging HEVC Intra Encoder“,** IEEE/ACM 16th Design Automation and Test in Europe Conference (DATE´13), Grenoble, France, March 2013, pp. 125-128.
* J. Henkel, T. Ebi, H. Amrouch, H. Khdr, „**Thermal Management for Dependable on-chip Systems“,** 18th Asia and South Pacific Design Automation Conference (ASP-DAC’13), Yokohama, Japan, January 2013, pp. 113-118.
* C. Hsieh, Z. Wang, J. Henkel, „**A Reconfigurable Hardware Accelerated Platform for Clustered Wireless Sensor Networks“,** IEEE 18th International Conference on Parallel and Distributed Systems (ICPADS 2012), Singapore, Singapore, December 2012, pp. 498-505.
* M. U. K. Khan, M. Shafique, J. Henkel, „**A Hierarchical Control Scheme for Energy Quota Distribution in Hybrid Distributed Video Coding“,** IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'12), Tampere, Finland, October 2012, pp. 483-492.
* Z. Wang, J. Henkel, „**HyCoS: Hybrid Compiled Simulation of Embedded Software with Target Dependent Code“,** IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'12), Tampere, Finland, October 2012, pp. 133-142.
* T. Ebi, H. Amrouch, J. Henkel, „**COOL: Control-based Optimization Of Load-balancing for Thermal Behavior“,** IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS'12), Tampere, Finland, October 2012, pp. 255-264.
* J. Jahn, S. Kobbe, S. Pagani, J. Chen, J. Henkel, „**Work in Progress: Malleable Software Pipelines for Efficient Many-core System Utilization“,** Proceedings of the 6th Many-core Applications Research Community (MARC) Symposium, Toulouse, France, July 2012, pp. 30-33.
* B. Vizzotto, B. Zatt, M. Shafique, S. Bampi, J. Henkel, “A Model Predictive Controller for Frame-Level Rate Control in Multiview Video Coding”, IEEE International Conference on Multimedia and Expo (ICME´12), Melbourne, Australia, July 2012, pp. 485-490.
* J. Feng, Z. Wang, J. Henkel, „**An Adaptive Data Gathering Strategy for Target Tracking in Cluster-based Wireless Sensor Networks“,** the 17th IEEE symposium on Computers and Communications (ISCC´12), Cappadocia, Turkey, June 2012, pp. 468-474.
* M. Abdelfattah, L. Bauer, C. Braun, M.E. Imhof, M.A. Kochte, H. Zhang, J. Henkel, H.-J. Wunderlich, „**Transparent Structural Online Test for Reconfigurable Systems“,** IEEE International On-Line Testing Symposium (IOLTS'12), Sitges, Spain, June 2012, pp. 37-42.
* L. Bauer, C. Braun, M. E. Imhof, M. A. Kochte, H. Zhang, H.-J. Wunderlich, J. Henkel, „**OTERA: Online Test Strategies for Reliable Reconfigurable Architectures“,** NASA/ESA Conference on Adaptive Hardware and Systems (AHS´12), Nuremberg, Germany, June 2012, pp. 38 - 45.
* M. Shafique, B. Zatt, F. L. Walter, S. Bampi, Jörg Henkel, “Adaptive Power Management of On-Chip Video Memory for Multiview Video Coding”, 49th ACM/EDA/IEEE Design Automation Conference (DAC´12), San Francisco, CA, USA, June 2012, pp. 866-875. **Best Paper Award**.
* S. Rehman, M. Shafique, Jörg Henkel, “Instruction Scheduling for Reliability-Aware Compilation”, 49th ACM/EDA/IEEE Design Automation Conference (DAC´12), San Francisco, CA, USA, June 2012, pp. 1288-1296. **Best Paper Award**.
* M. Shafique, B. Zatt, J. Henkel, “A Complexity Reduction Scheme with Adaptive Search Direction and Mode Elimination for Multiview Video Coding”, 29th Picture Coding Symposium (PCS´12), Kraków, Poland, May 2012, pp. 105-108.
* L. Bauer, A. Grudnitsky, M. Shafique, J. Henkel, “PATS: a Performance Aware Task Scheduler for Runtime Reconfigurable Processors”, 20th Annual International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM´12), Toronto, Canada, April/May 2012, pp. 208 - 215. **Best Paper Award**.
* C. Hsieh, Z. Wang, J. Henkel, „ECO/ee: Energy-aware Collaborative Organic Execution Environment for Wireless Sensor Networks“, IEEE Wireless Communications and Networking Conference (WCNC´12), Paris, France, April 2012, pp. 1998-2002.
* A.Grudnitsky, L. Bauer, J. Henkel, „Partial Online-Synthesis for Mixed-Grained Reconfigurable Architectures“, IEEE/ACM 15th Design Automation and Test in Europe Conference (DATE´12), Dresden, Germany, March 2012, pp. 1555 – 1560.
* F. Hameed, L. Bauer, J. Henkel, „Dynamic Cache Management in Multi-Core Architectures through Run-time Adaptation“, IEEE/ACM 15th Design Automation and Test in Europe Conference (DATE´12), Dresden, Germany, March 2012, pp. 485-490.
* Z. Wang, J. Henkel, „Accurate Source-Level Simulation of Embedded Software with Respect to Compiler Optimizations“, IEEE/ACM 15th Design Automation and Test in Europe Conference (DATE´12), Dresden, Germany, March 2012, pp. 382-387.
* M. Shafique, B. Zatt, S. Rehman, F. Kriebel, J. Henkel, “Power-Efficient Error-Resiliency for H.264/AVC Context-Adaptive Variable Length Coding”, IEEE/ACM 15th Design Automation and Test in Europe Conference (DATE´12), Dresden, Germany, March 2012, pp. 697-702.
* J. Henkel et al., „Invasive Manycore Architectures“, 17th Asia and South Pacific Design Automation Conference (ASP-DAC'12), Sydney, Australia, Jan.-Feb. 2012, pp. 193 - 200.
* S. Rehman, M. Shafique, F. Kriebel, J. Henkel, “RAISE: Reliability-Aware Instruction SchEduling for Unreliable Hardware”, 17th Asia and South Pacific Design Automation Conference (ASP-DAC'12), Sydney, Australia, Jan.-Feb. 2012, pp. 671-676.
* M.S. Srouji, Z. Wang, J. Henkel, “RDTS: A Reliable Erasure-Coding Based Data Transfer Scheme for Wireless Sensor Networks”, IEEE International Conference on Parallel and Distributed Systems (ICPADS'11), Tainan, Taiwan.
* B. Zatt, M. Shafique, S. Bampi, J. Henkel, “A Low-Power Memory Architecture with Application-Aware Power Management for Motion & Disparity Estimation in Multiview Video Coding”, IEEE/ACM 29th International Conference on Computer-Aided Design (ICCAD´11), pp. 40-47, 2011.
* H. Javed, M. Shafique, J. Henkel, S. Parameswaran, “System-Level Application-Aware Dynamic Power Management in Adaptive Pipelined MPSoCs for Multimedia”, IEEE/ACM 29th International Conference on Computer-Aided Design (ICCAD´11), pp. 616-623, 2011.
* M. Huebner, C. Tradowsky, D. Goehringer, L. Braun, F. Thoma, J. Henkel, J. Becker, “Dynamic processor reconfiguration”, IEEE International Conference on ReConFigurable Computing and FPGAs (ReConFig'11), Cancun, Mexico.
* J. Henkel et al., “Design and architectures for dependable embedded systems”, [IEEE International Conference on Hardware-Software Codesign and System Synthesis](http://www.codes-isss.org/) [(CODES+ISSS´11)](http://www.codes-isss.org/), Taipei, Taiwan, October 2011.
* S. Rehman, M. Shafique, F. Kriebel, J. Henkel, “Reliable Software for Unreliable Hardware: Embedded Code Generation aiming at Reliability Coding”, [IEEE International Conference on Hardware-Software Codesign and System Synthesis](http://www.codes-isss.org/) [(CODES+ISSS´11)](http://www.codes-isss.org/), Taipei, Taiwan, October 2011, (accepted for publication).
* B. Zatt, M. Shafique, S. Bampi, J. Henkel, “A Multi-Level Dynamic Complexity Reduction Scheme for Multiview Video Coding”, [IEEE 18th International Conference on Image Processing (ICIP´11)](http://www.icip2011.org/), Brussels, Belgium, September 2011.
* W. Ahmed, M. Shafique, L. Bauer, J. Henkel, “Adaptive Resource Management for Simultaneous Multitasking in Mixed-Grained Reconfigurable Multi-core Processors”, [IEEE International Conference on Hardware-Software Codesign and System Synthesis](http://www.codes-isss.org/) [(CODES+ISSS´11)](http://www.codes-isss.org/), Taipei, Taiwan, October 2011, (accepted for publication).
* T. Ebi, M.A. Al Faruque, J. Henkel, D. Kramer, W. Karl, “Economic Learning for Thermal-aware Power Budgeting in Many-core Architectures”, IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS´11), Taipei, Taiwan, October 2011 (accepted for publication).
* S. Kobbe, L. Bauer, J. Henkel, D. Lohmann, W. Schröder-Preikschat, “DistRM: Distributed Resource Management for On-Chip Many-Core Systems”, IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS´11), Taipei, Taiwan, October 2011 (accepted for publication).
* T. Ebi, H. Rauchfuss, A. Herkersdorf, J. Henkel, “Agent-based Thermal Management using Real-Time I/O Communication Relocation for 3D Many-Cores”, International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) 2011, Madrid, Spain, pp. 112-121.
* J. Henkel, L. Bauer, M. Hübner, A. Grudnitsky, “i-Core: A run-time adaptive processor for embedded multi-core systems”, International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA´11), Las Vegas, Nevada, USA, July 2011.
* S. Rehman, M. Shafique, F. Kriebel, J. Henkel, “ReVC: Computationally Reliable Video Coding on Unreliable Hardware Platforms: A Case Study on Error-Tolerant H.264/AVC CAVLC Entropy Coding”, [IEEE 18th International Conference on Image Processing (ICIP´11)](http://www.icip2011.org/), Brussels, Belgium, September 2011.
* M. Shafique, A. O. Tüfek, J. Henkel, “A High-Throughput Parallel Hardware Architecture for H.264/AVC CAVLC Encoding”, [IEEE 18th International Conference on Image Processing (ICIP´11)](http://www.icip2011.org/), Brussels, Belgium, September 2011, (accepted for publication).
* B. Zatt, M. Shafique, F. Sampaio, L. Agostini, S. Bampi, L. Henkel, “Run-Time Adaptive Energy-Aware Motion and Disparity Estimation in Multiview Video Coding”, [ACM/IEEE/EDA 48th Design Automation Conference (DAC´11)](http://www.dac.com/), San Diego, CA, USA, pp. 1026-1031, June 2011.
* H. Javed, M. Shafique, S. Parameswaran, J. Henkel, “Low-Power Adaptive Pipelined MPSoCs for Multimedia: An H.264 Video Encoder Case Study”, [ACM/IEEE/EDA 48th Design Automation Conference (DAC´11)](http://www.dac.com/), San Diego, CA, USA, pp. 1032-1037, June 2011.
* N. Iqbal, M. A. Saddique, J. Henkel, “SEAL: Soft Error Aware Low Power Scheduling by Monte Carlo State Space Under the Influence of Stochastic Spatial and Temporal Dependencies”, [ACM/IEEE/EDA 48th Design Automation Conference (DAC´11)](http://www.dac.com/), San Diego, CA, USA, June 2011.
* L. Bauer, M. Shafique, J. Henkel “Concepts, Architectures, and Run-time Systems for Efficient and Adaptive Reconfigurable Processors”, [NASA/ESA 6th Conference on Adaptive Hardware and Systems (AHS´11)](http://www.see.ed.ac.uk/ahs2011/), invited paper, San Diego, CA, USA, pp. 80-87, June 2011. MaXentric Technologies AHS **Best Paper Award**.
* P. Figuli. M. Huebner, R. Girardey, F. Bapp, T. Bruckschlögl, F. Thoma, J. Henkel, J. Becker, “A heterogeneous SoC architecture with embedded virtual FPGA cores and runtime core fusion”, NASA/ESA 6th Conference on Adaptive Hardware and Systems (AHS 2011),  San Diego, CA, USA, June 2011.
* J. Henkel, L. Bauer, M. Hübner, A. Grudnitsky, “i-Core: A run-time adaptive processor for embedded multi-core systems”, International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'11), Las Vegas, Nevada, USA.
* W. Ahmed, M. Shafique, L. Bauer, M. Hammerich, J. Henkel, J. Becker, “Run-Time Resource Allocation for Simultaneous Multi-Tasking in Multi-Core Reconfigurable Processors”, [IEEE 19th Symposium on Field-Programmable Custom Computing Machines (FCCM´11)](http://fccm.org/2011/), Salt Lake City, Utah, USA, pp. 29-32, May 2011.
* B. Oechslein, J. Schedel, J. Kleinöder, L. Bauer, J. Henkel, D. Lohmann, W. Schröder-Preikschat, “OctoPOS: A Parallel Operating System for Invasive Computing”, Systems for Future Multi-Core Architectures (SFMA), co-located with EuroSys 2011, Salzburg, Austria. April 2011.
* M. Shafique, L. Bauer, W. Ahmed, J. Henkel, “Minority-Game-based Resource Allocation for Run-Time Reconfigurable Multi-Core Processors”, [IEEE/ACM 14th Design Automation and Test in Europe Conference (DATE'11)](http://www.date-conference.com/), Grenoble, France, pp. 1261-1266, March 2011.
* B. Zatt, M. Shafique, S. Bampi, J. Henkel, “Multi-Level Pipelined Parallel Hardware Architecture for High Throughput Motion and Disparity Estimation in Multiview Video Coding”, [IEEE/ACM 14th Design Automation and Test in Europe Conference (DATE'11)](http://www.date-conference.com/), Grenoble, France, pp. 1448-1453, March 2011.
* W. Ahmed, M. Shafique, L. Bauer, J. Henkel, “mRTS: Run-Time System for Reconfigurable Processors with Multi-Grained Instruction-Set Extensions”, [IEEE/ACM 14th Design Automation and Test in Europe Conference (DATE'11)](http://www.date-conference.com/), Grenoble, France, pp. 1554-1559, March 2011.
* F. Hameed, M.A. Al Faruque, J. Henkel, “Dynamic Thermal Management in 3D Multi-Core Architecture through Run-time Adaptation”, [IEEE/ACM 14th Design Automation and Test in Europe Conference (DATE'11)](http://www.date-conference.com/), Grenoble, France, pp. 299-304, March 2011.
* J. Jahn, M.A. Al Faruque, J. Henkel, “CARAT: Context-Aware Runtime Adaptive Task Migration for Multi Core Architectures”, [IEEE/ACM 14th Design Automation and Test in Europe Conference (DATE'11)](http://www.date-conference.com/), Grenoble, France, pp. 515-520, March 2011.
* H. Amrouch, J. Henkel, “Self-Immunity Technique to Improve Register File Integrity against Soft Errors”, 24th International Conference on VLSI Design (VLSID'11), Chennai, India, pp. 189-194, January 2010.
* M. Shafique, B. Zatt, S. Bampi, J. Henkel, “Power-Aware Complexity-Scalable Multiview Video Coding for Mobile Devices”, [28th Picture Coding Symposium (PCS´10)](http://www.pcs2010.org), Nagoya, Japan, pp. 350-353, December 2010.
* B. Zatt, M. Shafique, S. Bampi, J. Henkel, “An Adaptive Early Skip Mode Decision Scheme for Multiview Video Coding”, [28th Picture Coding Symposium (PCS´10)](http://www.pcs2010.org), Nagoya, Japan, pp. 42-45, December 2010.
* M. Shafique, L. Bauer, J. Henkel, “Selective Instruction Set Muting for Energy-Aware Adaptive Processors”, [IEEE/ACM International Conference on Computer-Aided Design (ICCAD´10)](http://www.iccad.com/2010/index.html), San Jose, CA, USA, pp. 353-360, November 2010. ICCAD'10 Best Paper Nomination.
* N. Iqbal, J. Henkel, “SETS: Stochastic Execution Time Scheduling for Multicore Systems by Joint State Space and Monte Carlo”, [IEEE/ACM International Conference on Computer-Aided Design (ICCAD´10)](http://www.iccad.com/2010/index.html), San Jose, CA, USA, pp. 123-130, November 2010.
* T. Ebi, M.A. Al Faruque, J. Henkel, " NeuroNoC: Neural Network Inspired Runtime Adaptation for an On-chip Communication Architecture", [IEEE International Conference on Hardware-Software Codesign and System Synthesis](http://www.codes-isss.org/) [(CODES+ISSS´10)](http://www.codes-isss.org/), Scottsdale, Arizona, AZ, USA, pp. 223-230, October 2010.
* M. Shafique, L. Bauer, J. Henkel, "enBudget: A Run-Time Adaptive Predictive Energy-Budgeting Scheme for Energy-Aware Motion Estimation in H.264/MPEG-4 AVC Video Encoder", IEEE/ACM 13th Design Automation and Test in Europe Conference (DATE´10), Dresden, Germany, pp. 1725-1730, March 2010.
* R. Koenig, L. Bauer, T. Stripf, M. Shafique, W. Ahmed, J. Becker, J. Henkel, "KAHRISMA: A Novel Hypermorphic Reconfigurable-Instruction-Set Multi-grained-Array Architecture in: IEEE/ACM 13th. Design Automation and Test in Europe Conference (DATE´10), Dresden, Germany, pp. 819-824, March 2010.
* M. Shafique, B. Molkenthin, J. Henkel, "An HVS-based Adaptive Computational Complexity Reduction Scheme for H.264/AVC Video Encoder using Prognostic Early Mode Exclusion", IEEE/ACM 13th Design Automation and Test in Europe Conference (DATE´10), Dresden, Germany, pp. 1713-1718, March 2010.
* N. Iqbal, M. A. Saddique. J. Henkel, " DAGS: Distribution Agnostic Sequential Monte Carlo Scheme for Task Execution Time Estimation", IEEE/ACM 13th Design Automation and Test in Europe Conference (DATE´10), Dresden, Germany, pp. 1645-1648, March 2010.
* N. Iqbal, M. A. Saddique. J. Henkel, " RMOT: Recursion in Model Order for Task Execution Time Estimation in a Software Pipeline", IEEE/ACM 13th Design Automation and Test in Europe Conference (DATE´10), Dresden, Germany, pp. 953-956, March 2010.
* Th. Ebi, M. Al Faruque, J. Henkel, "TAPE: Thermal-Aware Agent-Based Power Economy for Multi/Many-Core Architectures", IEEE/ACM 27th. International Conference on Computer-Aided Design (ICCAD´09), San Jose, CA, USA, pp. 302-309. Nov. 2009, Received the IEEE/ACM William J. McCalla ICCAD **Best Paper Award**.
* M. Shafique, L. Bauer, J. Henkel, "REMiS: Run-time Energy Minimization Scheme in a Reconfigurable Processor with Dynamic Power-Gated Instruction Set", IEEE/ACM 27th. International Conference on Computer-Aided Design (ICCAD´09), San Jose, CA, USA, pp. 55-62., Nov. 2009.
* M. Shafique, B. Molkenthin, J. Henkel, "Non-Linear Rate Control for H.264/AVC Video Encoder with Multiple Picture Types using Image-Statistics and Motion-Based Macroblock Prioritization", 16th IEEE International Conference on Image Processing (ICIP´09), pp. 3429-3432, Nov. 2009.
* L. Bauer, M. Shafique, J. Henkel, "MinDeg: A Performance-guided Replacement Policy for Run-time Reconfigurable Accelerators", IEEE International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS´09), Grenoble, France, pp. 335-342, Oct. 2009.
* T. Bonny, J. Henkel, "LICT: Left-uncompressed Instructions Compression Technique to Improve the Decoding Performance of VLIW Processors", 46th ACM/EDA/IEEE Design Automation Conference (DAC´09), San Fransisco CA, USA, pp. 903-906, 2009.
* N. Iqbal, J. Henkel, "Efficient Constant-time Entropy Decoding for H.264", IEEE/ACM Design Automation and Test in Europe Conference (DATE’09), pp. 1440-1445, 2009.
* M.A. Al Faruque, T. Ebi, J. Henkel, "Configurable Links for Runtime Adaptive On-chip Communication", IEEE/ACM Design Automation and Test in Europe Conference (DATE’09), pp. 256-261, 2009.
* L. Bauer, M. Shafique, J. Henkel, "Cross-Architectural Design Space Exploration Tool for Reconfigurable Processors", IEEE/ACM Design Automation and Test in Europe Conference (DATE’09), pp. 1434-1439, 2009.
* M. Shafique, L. Bauer, J. Henkel, "A Parallel Approach for High Performance Hardware Design of Intra Prediction in H.264/AVC Video Codec", IEEE/ACM Design Automation and Test in Europe Conference (DATE’09), pp. 958-963, 2009.
* M. A. Al Faruque, T. Ebi, J. Henkel, " ROAdNoC: Runtime Observability for an Adaptive Network on Chip Architecture", IEEE/ACM International Conference on Computer-Aided Design (ICCAD'08), pp. 543-548, San Jose, 2008.
* T. Bonny, J. Henkel, "FBT: Filled Buffer Technique to reduce Code Size for VLIW Processors", IEEE/ACM International Conference on Computer-Aided Design (ICCAD'08), pp. 549-545, San Jose, 2008.
* L. Bauer, M. Shafique, J. Henkel, "A Computation- and Communication-Infrastructure for Modular Special Instructions in a Dynamically Reconfigurable Processor", IEEE 18th. International Conference on Field Programmable Logic and Applications (FPL’08), pp. 203-208, Heidelberg, Germany, 2008.
* M. Shafique, L. Bauer, J. Henkel, “3-Tier Dynamically AdaptivePower-Aware Motion Estimator for H.264/AVC Video Encoding”, IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED’08), Bangalore, India, pp. 147-152, August 2008.
* L. Bauer, M. Shafique, J. Henkel, "Run-time Instruction Set Selection in a Transmutable Embedded Processor", ACM/IEEE 45th. Design Automation Conference (DAC’08), Anaheim, pp. 55-61, June 2008.
* M.A. Al Faruque, R. Krist, J. Henkel, "ADAM: Run-time Agent-based Distributed Application Mapping for on-chip Communication", ACM/IEEE 45th. Design Automation Conference (DAC’08), pp. 760-765, Anaheim, June 2008.
* L. Bauer, M. Shafique, S. Kreutz, J. Henkel, "Run-time System for an Extensible Embedded Processor with Dynamic Instruction Set", Proc. of IEEE/ACM Design Automation and Test in Europe Conference (DATE’08), pp. 752-757, Munich, Germany, 2008. **Best Paper Award**.
* M. A. Al Faruque, J. Henkel, "Minimizing Virtual Channel Buffer for Routers in On-chip Communication Architectures", Proc. of IEEE/ACM Design Automation and Test in Europe Conference (DATE’08), pp. 1238-1243, Munich, Germany, 2008..
* T. Bonny, J. Henkel, "Instruction Re-encoding Facilitating Dense Embedded Code", Proc. of IEEE/ACM Design Automation and Test in Europe Conference (DATE’08), pp. 770-775, Munich, Germany, 2008.
* D. Hillenbrand, J. Henkel, "Block Cache for Embedded Systems", Proc. of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC'08) Seoul, Korea (accepted).
* Al Faruque, M.A., Ebi, T., Henkel, J., „Run-time Adaptive on-chip Communication Scheme“, IEEE/ACM International Conference on Computer-Aided Design (ICCAD'07), pp. 26-31, San Jose, Nov. 2007.
* Bauer, L., Shafique, M., Henkel, J., „Efficient Resource Utilization for an Extensible Processor through Dynamic Instruction Set Adaptation“ 5th Workshop on Application Specific Processors (WASP'07), Salzburg, Austria, pp. 39-46. Oct. 2007
* Shafique, M., Bauer, L., Henkel, J., „Optimized Application Architecture of the H.264 Video Encoder for Application Specific Platforms“, IEEE 5th Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia'07), Salzburg, Austria, pp. 119-124. Oct. 2007
* Al Faruque, M.A., Henkel, J., „Transaction Specific Virtual Channel Allocation in QoS Supported On-chip Communication“, IEEE/ACM 18th. International Conference on Application-specific Systems, Architectures and Processors (ASAP'07), Montreal , Canada, pp. 48-53. July 2007
* Bauer, L., Shafique, M., Teufel, D., Henkel, J., „A Self-Adaptive Extensible Embedded Processor“ , IEEE/ACM International Conference on Self-Adaptive and Self-Organizing Systems (SASO'07), Boston, MA, USA, pp. 344-347. July 2007
* Bauer, L., Shafique, M., Kramer, S., Henkel, J., „RISPP: Rotating Instruction Set Processing Platform“, ACM/IEEE/EDA 44th. Design Automation Conference (DAC'07), San Diego, CA, USA, pp. 791-796. June 2007
* Bonny, T.,Henkel, J., „Instruction Splitting for Efficient Code Compression“, ACM/IEEE/EDA 44th. Design Automation Conference (DAC'07), San Diego, CA, USA, pp. 646-651. June 2007
* Janapsatya, A., Ignjatovic, A., Parameswaran, S., Henkel, J., „Instruction Trace Compression for Rapid Instruction Cache Simulation“, IEEE/ACM Design Automation and Test in Europe Conference (DATE'07), Nice, France, pp. 803-808. April 2007
* Bonny, T., Henkel, J., „Efficient Code Density Through Look-up Table Compression“, IEEE/ACM Design Automation and Test in Europe Conference (DATE'07), Nice, France, pp. 809-814. April 2007
* Al Faruque, M.A., Weiss, G., Henkel, J., „Bounded Arbitration Algorithm for QoS-Supported On-chip Communication“ IEEE/ACM Int'l Conference on Hardware/Software Co-Design and System Synthesis (Codes+ISSS'06), Seoul, Korea. Oct. 2006
* Bonny, T.; Henkel, J., „Using Lin-Kernighan Algorithm for Look-up Table Compression to Improve Code Density“, Proc. of IEEE/ACM 16th. Great Lakes Symposium on VLSI (GLSVLSI'06), Philadelphia, USA, pp. 259-265. Apr. 30 - May 2, 2006
* Al Faruque, M.A., YE, X., Weiss, G., Henkel, J., „QoS-Oriented Configurable Networks on Chip“, Poster in: Workshop Future Interconnects and Networks on Chip in Design Automation and Test in Europe (DATE'06), Munich, Germany March 2006
* Lekatsas, H., Henkel, J., Jakkula, V., Chakradhar, S., „Using Shiftable Content Addressable Memories to Double Memory Capacity on Embedded Systems“, IEEE 19th. International Conference on VLSI Design 2006, pp. 639-644, Jan. 3.-7. 2006
* Xu, J.,Wolf, W., Henkel, J., Chakradhar, S. „H. 264 HDTV Decoder Using Application-Specific Networks-On-Chip“, IEEE International Symposium on Multimedia and Expo, ICME'05, Amsterdam, The Netherlands, pp. 1508-1511, July 6-8, 2005
* Xu, J., Wolf, W., Henkel, J., Chakradhar, S. „A methodology for design, modeling, and analysis of networks-on-chip“, IEEE International Symposium on Circuits and Systems, ISCAS'05, Vol.2, Kobe, Japan, pp. 1778-1781, May 23-26, 2005
* Lekatsas, H., Henkel, J., Jakkula, V., Chakradhar, S. „A unified architecture for adaptive compression of data and code on embedded systems“ ,IEEE Proc. of 18th. the International Conference on VLSI Design 2005, Kolkata, pp. 117-123, Jan. 3-7, 2005
* Cheung, N., Parameswaran, S., Henkel, J. „Battery-Aware Instruction Generation for Embedded Processors“, IEEE Asia South Pacific Design Automation Conference, ASP-DAC'05, Shanghai, China, pp. 553-556, Jan. 2005
* Kalla, P., Hu, X.S., Henkel, J., „A Flexible Framework for Communication Evaluation in SoC Design“, IEEE Asia South Pacific Design Automation Conference, ASP-DAC'05, Shanghai, China, pp. 956-959, Jan. 2005
* Cheung, N., Parameswaran, S., Henkel, J., „A Quantitative Study and Estimation Models for Extensible Instructions in Embedded Processors“, IEEE/ACM Proc. of International Conference on Computer-Aided Design, ICCAD'04, San Jose, California, USA, pp. 183-189, Nov. 2004
* Marculescu, R., Henkel, J.Pedram, M., „Quo Vadis Multimedia? From Desktop Multimedia to Distributed Multimedia Systems“, EEE/ACM Proc. of Design Automation and Test in Europe Conference, DATE’04, Paris, pp. 1020-1025, Feb. 2004
* J. Xu, W. Wolf, J. Henkel, S. Chakradhar, T. Lv, “A case study in networks-on-chip design for embedded video”, IEEE/ACM IEEE/ACM Proc. of Design Automation and Test in Europe Conference and Exhibition (DATE’04), pp.770-775, Feb. 2004.
* N. Cheung, S. Parameswaran, J. Henkel, J. Chan, “MINCE: matching instructions using combinational equivalence for extensible processor”, IEEE/ACM Proc. of Design Automation and Test in Europe Conference and Exhibition, pp. 1020-1025, Feb. 2004.
* J. Henkel, W. Wolf, S. Chakradhar, “On-chip networks: a scalable, communication-centric embedded system design paradigm”, IEEE Proc. of 17th. International Conference on VLSI Design (VLSI’04), pp.845-851, 2004.
* R. Marculescu, M. Pedram, J. Henkel, “Distributed multimedia system design: a holistic perspective”, IEEE/ACM Proc. of Design Automation and Test in Europe Conference (DATE’04), pp.1342-1347, Feb. 2004.
* P. Kalla, X.S. Hu, J. Henkel, “LRU-SEQ: a novel replacement policy for transition energy reduction in instruction caches”, IEEE/ACM Proc. of International Conference on Computer Aided Design, pp. 518-522, Nov. 2003.
* N. Cheung, S. Parameswaran, J. Henkel “INSIDE: Instruction Selection/Identification & Design Exploration for extensible processors”, IEEE/ACM Proc. of International Conference on Computer Aided Design, pp. 291-297, 9-13 Nov. 2003.
* P. Kalla, J. Henkel, X. S. Hu, ”SEA: fast power estimation for micro-architectures”, IEEE Proc. of 5th. International Conference on ASIC, pp.1200, Oct. 2003.
* T. Lv, J. Henkel, H. Lekatsas, W. Wolf, ”Enhancing signal integrity through a low-overhead encoding scheme on address buses”, IEEE/ACM Proc. of Design Automation and Test in Europe Conference and Exhibition (DATE’03), pp. 542-547, 2003.
* H. Lekatsas, J. Henkel, S. Chakradhar, V. Jakkula, M. Sankaradass, “CoCo: a hardware/software platform for rapid prototyping of code compression technique”, IEEE/ACM Proc. of Design Automation Conference (DAC’03), pp. 306-311, June 2003.
* N. Cheung, J. Henkel, S. Parameswaran, ”Rapid configuration and instruction selection for an ASIP: a case study”, IEEE/ACM Proc. of Design Automation and Test in Europe Conference and Exhibition (DATE’03), pp. 802-807, 2003.
* P. Kalla, J. Henkel, X.S. Hu, ”SEA: fast power estimation for micro-architectures”, IEEE/ACM Proc. of Asia and South Pacific Design Automation Conference (ASP-DAC’03), pp. 600-605, 2003.
* S. Parameswaran, J. Henkel, H. Lekastas, ”Multi-parametric improvements for embedded systems using code-placement and address bus coding”, IEEE/ACM Proc. of Asia and South Pacific Design Automation Conference (ASP-DAC’03), pp. 15-21, 2003.
* R. Chandra, J. Henkel, P.R. Panda, S. Parameswaran, L. Ramachandran, ”Specification and design of multi-million gate SOCs” (tutorial), IEEE Proc. 16th. International Conference on VLSI Design (VLSI’03), pp. 18-19, 2003.
* H. Lekatsas, J. Henkel, V. Jakkula, “Design of an One-cycle Decompression Hardware for Performance Increase in Embedded Systems”, IEEE/ACM Proc. of 39th. Design Automation Conference (DAC’02), pp.34-39. June 2002.
* H. Lekatsas, J. Henkel, V. Jakkula, “1-Cycle Code Decompression Circuitry for Performance Increase of Xtensa-1040-based Embedded Systems“, IEEE Proc. of Custom Integrated Circuits Conference (CICC’02), pp. 9-12, May 2002.
* T. Lv, J. Henkel, H. Lekatsas, W. Wolf, "An Adaptive Dictionary Encoding Scheme for SOC Data Buses", IEEE/ACM Proc. of Design Automation and Test in Europe Conference 2002 (DATE’02), pp.1059-1064, March 2002.
* T. M. Lee, J. Henkel, W. Wolf, "Dynamic Runtime Re-Scheduling Allowing Multiple Implementations of a Task for Platform-based Designs", IEEE/ACM Proc. of Design Automation and Test in Europe Conference (DATE’02), pp.296-301, March 2002.
* J. Henkel, H. Lekatsas, V. Jakkula, “Encoding Schemes for Address Buses in Energy Efficient SOC Designs”, Proc. of 11th. IFIP International Conference on Very Large Scale Integration (VLSI-SOC ‘01), pp.242-246, Dec’01.
* H. Lekatsas, J. Henkel, “ETAM++: Extended Transition Activity Measure for Low Power Address Bus Designs”, Proc. of IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC’02), pp.113-120, Jan’02.
* S. Parameswaran, J. Henkel, “I-CoPES: Fast Instruction Code Placement for Embedded Systems to Improve Performance and Energy Effciency”, Proc. of IEEE/ACM International Conf. on CAD (ICCAD’01), pp.635-641, Nov. 2001.
* T. Givargis, F. Vahid, J. Henkel, “System-level Exploration for Pareto-optimal Configurations in Parameterized System Designs”, Proc. of IEEE/ACM International Conf. on CAD (ICCAD’01), pp.25-30, Nov. 2001.
* H. Lekatsas, J. Henkel, W. Wolf, “Design and Simulation of a Pipelined Decompression Architecture for Embedded Systems”, IEEE/ACM 14th. International Symposium on System Synthesis (ISSS’01), (accepted for publication). pp. 63-68, Sep. 2001.
* W. Wolf, J. Henkel, “Platform-Based Design”, presented as tutorial at IEEE/ACM Design and Test in Europe Conference (DATE’01), March 2001.
* J. Henkel, H. Lekatsas, “A2BC: Adaptive Address Bus Coding for Low Power Deep Sub-micron Designs”, Proc. of IEEE/ACM 38th. Design Automation Conference (DAC’01), pp. 744-749, June 2001.
* T. Givargis, F. Vahid, J. Henkel, “Trace-driven System-level Power Evaluation of System-on-a-Chip Cores”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC’01), pp. 306-311, Feb. 2001.
* J. Henkel, X. S. Hu, “Quo Vadis SLD ?” (invited), System Level Design Special Report, Electronic News Online, Cahners, Dec. 18th. 2000.
* H. Lekatsas. J. Henkel, W. Wolf, “A Decompression Architecture for Low Power Embedded Systems”, IEEE/ACM Proc. of International Conference on Computer Design (ICCD’00), pp. 571-574, 2000.
* T. Givargis, F. Vahid, J. Henkel, “Instruction-based System-level Power Evaluation of System-on-a-chip Peripheral Cores”, IEEE/ACM 13th. International Symposium on System Synthesis (ISSS’00), pp.163-169, 2000.
* H. Lekatsas, J. Henkel, W. Wolf, “Code Compression for Low Power Embedded Systems Design”, IEEE/ACM 37th. Design Automation Conference (DAC’00), pp.294-299, June 2000.
* H. Lekatsas, J. Henkel, W. Wolf, “Code Compression as a Variable in Hardware/Software Co-Design”, Proc. of 8th. IEEE/ACM International Workshop on Hardware/Software Codesign (Codes’00), pp. 120-124, May 2000.
* T. Givargis, F. Vahid, J. Henkel, “Fast Cache and Bus Power Estimation for Parameterized System-on-a-Chip Design”, IEEE/ACM Conference on Design Automation and Test in Europe Conference (DATE’00), pp.333-338, March 2000.
* H. Lekatsas, J. Henkel, W. Wolf, “Arithmetic Coding for Low Power Design”, IEEE International Data Compression Conference (DCC’00), pp.430-439, March 2000 .
* T. Givargis, F. Vahid, J. Henkel, “A hybrid approach for core-based system-level power modeling”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC’00), pp.141-145, 2000.
* J. Henkel, “IP-based low power hardware/software partitioning”, Proc. of IFIP WG10.5, International Workshop on IP Based Synthesis and Design, Grenoble, France, Dec. 1999.
* J. Henkel, “A Low Power Hardware/Software Partitioning Approach for Core-based Embedded Systems”, IEEE/ACM 36th. Design Automation Conference (DAC’99), pp.122-127, 1999.
* T. Givargis, J. Henkel, F. Vahid, “Interface and Cache Power Exploration for Core-based Embedded Systems Design”, IEEE/ACM International Conf. on CAD (ICCAD’99), pp.270-273, 1999.
* J. Henkel, “A Methodology for Minimizing Power Dissipation of Embedded Systems through Hardware/Software Partitioning”, IEEE Proc. of Grand Lakes Symposium on VLSI, pp.86-89, March 1999.
* J. Henkel, F. Vahid, Invited Half-Day Tutorial: “Core-based Design of Systems on a Chip”, tutorial held at 11th. IEEE Int'l ASIC Conference, Rochester, NY, 13th. Sept. 1998.
* Y. Li, J. Henkel, “A Framework for Estimating and Minimizing Energy Dissipation of Embedded HW/SW Systems”, IEEE/ACM 35th. Design Automation Conference (DAC’98) 1998, pp.188-193, 1998.
* J. Henkel, Y. Li, “Energy-Conscious HW/SW-Partitioning of Embedded Systems: A Case Study on an MPEG-2 Encoder”, IEEE/ACM Proc. of 6th. International Workshop on Hardware/Software Codesign, pp. 23-27, 1998.
* Y. Li, W. Wolf, J. Henkel, “Task-level Memory Hierarchy Synthesis for Low Power Real-Time Systems”, 6th. IEEE/ACM International Workshop on Hardware/Software Codesign, 1998.
* J. Henkel, R. Ernst, “High-Level Estimation Techniques for Usage in Hardware/Software Co-Design”, IEEE Proc. of Asia and South Pacific DAC'98, pp. 353-360, 1998.
* J. Henkel, R. Ernst, “A Hardware/Software Partitioner using a dynamically determined Granularity”, IEEE/ACM Proc. of 34th. Design Automation Conference (DAC) 1997, pp. 691-696, 1997.
* J. Henkel, F. Vahid, L. Ramachandran, Half-Day Tutorial: “Hardware/Software Co--design of Embedded Systems”, IEEE/ACM European Design and Test Conf. 97, Paris, France, March 17th. 1997.
* J. Henkel, R. Ernst, “The Interplay of Run-Time Estimation and Granularity in HW/SW Partitioning”, IEEE/ACM Proc. of 4th. IEEE International Workshop on Hardware/Software Codesign, Pittsburgh, pp. 52-58, 1996.
* J. Henkel, F. Vahid, L. Ramachandran, Full-Day Tutorial: “Hardware/Software Codesign of Embedded Systems”, Scriptum of tutorial, International Conference on CAD (ICCAD) 1995, San Jose, CA, 1995.
* J. Henkel, R. Ernst, “A Path-Based Estimation Technique for Estimating Hardware Runtime in HW/SW-Cosynthesis”, IEEE/ACM Proc. of 8th. International Symposium on System Synthesis, pp. 116-121, 1995.
* J. Henkel, R. Ernst, U. Holtmann, Th. Benner, “Adaptation of Partitioning and High-Level Synthesis in Hardware/Software Co-Synthesis”, IEEE/ACM Proc. of International Conference on CAD, pp. 96-100, 1994.
* D. Herrmann, J. Henkel, R. Ernst, “An approach to the adaptation of estimated cost parameters in the COSYMA system”, IEEE/ACM Proc. of 3rd. IEEE International Workshop on Hardware/Software Codesign, pp. 100-107, 1994.
* J. Henkel, R. Ernst, H. Grosenick, P. Lueders, Th. Benner, “Visualisierung der Datenstrukturen des Hardware/Software Co-Entwurf Systems COSYMA” 6. E.I.S. Workshop, Tuebingen, Germany, pp. 86-92, Nov. 1993.
* Th. Benner, J. Henkel, R. Ernst, “Interne Darstellung von Hardware/Software Systemen”, GI/ITG--Workshop "CAD--Umgebungen und Methoden des Entwurfs von Schaltkreisen und Systemen", Dresden, Germany, 1993.
* J. Henkel, Th. Benner and R. Ernst, “Hardware generation and partitioning effects in the COSYMA system”, 2nd. IEEE/ACM International Workshop on Hardware--Software Codesign, Cambridge, Massachusetts, 7.-8. Oct. 1993.
* Th. Benner, J. Henkel, R. Ernst, “Internal Representation of Embedded Hardware/Software-Systems”, Codes/CASHE Workshop, Innsbruck, Austria, 1993.
* R. Ernst, J. Henkel, “Hardware-Software Codesign of Embedded Controllers Based on Hardware Extraction”, 1st. International Workshop on Hardware-Software Co-Design, Estes Park, Colorado, 1992.
* J. Henkel, R. Ernst, “Hardware/Software-Co-Design fuer Mikrocontroller”, Workshop fuer Entwurfsmethodik fuer Integrierte Schaltungen und Systeme, Darmstadt, Germany, 1992.