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Customized Checkerboard Test Structures to Localize Interconnection Point Defects

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Abstract — **To localize point defects that occur inside numerous interconnection layers, a multilevel Checkerboard Test Structure is presented. Here, the large defect sensitive area inside boundary pads is divided into many distinguishable subchips. To provide test structure data that reflect yield of product chips, each subchip layout will be customized to real circuit designs of product chips. Defects are detected and localized by simple electrical measurements. Only the layer specific defect localization enables precise defect parameter extraction to provide detailed defect statistics and process problem debugging.**

1 Introduction

TODAY'S complexity of integrated circuits require more and more interconnection layers to connect all circuit cells and devices. For that, typical interconnection defects like intermetal shorts and virtual vias as well as the 3D-influence of underlying layers gain more importance on chip yield and defect statistics [StRo95], [Maly90], [Walk87]. To get defect statistics, simple test structures of comb and serpentine lines are commonly used [LYWM86]. But, often the yield of these test structures does not fit to observed yield of product chips within the same fab.

So, especially designed test structures to control process steps for polysilicon and metal layers are on demand. Two major methods to organize test chips are known, the "2 by N" probe-pad array [Bueh79] and standard boundary pads. To detect random point defects, the defect sensitive area inside a "2 by N" array is relatively small so that the large sensitive area inside the boundary pads seems to be more suitable. But here the number of pads is relatively small so that methods are required to separate and localize defects.

So, we decide to develop large area test chips to improve accuracy of defect statistics. The following Section describes the design principle of the Checkerboard Test Structure. Section 3 presents the procedure to include customized circuit layouts of product chips to that test structure. Section 4 deals with the digital measurement procedure and the localization of electrically detected defects. Section 5 gives some experimental results and finally we conclude our approach.

2 Checkerboard Test Structure

An undesigned short circuit defect is only detectable between test structure layout elements connected to electrically distinguishable pads. For that, all test structure layout objects that are connected to one single pad are called a **Permutation Line**. To increase the number of separable short circuits without increasing the number P of pads, all possible $\frac{1}{2}\cdot P\cdot(P-1)$ neighborhood relationships of Permutation Lines have to be arranged inside a test chip. To also localize these short circuits, each neighborhood relationship has to be implemented exactly once inside the test chip area. For that, each Permutation Line has to be adjacent to every other Permutation Line just once. The **Permutation Procedure** introduced in [HeSt94] arranges all pairs of Permutation Lines without crossing each other in the rows of a **Permutation Matrix** so that each pair of Permutation Lines exists once for m different index values.

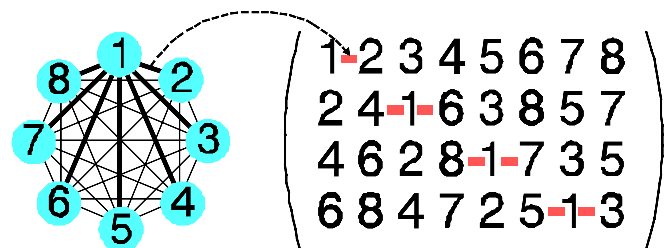

Fig. 1: Example of the Permutation Procedure for $m=8$ values.
Left: Complete neighborhood graph introduced by [HeWe94]:
node: Permutation Line connected to one pad.
edge: Two nodes are connected by an edge if the Permutation Lines connected to these pads are adjacently placed anywhere inside a test chip with only nonconducting material between them.
Right: Permutation Matrix, where the gray boxes mark pairs to line "1".

The following equation will be used to calculate the elements $a[i,j]$ of the Permutation Matrix, where the number m of used index values has to be even.

$$
a[i,j] := \begin{cases} j+2\cdot i-2 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i \le \frac{m-j+2}{2} \\ 2\cdot m-j-2\cdot i+3 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i > \frac{m-j+2}{2} \\ 2\cdot i-j-1 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i > \frac{j+1}{2} \\ j-2\cdot i+2 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i \le \frac{j-1}{2} \end{cases} \qquad \textbf{(1)}
$$

i : row index of the Permutation Matrix
j : column index of the Permutation Matrix

To enable the separation and localization of defects anywhere inside or in-between multilevel interconnection layers the two-dimensional Permutation Matrix will be copied one above another which results in the following **Vector Matrix**:

$$
V(m,C) := \begin{pmatrix} \begin{pmatrix} (C-1)m-a[1,1] \\ \vdots \\ 2m+a[1,1] \\ m+a[1,1] \\ a[1,1] \end{pmatrix}_{1,1} & \begin{pmatrix} (C-1)m-a[1,2] \\ \vdots \\ 2m+a[1,2] \\ m+a[1,2] \\ a[1,2] \end{pmatrix}_{1,2} & .. & \begin{pmatrix} (C-1)m-a[1,j] \\ \vdots \\ 2m-a[1,j] \\ m-a[1,j] \\ a[1,j] \end{pmatrix}_{1,j} \\ \begin{pmatrix} (C-1)m-a[2,1] \\ \vdots \\ 2m+a[2,1] \\ m+a[2,1] \\ a[2,1] \end{pmatrix}_{2,1} & \begin{pmatrix} (C-1)m-a[2,2] \\ \vdots \\ 2m+a[2,2] \\ m+a[2,2] \\ a[2,2] \end{pmatrix}_{2,2} & .. & \begin{pmatrix} (C-1)m-a[2,j] \\ \vdots \\ 2m-a[2,j] \\ m-a[2,j] \\ a[2,j] \end{pmatrix}_{2,j} \\ & \vdots & & \\ \begin{pmatrix} (C-1)m-a[i,1] \\ \vdots \\ 2m+a[i,1] \\ m+a[i,1] \\ a[i,1] \end{pmatrix}_{i,1} & \begin{pmatrix} (C-1)m-a[i,2] \\ \vdots \\ 2m+a[i,2] \\ m+a[i,2] \\ a[i,2] \end{pmatrix}_{i,2} & .. & \begin{pmatrix} (C-1)m-a[i,j] \\ \vdots \\ 2m-a[i,j] \\ m-a[i,j] \\ a[i,j] \end{pmatrix}_{i,j} \end{pmatrix} \qquad \textbf{(2)}
$$

It can be seen that all layers base on the same Permutation Matrix, just increasing the index values in a multiple of *m*. The number of values of one vector corresponds to the number *C* of conducting interconnection levels. The following example shows a Vector Matrix for *m=8* values and *C=3* layer.

$$
V(8,3) := \begin{pmatrix} \begin{pmatrix}17\\9\\1\end{pmatrix}_{1,1} & \begin{pmatrix}18\\10\\2\end{pmatrix}_{1,2} & \begin{pmatrix}19\\11\\3\end{pmatrix}_{1,3} & \begin{pmatrix}20\\12\\4\end{pmatrix}_{1,4} & \begin{pmatrix}21\\13\\5\end{pmatrix}_{1,5} & \begin{pmatrix}22\\14\\6\end{pmatrix}_{1,6} & \begin{pmatrix}23\\15\\7\end{pmatrix}_{1,7} & \begin{pmatrix}24\\16\\8\end{pmatrix}_{1,8} \\ \begin{pmatrix}18\\10\\2\end{pmatrix}_{2,1} & \begin{pmatrix}20\\12\\4\end{pmatrix}_{2,2} & \begin{pmatrix}17\\9\\1\end{pmatrix}_{2,3} & \begin{pmatrix}22\\14\\6\end{pmatrix}_{2,4} & \begin{pmatrix}19\\11\\3\end{pmatrix}_{2,5} & \begin{pmatrix}24\\16\\8\end{pmatrix}_{2,6} & \begin{pmatrix}21\\13\\5\end{pmatrix}_{2,7} & \begin{pmatrix}23\\15\\7\end{pmatrix}_{2,8} \\ \begin{pmatrix}20\\12\\4\end{pmatrix}_{3,1} & \begin{pmatrix}22\\14\\6\end{pmatrix}_{3,2} & \begin{pmatrix}18\\10\\2\end{pmatrix}_{3,3} & \begin{pmatrix}24\\16\\8\end{pmatrix}_{3,4} & \begin{pmatrix}17\\9\\1\end{pmatrix}_{3,5} & \begin{pmatrix}23\\15\\7\end{pmatrix}_{3,6} & \begin{pmatrix}19\\11\\3\end{pmatrix}_{3,7} & \begin{pmatrix}21\\13\\5\end{pmatrix}_{3,8} \\ \begin{pmatrix}22\\14\\6\end{pmatrix}_{4,1} & \begin{pmatrix}24\\16\\8\end{pmatrix}_{4,2} & \begin{pmatrix}20\\12\\4\end{pmatrix}_{4,3} & \begin{pmatrix}23\\15\\7\end{pmatrix}_{4,4} & \begin{pmatrix}18\\10\\2\end{pmatrix}_{4,5} & \begin{pmatrix}21\\13\\5\end{pmatrix}_{4,6} & \begin{pmatrix}17\\9\\1\end{pmatrix}_{4,7} & \begin{pmatrix}19\\11\\3\end{pmatrix}_{4,8} \end{pmatrix}
$$

Now the matrices have to be translated into a test structure design. An obvious approach to the separation and localization of defects is to partition the chip area into a large number of subchips, each containing one pair of Permutation Lines per layer. So, each value of the Vector Matrix will be replaced by a vertical line generating rectangular subchips. The checkered arrangement of subchips is responsible for the naming of the **Checkerboard Test Structure**. The Checkerboard Test Structure for the Vector Matrix *V(8,3)* introduced above can be seen in Figure 2, where just the indices of the Permutation Lines within the lowest layer are visible. Here for instance, those subchips are patterned that contain the Permutation Line index "1" (ref. Figure 1).

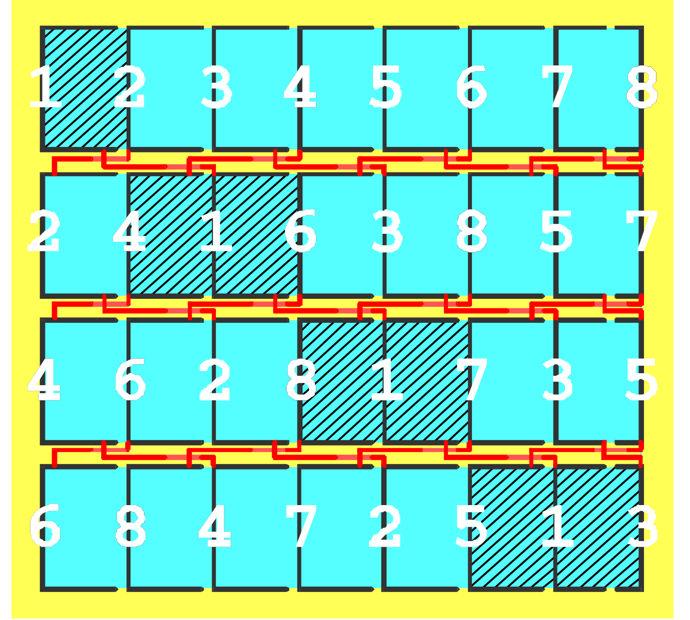

Fig. 2: Transformation of the lowest layer of the Vector Matrix to a Checkerboard Test Structure, where the Vector Matrix bases on a Permutation Matrix of *m=8*.

Inside these subchips, customized layout designs will be placed to detect the defects. Between adjacent subchip rows, a routing channel provides the connection of Permutation Lines referring to the same index value. All routing channels are identical. The basic principle to design a routing channel is described in the Appendix A of [HeSt94]. The principle shown in Figure 2 will be individually done per layer and finally all single layer frame designs will be arranged one above another. The equations of the following Table 1 are used to dimension the Checkerboard Test Structure.

Equation	No.
$m := \left(\frac{P}{C} \text{ div } 2\right)\cdot 2$ thus $\frac{m}{2}\in\mathbb{N}$ m : even number of individual values inside a Permutation Matrix P : number of pads C : number of (semi-)conducting interconnection layers	**(3)**
$P = m \cdot C$	**(4)**
$x_{chip} = (m-1)\cdot x_{subchip}$ x_{chip} : extension of test chip in x-direction x_{sub} : extension of subchip in x-direction	**(5)**
$y_{chip} = ½\cdot m\cdot y_{subchip}$ y_{chip} : extension of test chip in y-direction y_{sub} : extension of subchip in y-direction	**(6)**
$S := ½\cdot m\cdot(m-1)$ S : number of subchips inside Checkerboard Test Structure	**(7)**

Tab. 1: Equations to dimension a Checkerboard Test Structure.

The first step is always to determine the number of values inside a Permutation Matrix. Then either the size of the subchips will be calculated for a given size of a test chip or the test chip size results in a given size of a subchip layout. If for instance a functional tester having $P=48$ bidirectional channels will be available to measure a manufactured 2-level Checkerboard Test Structure, we get $m=24$ values to calculate the Permutation Matrix. If also a still existing probecard will be used, the corresponding pad frame ($P\geq48$) limits the chip size to $x_{chip} \cdot y_{chip}$. Then, the equations (6) and (7) result in a subchip size of $x_{sub} \cdot y_{sub}$. So, all in all 276 subchips will be provided to include real circuit layout designs to detect point defects.

The following Figure 3 shows the frame of a designed Checkerboard Test Structure. At the boundary of each subchip there is a unique set of Permutation Lines that are all connected to different pads. Here, for example, all Permutation Lines connected to two pads are highlighted. Both lines are neighbored in one subchip only (row four and column ten), which is the key to the defect localization facility.

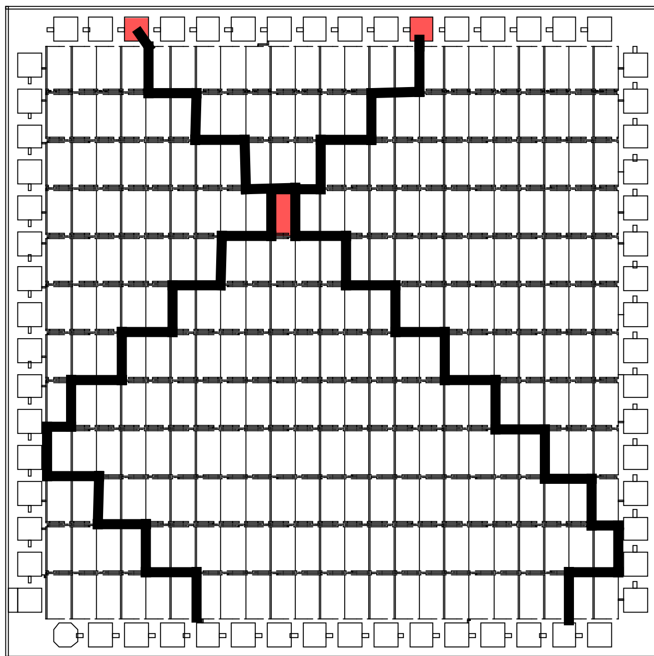

Fig. 3: Frame of a Checkerboard Test Structure with 276 subchips.

3 Customized Layout inside Subchips

Each subchip contains a unique pair of Permutation Lines per layer. So, within a layer each layout element inside the subchip has to be connected to either the left vertical Permutation Line or the right vertical Permutation Line. This has to be done individually for each layer. To also enable the localization of short circuits within different layers, the following Figure 4 shows two neighborhood graphs, where the nodes stand for the Permutation Lines inside a three-layer subchip. The Vector Matrix of Equation (2) only provides a clear localization of short circuits for the neighborhood relationships shown on the left neighborhood graph. So, the layout elements inside a subchip should be arranged in a way that minimizes the neighborhood relationships shown in the right neighborhood graph. Often, this is of no consequence because defects that results in multiple short circuits connect more than just two Permutation Lines. So, at least one edge of the left neighborhood graph is involved too.

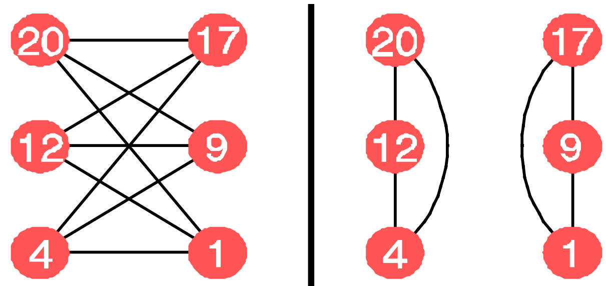

Fig. 4: Neighborhood graphs of the Permutation Lines inside the subchip (row $i=2$ and column $j=2$) of the Vector Matrix $V(8,3)$.
Left: Pairs of Permutation Lines indicating clearly locatable defects.
Right: Pairs of Permutation Lines indicating multiple defect positions.

Faults and defects will be detected inside the subchips. For that, customized layout elements will be designed inside the subchips that correspond to regular layouts used inside product chips (ref. Figures 5 and 6). So, defect statistics based on Checkerboard Test Structures represent the same problems that occur inside regular product chips. More than 90% of the total chip area is completely filled with these customized defect sensitive structures. So, there is a large defect sensitive area to detect random point defects even if the average defect density is low.

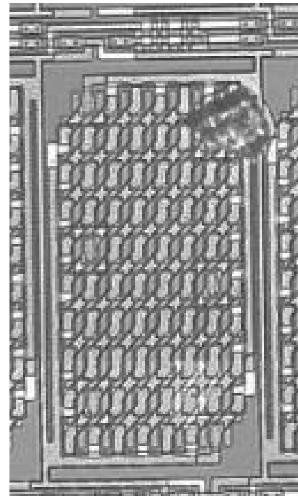

Fig. 5: Subchip containing customized layout elements in metal 1 and metal 2.

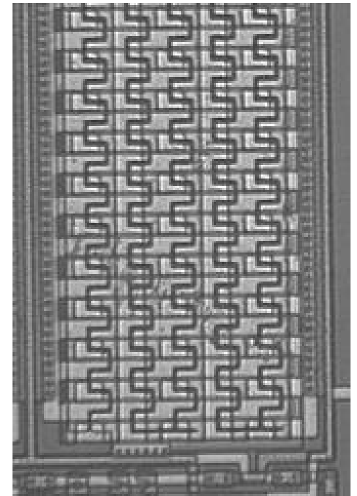

Fig. 6: Subchip containing customized layout elements in poly and metal 1.

In most cases, all subchips contain the same customized layout design. It is also possible to distribute different subchip layout designs within a single Checkerboard Test Structure. For that, all values of the Permutation Matrix will be divided into subsets. Then, the same subchip design will be included in those subchips of which its two Permutation Lines either belong to the same subset or belong to the same pair of subsets. Within the example Checkerboard Test Structure of the following Figure 7 two subsets (1,2,3,4) and (5,6,7,8) were created to include three different subchip designs "A", "B" and "C". The first design "A" will be implemented inside all

subchips where both Permutation Lines belong to the subset (1,2,3,4). The second design "B" will be implemented inside all subchips where both Permutation Lines belong to the subset (5,6,7,8). Finally, the third design "C" will be implemented inside all subchips where one Permutation Line belongs to the subset (1,2,3,4) while the other Permutation Line belongs to the subset (5,6,7,8). So, even if for instance systematic problems should result in faults inside all subchips containing the design "A", it remains still possible to analyze point defects within the subchips containing the design "B".

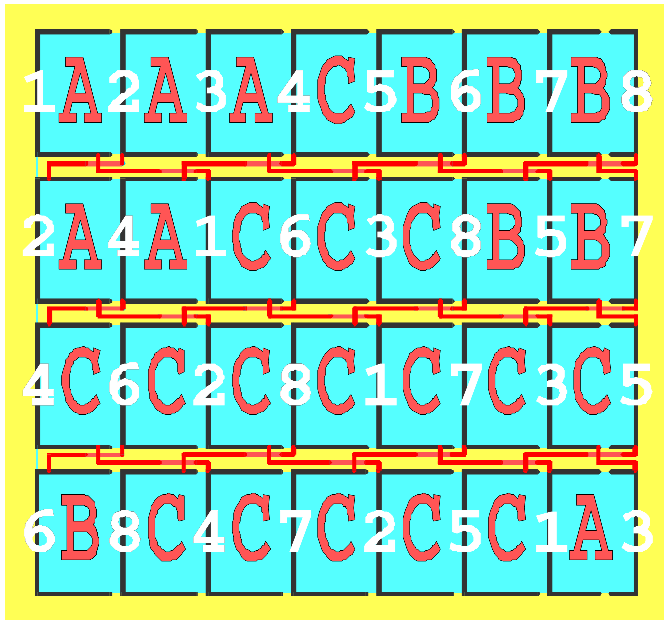

Fig. 7: Distribution of three different subchip designs "A", "B" and "C" within a Checkerboard Test Structure.

4 Measurements and Localization of Defects

Generally, short circuits are detectable, testing the resistance between different pads or Permutation Lines, respectively. To measure the resistance of the test structures, a digital tester will be used, because the electrical test must only decide whether there is a defect or not [HeWe95c]. The measured values are assigned to possible defects according to the following Table.

measured value		expected value in reference data	detected type of defect
voltage	binary		
$V_{measured} < V_{threshold}$	0	0	defectless
$V_{measured} < V_{threshold}$	1	0	short circuit

Tab. 2: Conversion of measured data (ref. [HeWe95d]).

If a defect occurs, two or more Permutation Lines inside the test structure are connected to each other. The defect will be localized inside a Checkerboard Test Structure because each pair *(p,q)* of Permutation Lines can be clearly assigned to a unique subchip in row *i* and column *j* inside the Vector Matrix. For that, all conducting layers of a Checkerboard Test Structure will be consecutively numbered, starting with the index value "1" for the lowest layer. So, the top layer will be given the index value "*n*". Due to the implementation of each Permutation Line in one layer *L* only, the indices of Permutation Lines range from $(L-1)\cdot m+1$ to $L\cdot m$, where *m* stands for the total number of values inside the Permutation Matrix. So, all fail value pairs *(p,q)* will be localized inside a test chip using the flow charts of Figure 8 and 9 where the equations of Table 3 occur. The gray shaded box in Figure 8 refers to the defects between the Permutation Lines indicated in the right neighborhood graph of Figure 4.

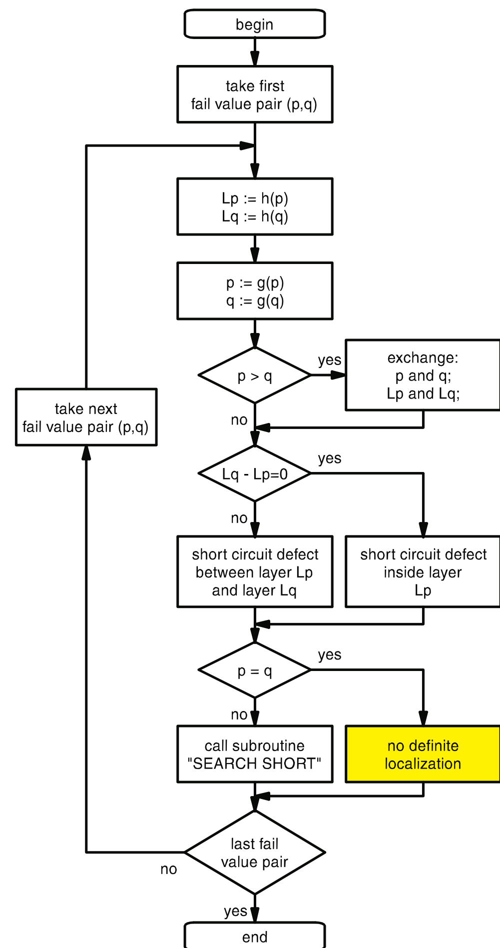

Fig. 8: Procedure to localize defects that results in electrically detectable faults.

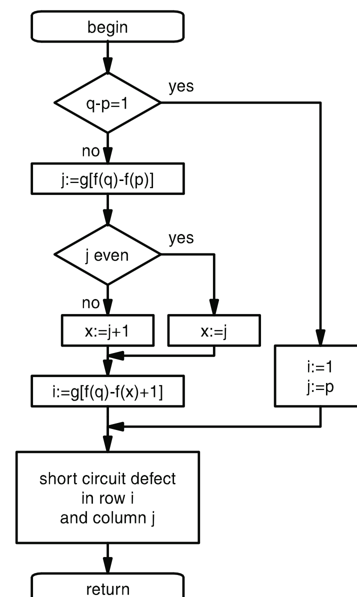

Fig. 9: Subroutine "SEARCH SHORT".

$$f(x) := \begin{cases} \frac{x}{2} & \text{if } \frac{x}{2} \in \mathbb{N} \wedge 1 < x \le m \\ m - \left[\frac{x-1}{2}\right] & \text{if } \frac{x-1}{2} \in \mathbb{N} \wedge 1 \le x < m \end{cases}$$	**(8)**
$$g(x) := \begin{cases} ((x-1) \bmod m)+1 & \text{if } x > 0 \\ (x \bmod m)+m & \text{if } x \le 0 \end{cases}$$	**(9)**
$h(x) := ((x-1) \operatorname{div} m)-1$	**(10)**

Tab. 3: Equations used in the localization flowcharts.

If more than just two lines are connected, the following procedure will help to disentangle these multiple connection faults.

1. All possible Permutation Line index pairs *(p,q)* will be extracted from the set of *k* connected pads.
2. The localization index *(i,j)* will be determined for each pair *(p,q)* of Permutation Lines using the flowcharts of Figure 8 and Figure 9.
3. Then, bundles of Permutation Lines will be determined by combining those pairs $(p,q)_1$ and $(p,q)_2$ that have a common pad index and their localization indices meet:

$$(i_1 = i_2 \wedge |j_1 - j_2| = 1) \vee (|i_1 - i_2| = 1 \wedge j_1 = j_2) \quad \mathbf{(11)}$$

4. Finally, we select the smallest number *d* of bundles containing the indices of all *k* connected pads. So, *d* represents the minimum number of defects that have caused the measured multiple fault.

The following Figure 10 shows a Checkerboard Test Structure based on 24 pads per layer containing a measured short circuit between *k=3* pads (indices: 5,16,18).

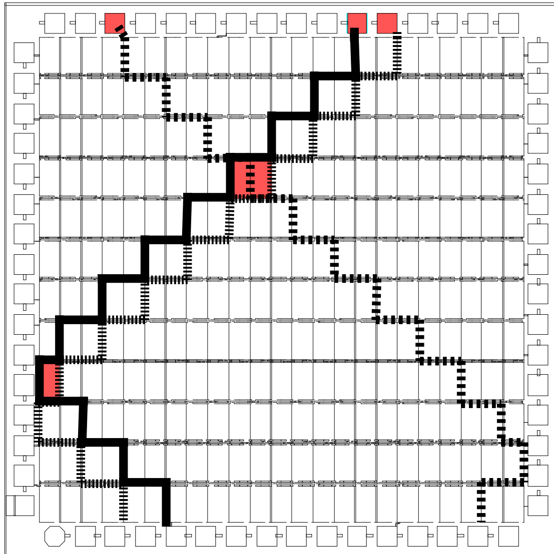

Fig. 10: Checkerboard Test Structure containing a defect connecting 3 adjacent Permutation Lines.

So, there are three possible Permutation Line index pairs (5,16), (5,18) and (16,18). Only the pairs (5,16) and (5,18) are adjacently placed as neighbors in subchip row 4 and may be combined in a bundle that holds the pad indices (5,16,18). In this case, there is only one bundle that contains all connected pads (*d=1*). The majority of all faults that connect more than just two pads may be summarized in just one "large" bundle.

5 Experimental Results

At ELMOS in Dortmund, Germany, two customized Checkerboard Test Structures were manufactured to control defect appearance inside the interconnection process. Each test structure has 276 distinguishable subchips containing layout elements also used in regular product chips. The subchips of the Checkerboard Test Structure **CTS1** contain layout elements in metal 1 and metal 2 (ref. Fig. 5). The subchips of the Checkerboard Test Structure **CTS2** contain layout elements in poly and metal 1 (ref. Fig. 6). A manufactured wafer holds 109 Checkerboard Test Structures CTS1 and CTS2 each. All in all, a lot "A" of 23 wafers and a lot "B" of 25 wafers were manufactured. So, **10,464 test chips** were analyzed using digital tester based measurements followed by the defect detection and localization procedure.

Figure 11 and Figure 12 show the defect density distribution dependent on the interconnection layer. The defect density is almost the same in each layer, which indicates well-selected design rules, except some problems during the manufacturing of poly in lot "B". The localization of all defects enables efficient collection of images to determine defect size distributions as can be seen in Figure 13. Figures 14 and 15 show some detected defects inside the different subchip designs inside the Checkerboard Test Structures.

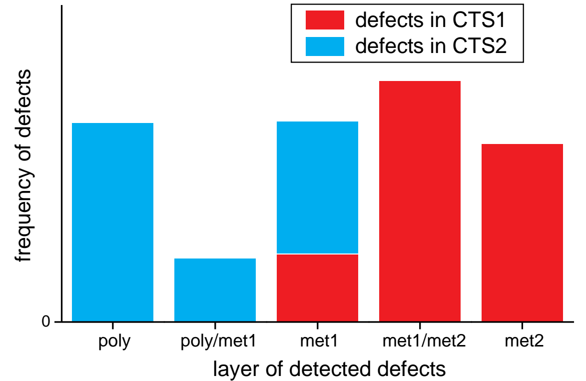

Fig. 11: Defect density distribution per layer in lot "A".

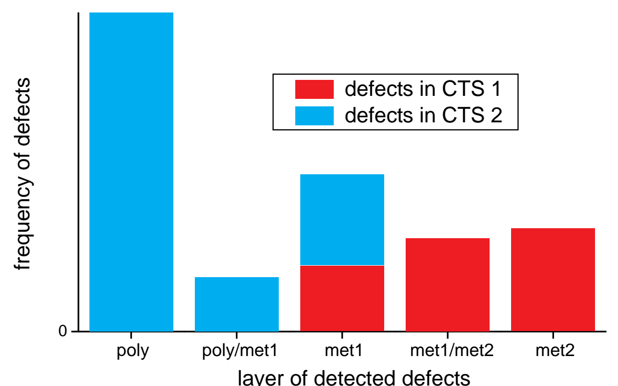

Fig. 12: Defect density distribution per layer in lot "B".

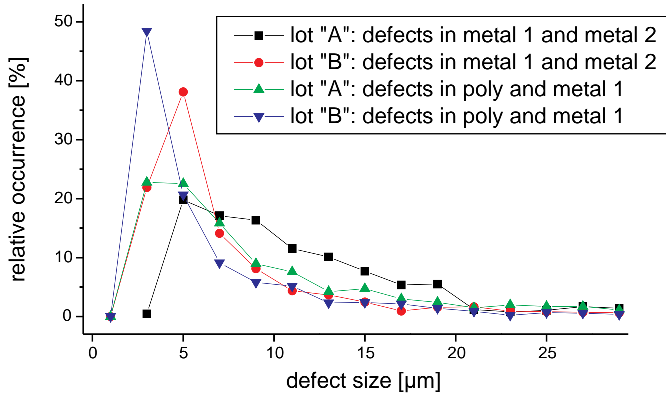

Fig. 13: Defect size distributions in lot "A" and "B".

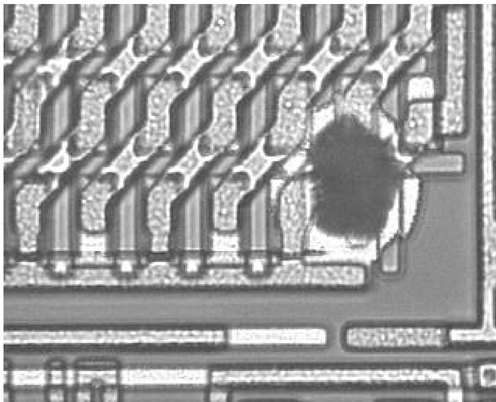

Fig. 14: Detected defect in a customized subchip containing layout elements in metal 1 and metal 2 (CTS1).

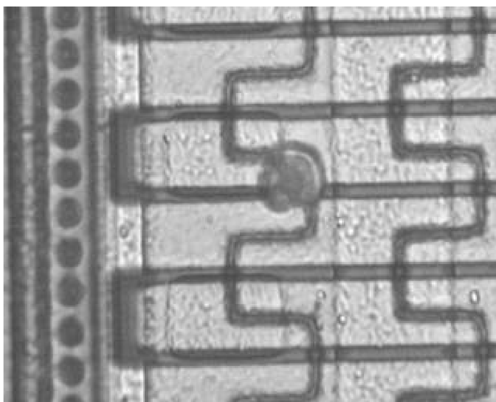

Fig. 15: Detected defect in a customized subchip containing layout elements in poly and metal 1 (CTS2).

All electrically detected short circuits were optically inspected. The following table gives the percentage of visible defects and not visible defects.

lot	layer	visible	not visible
A	metal 1	94 %	6 %
A	intermetal	22 %	78 %
A	metal 2	96 %	4 %
B	metal 1	81 %	19 %
B	intermetal	57 %	43 %
B	metal 2	78 %	22 %

Tab. 4: Percentage of visible defects.

6 Conclusion

Test structures are used to get data about defects in interconnection layers. If these data should correspond to measured yield of product chips it is highly recommended to design test structures that partly contain real circuit designs of product chips. The described method to design Checkerboard Test Structures enables the implementation of real circuit designs inside numerous subchips. The Checkerboard Test Structure detects systematic problems as well as random defects due to its extensive defect sensitive area. However, the permutation of test structure lines guarantees the separation of digitally measured single and multiple faults as well as a layer specific localization of defects inside the subchips even if the number of boundary pads is limited. The systematical design of the Checkerboard Test Structure enables a machine-assisted generation of test chips within seconds. There is no limitation to the number of layers and no requirement of any active semiconductor devices to separate Permutation Lines or disentangle multiple faults, respectively.

Acknowledgment

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