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Defect Cluster Analysis to Detect Equipment Specific Yield Loss Based on Yield-to-Area Calculations

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ABSTRACT

Defect parameter extraction plays an important role in process control and yield prediction. A methodology of evaluating wafer level defect clustering will be presented to detect equipment specific particle contamination. For that, imaginary wafermaps of a variety of different chip areas are generated to calculate a yield-to-area dependency. Based on these calculations a Micro Density Distribution (MDD) will be determined for each wafer. The range and course of the MDD may indicate specific failures of equipment tools.

Keywords: IC manufacturing, process control, test structure, defect density distribution, laser scattering, particle defect, yield, cluster analysis

1 INTRODUCTION

Today's complexity of integrated circuits requires more and more conducting backend layers to connect all circuit cells and devices. Undesigned layout objects (**defects**) can occur during the manufacturing process. Dependent on the layout, defects can become the cause of electrically measurable **faults** which are responsible for manufacturing related malfunctions of chips. Particle contamination generated by manufacturing equipment is the main cause for yield loss. Clustered defects indicate problems in specific process steps mainly caused by just one equipment tool. So, defect density distributions and defect cluster analysis are important for yield prediction and to control quality of process steps and product chips.

The following two procedures are used to detect and localize particles, defects and faults. First, **optical in-line defect inspection** using digital image processing tools and laser scattering techniques will detect particles, but it is difficult to get an accurate defect-to-yield correlation [FiDa90], [TrBG95], [CGLW96].

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Second, a **post process fault analysis** extracts killer defects inside test structures or product chips containing repeating geometries, respectively [HeSt94], [ChSz96], [HeWe96a], [LMLW96]. But, detection and localization of defects are difficult and take a lot of time.

To detect equipment problems, it should be sufficient to investigate the degree of defect clustering on a wafer. If this could be done just analyzing the distribution of relative defect densities, even optical inspection systems may be used, because their defect-to-yield correlation problem only applies to absolute defect densities. For that, this paper presents a methodology to evaluate clustering of defects by determining and analyzing wafer level defect density distributions. Section 2 will describe our procedures to collect defect data based on optical and electrical measurements. In Section 3 an imaginary yield calculation will be presented to provide yield-to-area curves. Section 4 gives guidelines how to evaluate defect clusters. In Section 5 we present some experimental results and finally we conclude our approach.

2 COLLECTION OF DEFECT DATA

Defect data have to be collected using different measurement techniques to get a methodology to indicate clustered defects that is independent of the procedure to detect defects. Here we used laser scattering tools as well as electrical measurement at test structures.

2.1 Optical Measurements

Using a laser scattering tool like a Tencor Surfscan 7600 enables the optical in-line detection of yield limiting defects. These tools can be used on bare wafers as well as on patterned wafers. After a complete wafer scan the system yields an event list containing the approximate defect size, the absolute defect position on the wafer and the intensity of the reflected laser beam.

2.2 Electrical Measurements

To get defect statistics, simple test structures of comb and serpentine lines are commonly used [Bueh83], [LYWM86]. But, simple test structures do not provide any defect localization inside large chip areas. Only a precise defect localization inside the chip area will enable the investigation how many electrical faults were also detected by surfscan measurement procedures and vers versa. Furthermore, the localization also simplifies the optical determination of defect parameters like size and outline as well as the mechanisms how a defect results from a specific process step. So, especially designed test structures to control process steps for polysilicon and metal layers are on demand. Two major methods to organize test chips are known, the "2 by N" probe-pad array [Bueh79] and standard boundary pads. To detect random point defects, the defect sensitive area inside a "2 by N" array is relatively small so that the large sensitive area inside the boundary pads seems to be more suitable. But here the number of pads is relatively small so that methods are required to separate and localize defects.

An undesigned short circuit defect is only detectable between test structure layout elements connected to electrically distinguishable pads. For that, all test structure layout objects that are connected to one single pad are called a **Permutation Line**. To increase the number of separable short circuits without increasing the number P of pads, all possible $\frac{1}{2} \cdot P \cdot (P-1)$ neighborhood relationships of Permutation Lines

have to be arranged inside a test chip. To also localize these short circuits, each neighborhood relationship has to be implemented exactly once inside the test chip area. For that, each Permutation Line has to be adjacent to every other Permutation Line just once. The **Permutation Procedure** introduced in [HeSt94] arranges all pairs of Permutation Lines without crossing each other in the rows of a **Permutation Matrix** so that each pair of Permutation Lines exists once for *m* different index values.

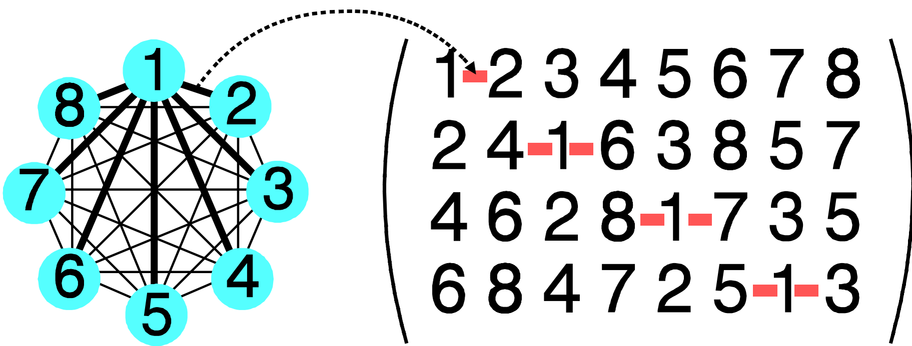


Fig. 1: Example of the Permutation Procedure for *m=8* values.
Left: Complete neighborhood graph introduced by [HeWe94]:
node: Permutation Line connected to one pad.
edge: Two nodes are connected by an edge if the Permutation Lines connected to these pads are adjacently placed anywhere inside a test chip with only nonconducting material between them.
Right: Permutation Matrix, where the gray boxes mark pairs to line "1".

The following equation will be used to calculate the elements *a[i,j]* of the Permutation Matrix, where the number *m* of used index values has to be even.

$$a[i,j] := \begin{cases} j+2\cdot i-2 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i \le \frac{m-j+2}{2} \\ 2\cdot m-j-2\cdot i+3 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i > \frac{m-j+2}{2} \\ 2\cdot i-j-1 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i > \frac{j+1}{2} \\ j-2\cdot i+2 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i \le \frac{j+1}{2} \end{cases} \qquad \textbf{(1)}$$

i : row index of the Permutation Matrix
j : column index of the Permutation Matrix

Now, the Permutation Procedure will be transferred into a test structure design. An obvious approach to the separation and localization of defects is to partition the chip area into a large number of subchips, each containing one pair of Permutation Lines. So, each value of the Permutation Matrix will be replaced by a vertical line generating rectangular subchips. The following Figure 2 shows the frame of such a checkered arrangement of subchips which is called a **Checkerboard Test Structure (CTS)**. At the boundary of each subchip there is a unique set of Permutation Lines that are all connected to different pads. Here, for example, all Permutation Lines connected to two pads are highlighted. Both lines are neighbored in one subchip only (row 15 and column 14), which is the key to the defect localization facility.

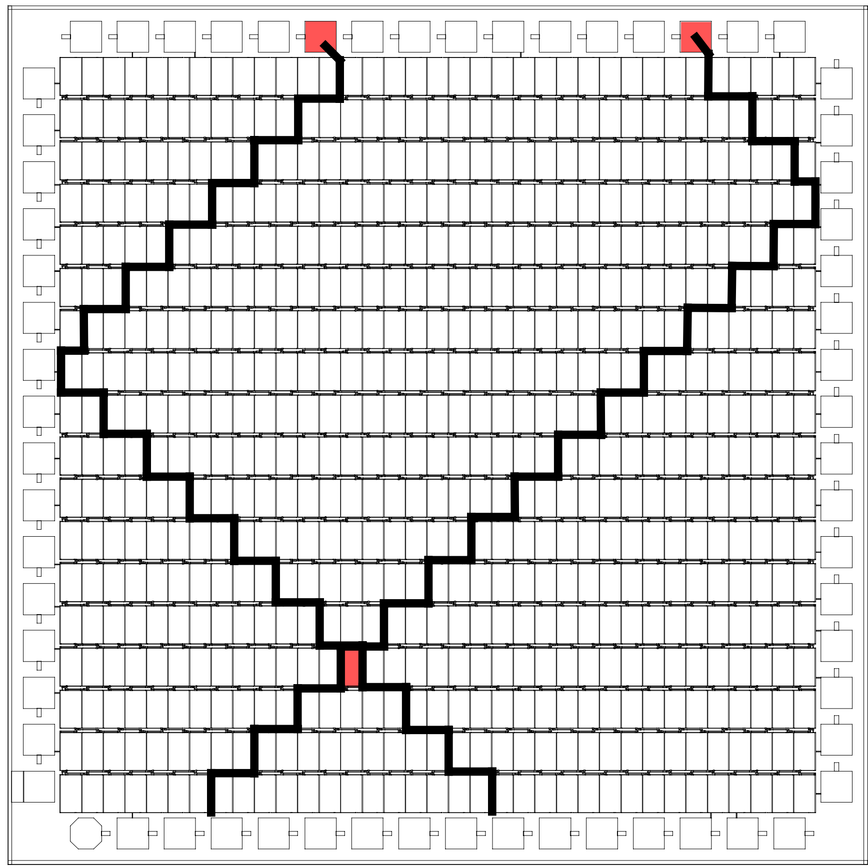


Fig. 2: Automatically generated Checkerboard Test Structure containing 630 subchips (k=1, p=36).

The principle described above will be individually done per layer and finally all single layer frame designs will be arranged one above another. So, the total chip area of a Checkerboard Test Structure will be divided into a large number *n* of electrically distinguishable subchips.

$$n := \frac{p}{2 \cdot k} \cdot \left(\frac{p}{k} - 1 \right) \quad \textbf{(2)}$$

n : number of subchips
p : number of pads
k : number of conducting layers

The Checkerboard Test Structure detects systematic problems as well as random defects due to its extensive defect sensitive area. The systematical design of the Checkerboard Test Structure enables a machine-assisted generation of test chips. There is no limitation to the number of layers and no requirement of any active semiconductor devices to separate test structure lines or disentangle multiple faults, respectively. Inside the subchips, customized layout designs will be placed to detect the defects. If a short circuit occurs, two or more test structure lines are connected. Since we know in which subchips these specific lines are neighbored we can conclude to the subchip that contains the defect. So it is possible to determine an event list of electrically detected defects including their precise location on the wafer. Localization procedures are described in [HeSt94], [HeWB97a] that also indicates the layer of each defect.

3 IMAGINARY YIELD CALCULATION

Uniformly distributed particles result in a defect density which is constant throughout the wafer. In reality particles are not uniformly distributed building clusters of defects. For two wafers with the same average defect density, the more defects are clustered the higher the yield will be [Murp64], [StRo95]. If we have for example a wafer of 100 chips and 25 uniformly distributed defects, we will have approximately 75 chips having 0 defects and 25 chips having 1 defect. If the 25 defects are clustered, we get more than 75 chips having 0 defects, because there will also be some chips having 2, 3, and even more defects.

Our intention is to indicate clustered defects by imaginarily varying the chip area of a wafermap containing detected defects. Then the yield will be determined dependent on the chip area. For that, an imaginary wafermap will be generated based on a given chip area ($dx \cdot dy$) and the original wafer diameter (d). First, a chip array with $col=d/dx$ columns and $row=d/dy$ rows has to be calculated. The center of this chip array ($x_0=(col \cdot dx)/2$, $y_0=(row \cdot dy)/2$) will be placed into the center of the wafer. Now, all chips have to be faded out totally or partly lying outside the wafer boundary. Going through an optical or electrical event list each chip can be marked as pass or fail dependent on the absolute position of a defect. If an imaginary chip area does not contain any defects it will be defined as **pass chip**. If an imaginary chip area contains at least one defect it will be defined as **fail chip**. Then the yield Y will be determined by the following equation.

$$Y = \frac{\text{number of pass chips}}{\text{total number of chips}} \qquad \textbf{(3)}$$

Table 1 shows the generation of imaginary wafermaps and the yield calculations for 6 different chip areas. The chips of wafermap number 3 are similar to the original chip area. The procedure using imaginary wafermaps results in curves that describe the yield (y-axis) dependent on the chip area (x-axis) as can be seen in the following Figure.

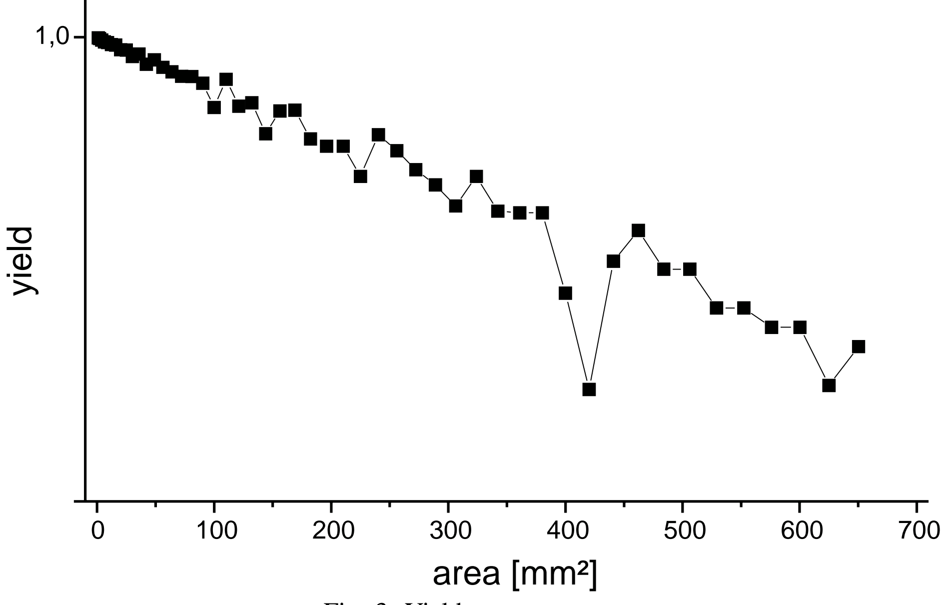
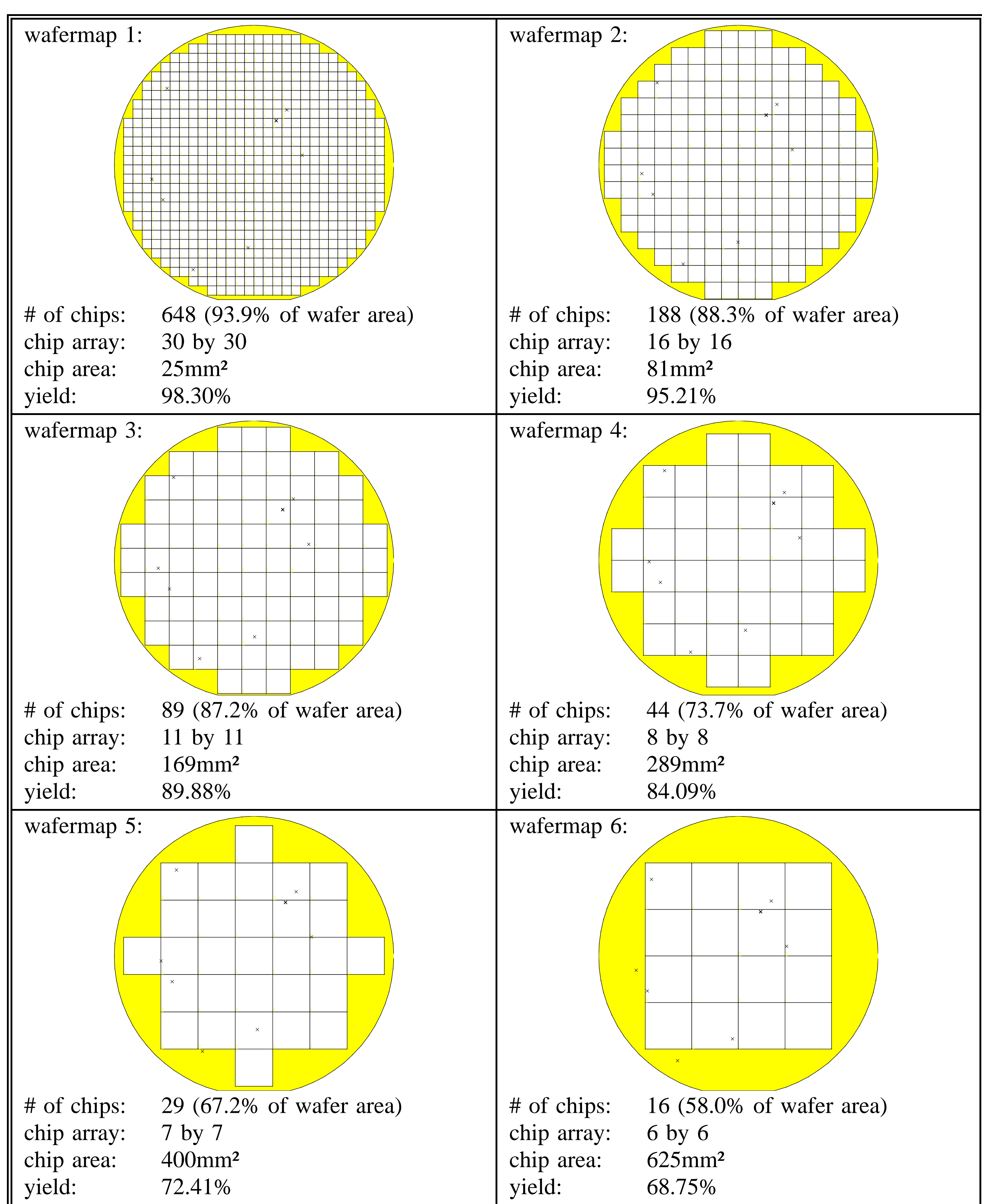


Fig. 3: Yield-to-area curve.



wafermap 1: # of chips: 648 (93.9% of wafer area) chip array: 30 by 30 chip area: 25mm² yield: 98.30%	wafermap 2: # of chips: 188 (88.3% of wafer area) chip array: 16 by 16 chip area: 81mm² yield: 95.21%
wafermap 3: # of chips: 89 (87.2% of wafer area) chip array: 11 by 11 chip area: 169mm² yield: 89.88%	wafermap 4: # of chips: 44 (73.7% of wafer area) chip array: 8 by 8 chip area: 289mm² yield: 84.09%
wafermap 5: # of chips: 29 (67.2% of wafer area) chip array: 7 by 7 chip area: 400mm² yield: 72.41%	wafermap 6: # of chips: 16 (58.0% of wafer area) chip array: 6 by 6 chip area: 625mm² yield: 68.75%

Table 1: Generated imaginary wafermaps for 6 different chip areas.

4 CLUSTER EVALUATION

The procedure to determine yield-to-area curves will now be used to evaluate defect clustering. For that, we first have to model yield-to-area curves for unclustered defects within a uniform distribution. Then we will compare these results to clustered defect distributions that occur in reality.

4.1 Uniform Distribution of Defects

A software tool was developed to generate an event list of uniformly distributed defects. The following Figure gives yield-to-area curves for different defect densities.

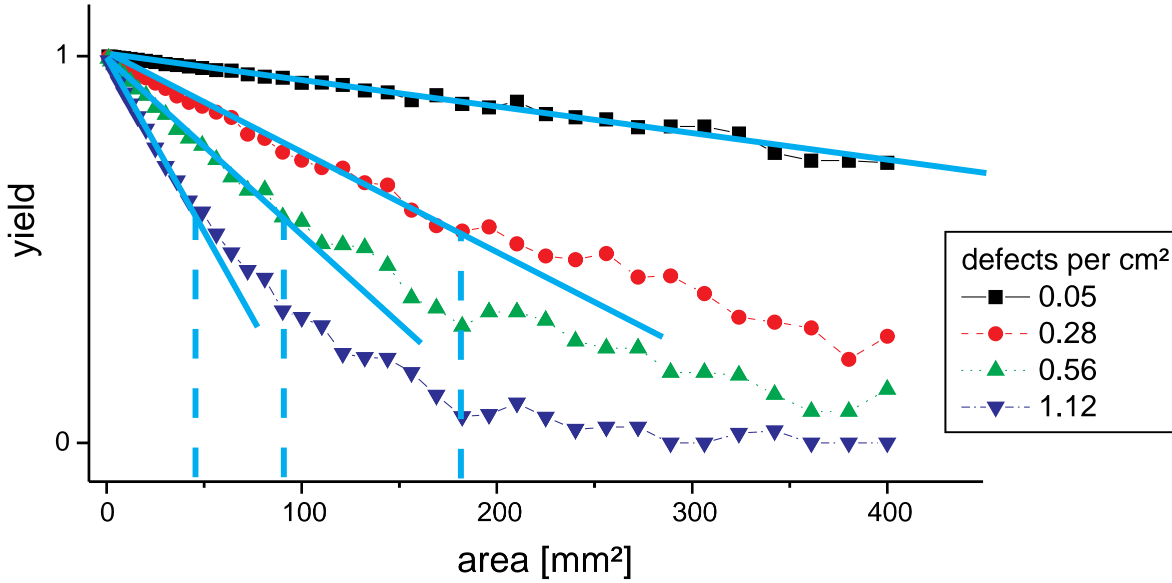


Fig. 4: Yield-to-area curves of uniformly distributed defects.

If the chip area is small enough, the yield-to-area curves may be linearly modeled. The linearly modeling also depends on the defect density, because most of the defective chips should not contain more than one defect. But, Figure 4 clearly shows that even for uniformly distributed defects this will only be provided for the following approximation:

$$A \cdot D < 0.5 \quad \textbf{(4)}$$

A : chip area
D : defect density

Now we have to investigate how clustered defects will change the course of the linear part of the yield-to-area curve.

4.2 Clustered Defects

Regarding the defects within the wafermaps of Table 1 it is obvious that there are clustered defects in the upper right area and the lower left area. As expected the yield-to-area curve of Figure 3 oscillates and may not be modeled with just a straight line. Nevertheless, the area and the defect density meet approximation (4).

4.3 Micro Density Distributions (MDD) of Defects

Each equipment tool of a process step contributes just a few defects to the final defect map on a wafer after passing many process steps. Koren et al. have analyzed defect maps of 57 wafers. Each defect map was clustered, but they could not indicate any correlation between defect maps of different wafers [KoKS94]. Nevertheless, the degree of defect clustering on a single wafer should be sufficient to detect a specific failure of an equipment tool. Such a failure results in an unexpected increase of defect density, which significantly changes the final defect map. So, we want to indicate such specific failures of equipment tools analyzing yield-to-area curves as one can be seen in Figure 5.

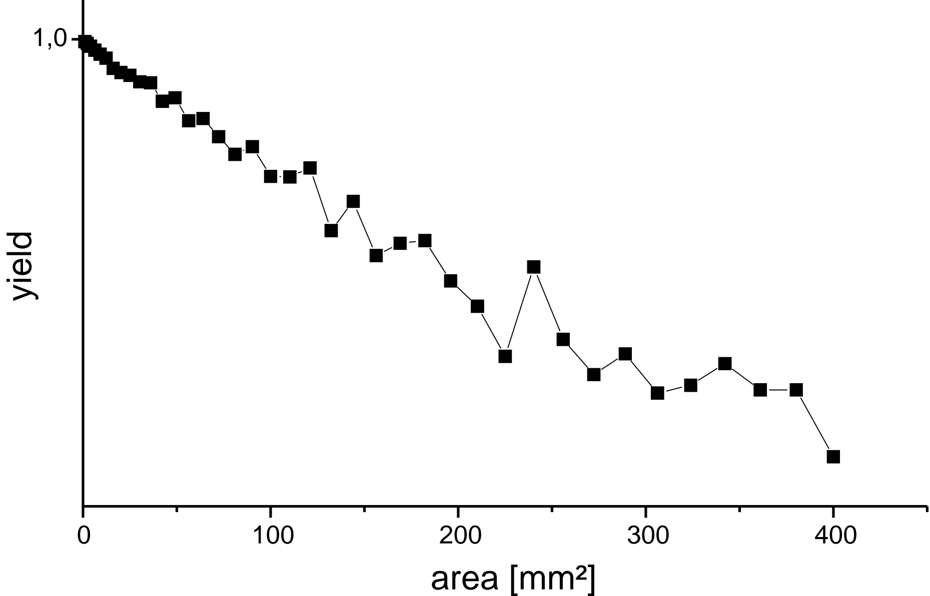


Fig. 5: Yield-to-area curve of electrically detected defects on a wafer.

To measure the intensity of the oscillation of the yield-to-area curve, we determine the **Micro Density Distribution (MDD)** of defects. For each yield value *Y* of the yield-to-area curve the defect density *D* may be calculated dependent on the chip area *A*.

$$D = \frac{1 - Y}{A} \qquad \textbf{(5)}$$

This calculation bases on the assumption that a fail chip contains no more than 1 defect. For that, the average defect density $\bar{D}_n$ of *n* calculated values D_i has to be within the limits of approximation (4).

$$A_n \cdot \bar{D}_n < 0.5 \qquad \text{where:} \quad \bar{D}_n = \frac{1}{n} \sum_{i=1}^{n} D_i \qquad \textbf{(6)}$$

A_n : chip area corresponding to defect density D_n

It is important to start calculating the defect density D_i within the yield-to-area curve for the smallest available chip area A_1 then the chip area has to be increased until approximation (6) will become false. Now it is possible to determine the Micro Density Distribution by counting the occurrence of defect density values per density interval which can be seen in the following Figure 6. To get comparable defect density distributions within different layers on a wafer, we use the probability density of defects

by normalizing the curve which means that the sum of all occurrence values has to be set to "1". In addition to that, we also determine the overall defect density on a wafer as the total number of defects on a wafer divided by the total area of the wafer. Figure 6 contains this value as additional small vertical peak.

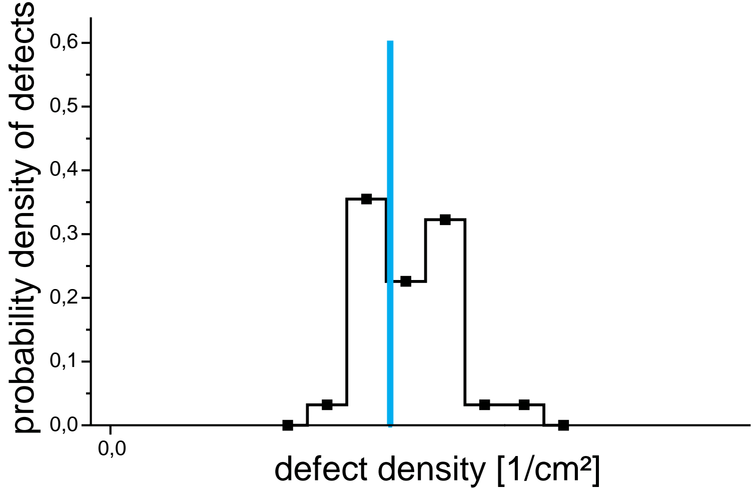


Fig. 6: Micro Density Distribution of electrically detected defects on a wafer.

Now the course of the Micro Density Distribution will be evaluated to detect specific failures of equipment tools. There are two characteristic MDD courses. Clustered defects launched by many equipment tools result in a wide MDD having many different defect density intervals. If one specific process step is mainly responsible for defect clustering, we get a MDD having peaks in nonconsecutive intervals which then will be called an irregular MDD.

5 EXPERIMENTAL RESULTS

At Thesys Gesellschaft für Mikroelektronik mbH in Erfurt Germany, a Checkerboard Test Structure (CTS) was designed to control defect appearance inside the interconnection layers "metal-1" and "metal-2" of a single poly, double metal 1.5µm HCMOS 6-inch p-well process. The CTS has 72 Permutation Lines (36 lines per interconnection metal layer). The CTS was designed on top of the gate array THA10075 which consists of 37485 gates (299880 transistors) on a chip area of 11.7mm x 11.7mm. All in all 630 distinguishable subchips with an active area of 100mm² contain serpentine lines, via and contact strings. In addition to electrical measurements, Tencor 7600 based surfscan data were collected after processing metal-1, vias, and metal-2. The following Figures 7, 9, 11, and 13 show the yield-to-area curves of 4 inspected wafers. The Figures 8, 10, 12, and 14 give the probability density of defects for the same wafers. The vertical peaks represent the overall defect density within a layer on the wafer. The peak always is within the defect density distribution determined by the methodology described in Section 4.3.

Wafer 8 shows a wide Micro Density Distribution of metal-2 defects as well as a wide Micro Density Distribution of the electrically detected defects. Especially the irregular MDD of metal-2 indicates highly clustered defects. Detailed optical inspection using a microscope provides a defect classification that indicates some specific failures of equipment tools during processing of metal-2 which could not be observed on the other 3 wafers.

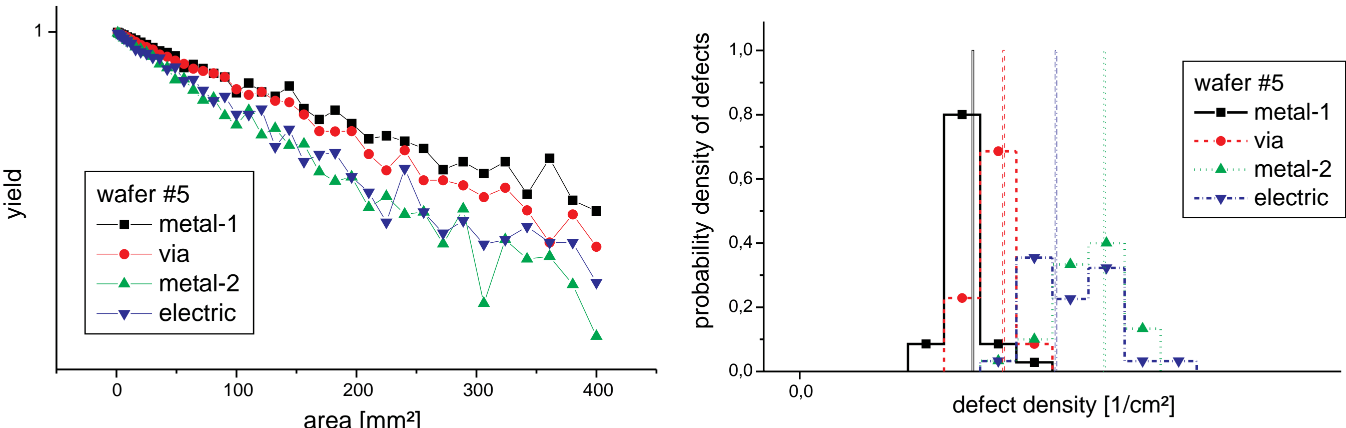


Fig. 7: Yield-to-area curve of optically and electrically detected defects on wafer 5.

Fig. 8: Micro Density Distribution of optically and electrically detected defects on wafer 5.

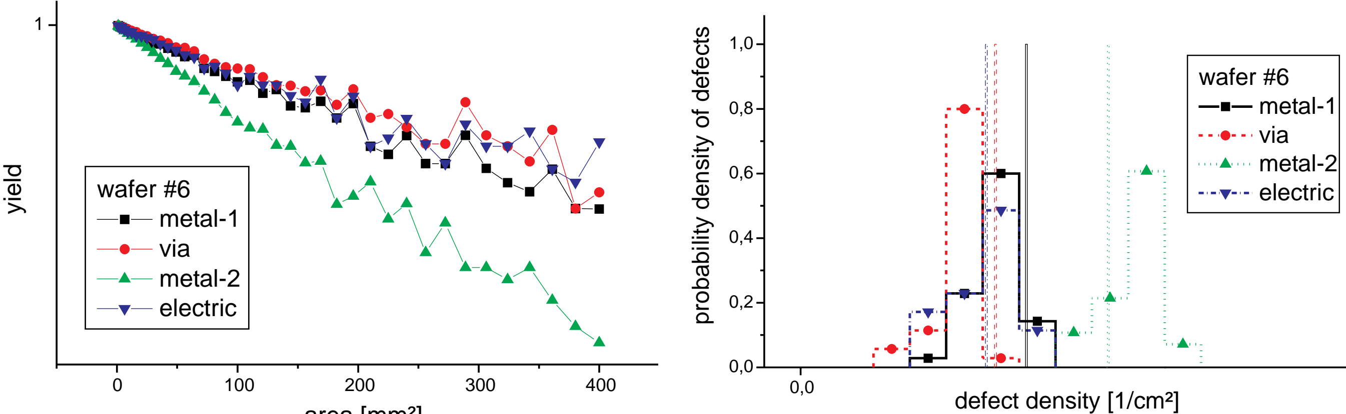


Fig. 9: Yield-to-area curve of optically and electrically detected defects on wafer 6.

Fig. 10: Micro Density Distribution of optically and electrically detected defects on wafer 6.

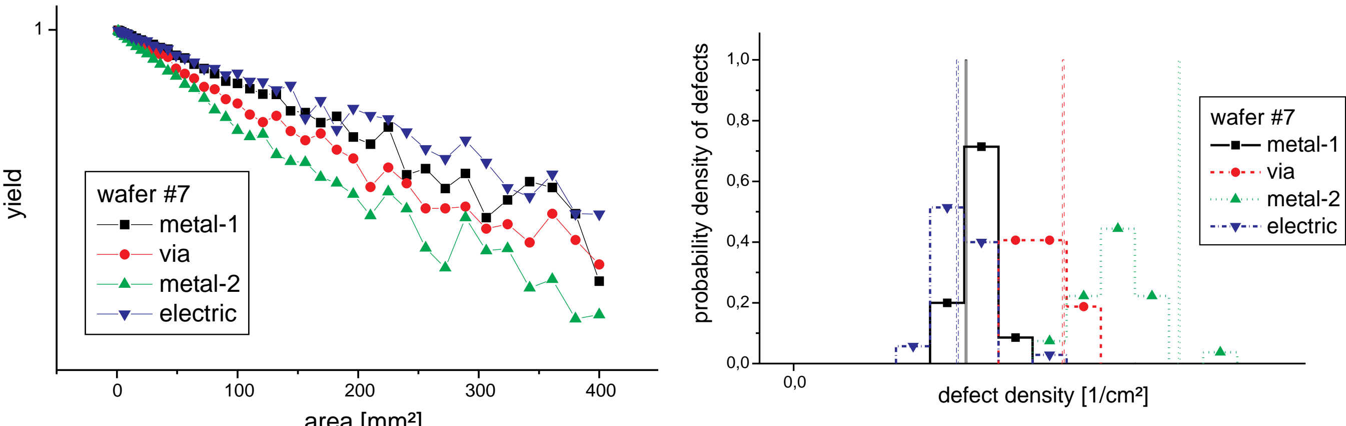


Fig. 11: Yield-to-area curve of optically and electrically detected defects on wafer 7.

Fig. 12: Micro Density Distribution of optically and electrically detected defects on wafer 7.

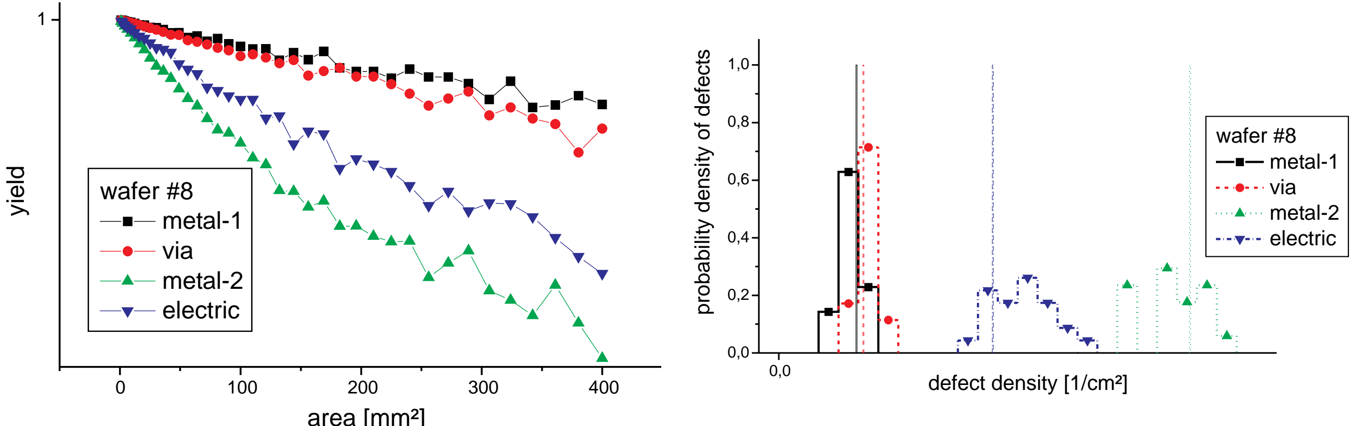


Fig. 13: Yield-to-area curve of optically and electrically detected defects on wafer 8.

Fig. 14: Micro Density Distribution of optically and electrically detected defects on wafer 8.

6 CONCLUSION

Instead of just one overall defect density value per wafer we presented a methodology to provide individual defect density distribution per wafer to evaluate wafer specific clustering of defects. The degree of clustering will be represented by the range of the Micro Density Distribution (MDD). The more different defect density values occur within the density distribution, the more clustered defects will be found on the wafer.

To enable this methodology, data about defects are required that include the layer and the position of each detected defect. So, optical detection systems are used after selected process steps to provide position specific defect data. In addition to that, a Checkerboard Test Structure enables precise localization of defects detected by electrical measurements only. Our investigation results that irregular distributions may be used to identify specific failures of equipment tools.

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