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Correlation between Particle Defects and Electrical Faults determined with Laser Scattering Systems and Digital Measurements on Checkerboard Test Structures

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ABSTRACT

To improve accuracy of defect densities, yield prediction and failure analysis, this paper compares data on defects and faults collected by electrical measurement methods and laser scattering systems. For that we choose the checkerboard test structure design to partition the whole chip area into a large number of subchips, each containing defect sensitive comb lines. A digital tester based measurement procedure enables the detection and separation of faults. Additional analysis procedures guarantee a layer-specific fault localization inside specific subchips. Manufacturing of test chips at *Thesys Gesellschaft für Mikroelektronik* was accompanied by laser scattering after selected processed layers. Finally, wafermaps based on electrically detected faults and optically detected particle defects were analyzed to determine correlations between defects and faults.

Keywords: IC manufacturing, process control, metallization, test structures, defect parameter extraction, defect statistics, laser scattering, particle defects, yield prediction

1 INTRODUCTION

Decreasing time to market and faster scaling down of design rules yield to an aggressive development within the semiconductor industry. Dependent on the layout, particles (physical defects) can become the cause of electrically measurable faults (e. g. killer defects) which are responsible for manufacturing related malfunctions of chips. For smaller features the ability to extract accurate defect densities is crucial. Generally, the particle density will be determined using laser scattering systems on all product wafers after selected process steps [TBG95]. In addition to that especially designed wafers containing test chips will be used to control process integrity [Bren92].

Laser scattering systems have problems in detecting undesigned layout elements (pattern defects) caused by photolithographic errors. Furthermore not every detected particle results in an electrically measurable fault. Electrically measurable test structures detect faults only induced by defects inside the layout region of test chips. Furthermore there are defects that are to small to become an electrically measurable fault. So, test structure related yield and defect densities are difficult to transfer to product chip related yield and defect densities, especially if design rules are different.

To improve accuracy of defect densities, we decide to compare data on defects and faults collected by both measurement methods. The following Section 2 describes the design principle of the checkerboard test structure which enables a layer-sensitive localization of electrical faults. Section 3 deals with the electrical measurement procedure and the laser scattering measurement technique. Section 4 gives some correlations between both types of measured data. Finally Section 5 conclude our approach.

2 CHECKERBOARD TEST STRUCTURES

A special test structure is required to enable an efficient comparison between surfscan detected defects and electrically measurable faults. It should provide a *large defect sensitive areas* to detect defects even if the average defect density is low. A *layer sensitive defect separation* is required to assign electrically detected defects to a specific layer. Only a *precise defect localization* inside the chip area will enable the investigation how many electrical faults were also detected by surfscan measurement procedures and vers versa. Furthermore, the localization also simplifies the optical determination of defect parameters like size and outline as well as the mechanisms how a defect results from a specific process step.

Two major methods to organize test chips are known, the "2 by N" probe-pad array [Bueh79] and standard boundary pads. The defect sensitive area inside a "2 by N" array is relatively small so that the large sensitive area inside the boundary pads seems to be more suitable. But here the number of pads is relatively small so that methods are required to separate defects. Checkerboard test structures introduced by [Hess94], [HeSt94], [HeWe95b] combine the large defect sensitive area inside a given pad frame and a precise defect localization.

To detect short circuits, checkerboard test structures divide the total chip area into a large number **n** of electrically distinguishable subchips.

$$n := \frac{p}{2 \cdot k} \cdot \left(\frac{p}{k} - 1 \right) \quad \textbf{(1)}$$

n : number of subchips
p : number of pads
k : number of conducting layers

Each subchip contains a unique set of test structure lines which are connected to different pads. The following figure 1 shows the frame of a designed checkerboard test structure. Here, for example all test structure lines connected to two pads are highlighted. Both lines are neighbored in one subchip only.

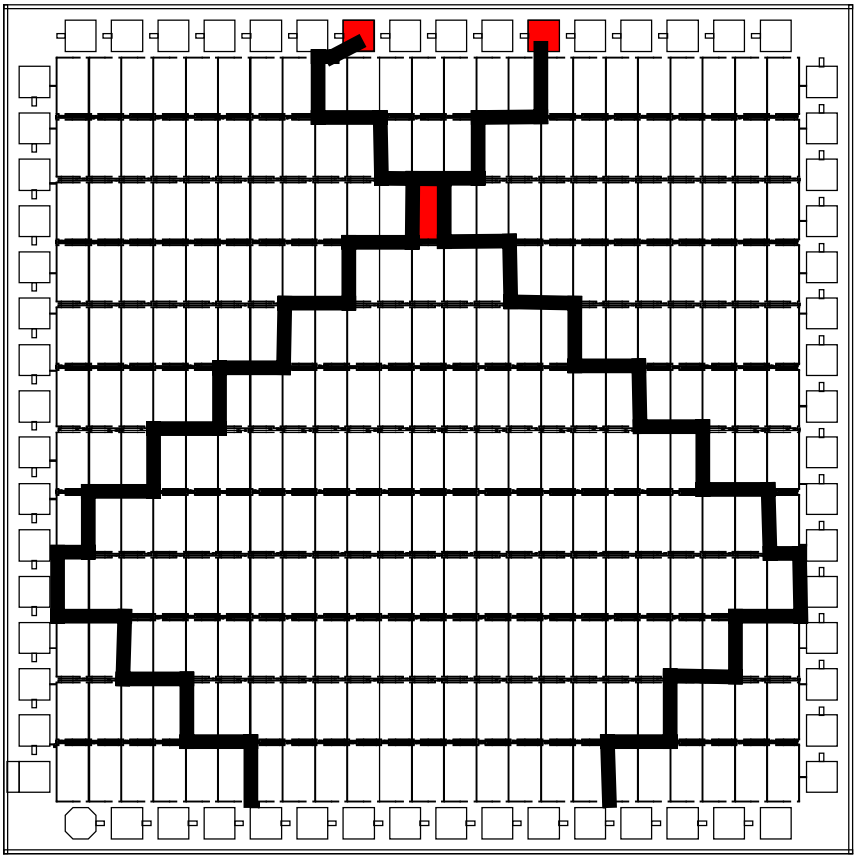

Fig. 1: Checkerboard test structure with 276 subchips, each containing a set of 4 distinguishable test structure lines.

If a short circuit occurs, two or more test structure lines are connected. Since we know in which subchips these specific lines are neighbored we can conclude to the subchip that contains the defect. Precise localization procedures are described in [HeSt94], [HWLS96] that also handle multiple shorts.

In addition to that, open circuits will be detected if a diode matrix will be combined with the design of the checkerboard test structure [HeWe94a], [HWLS96]. In this case, the number of subchips decreases to

$$n := \frac{p}{2 \cdot (k+1)} \cdot \left(\frac{p}{(k+1)} - 1 \right) \qquad \textbf{(2)}$$

If an open circuit occurs, the implemented connection of two pads is interrupted. Since we know in which subchip the implemented connection is placed we can conclude to the subchip that contains the defect. Again, precise localization procedures will be found in [HWLS96].

Faults and defects will be detected inside the subchips. So, comb lines, meandrous lines or via strings will be designed inside the subchips to detect different types of faults which are the result of process specific defects (ref. figure 2). They will be connected to the test structure lines placed at the border of each subchip.

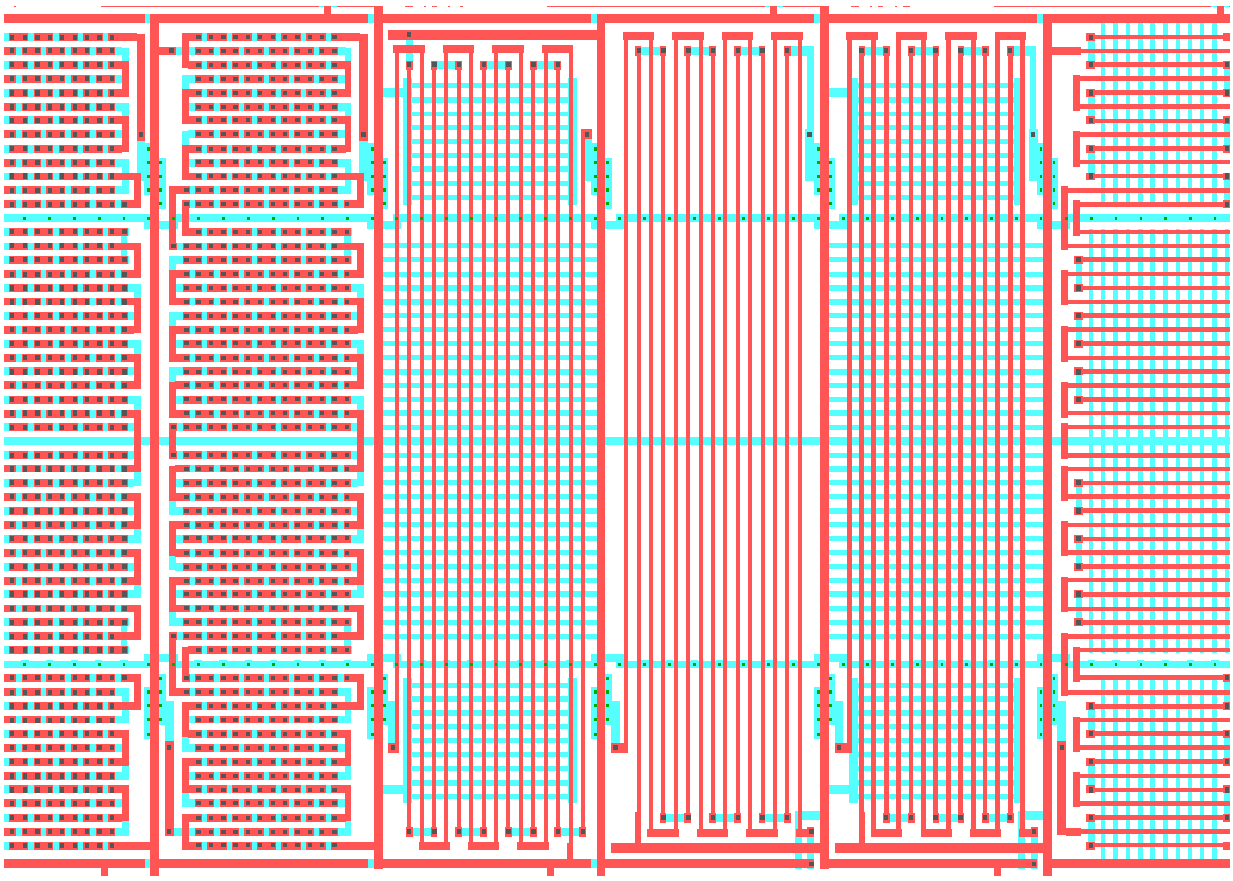

Fig. 2: Detail view of 5 subchips inside a checkerboard test structure.

Checkerboard test structures cannot only be used as a test chip to characterize wafer fabrication process resolution but also alongside with standard chips as a process control monitor. To measure the resistance of the test structures, a digital tester will be used, because the electrical test must only decide whether there is a defect or not. The measured values are assigned to possible defects according to [HeWe95d]. The use of a digital tester guaranties a measuring procedure without any additional measuring effort (equipment and time). The systematically designed checkerboard framework enables a machine-assisted generation of test chips without any limitation to the number of layers.

3 MEASUREMENT PROCEDURE

At Thesys Gesellschaft für Mikroelektronik mbH in Erfurt Germany, a checkerboard test structure was designed to control defect appearance inside the interconnection layers "metal-1" and "metal-2" of a single poly, double metal 1.5µm HCMOS 6-inch p-well process. The CTS has 72 test structure lines (36 lines per interconnection metal layer). The CTS was designed on top of the gate array THA10075 which consists of 37485 gates (299880 transistors) on a chip size of 11.7mm x 11.7mm. All in all 630 distinguishable subchips with an active area of 100mm² contain serpentine lines, via and contact strings. Figure 3 shows a part of the test chip layout. If a defect occurs and causes a fault, test structure lines are interrupted or connected to each other. Since we know in which subchips the test structure lines are implemented, we can conclude to the subchips containing the defects.

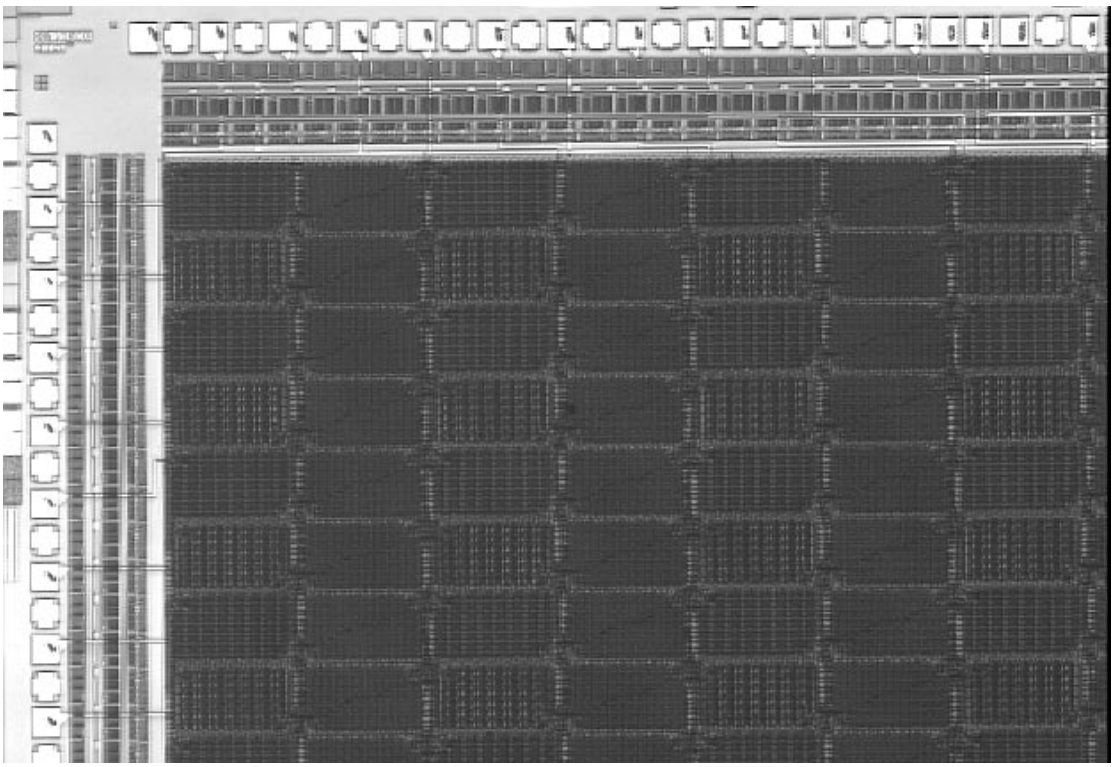

Fig. 3: Upper left Corner of a manufactured checkerboard test structure.

Two lots were manufactured, lot "A" containing six wafers and lot "B" containing four wafers. The electrical faults of all chips were determined using a digital tester followed by a defect detection and localization procedure [HeWe95d], [HWLS96]. All these algorithms including the generation of the golden device have been implemented in a program system called VIADUCT (**V**ersatile Automatic **I**dentification **A**nalysis of **D**efects from **U**ndesigned Open and Short **C**ircuits in **T**est Structures). VIADUCT generates an *event list* of all detected faults. This binary data file provides the absolute position on the wafer of each fault inside a subchip, the layer of each fault, and some information according to the designed test structure lines inside the defective subchip.

The surfscan measurements were performed using a Tencor SFS 7600 measuring system. A surfscan defect detection of all wafers of lot "A" was done after processing the metal-1 layer only (level-ID: D22). The wafers of lot "B" were inspected six times according to the following table.

level ID	Inspection after manufacturing process step
K33	contacts
D22	metal-1
C03	vias
R23	metal-2 (before etching)
R01	metal-2 (after etching)
E03	glass

Tab. 1: Surfscan inspection of lot "B".

The Tencor system provides a binary data file of all detected defects per wafer, also called an *event list*. Each event will be described with its absolute position on the wafer, the intensity of the reflected laser beam, and the estimated size of the defect. A novel program called VIASTAT now enables the comparison of both event lists. To enable a realistic comparison of both measurement techniques, only those surfscan defects were taken into account that are placed inside the defect-sensitive array of subchips. This area is about 73% of each checkerboard test structure chip area. The remaining 27% of the total chip area is covered by the pads and the sawing lines. The following figure shows the percentage of surfscan defects, which are outside the subchip arrays.

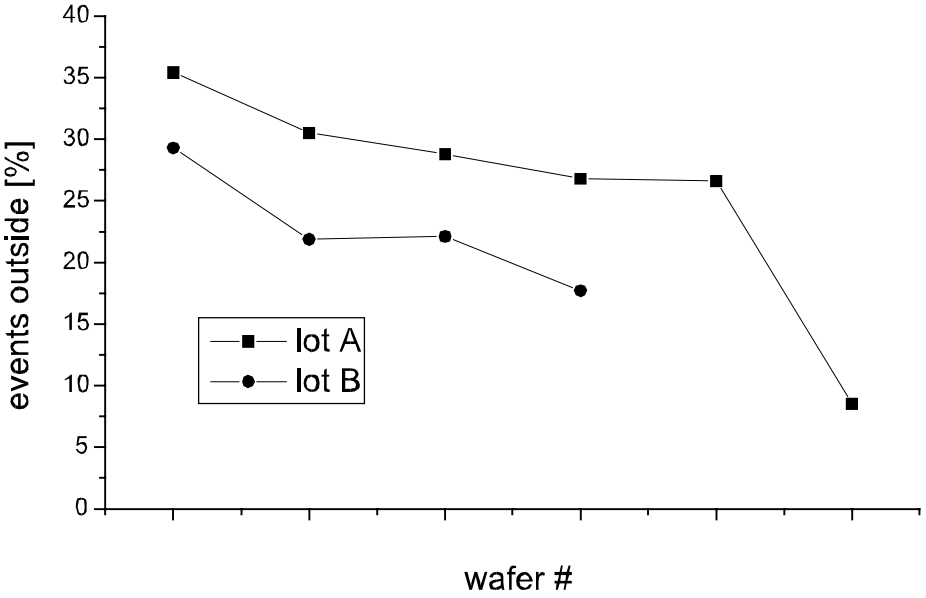

Fig. 4: Percentage of detected surfscan defects outside the defect-sensitive area of the checkerboard test structure.

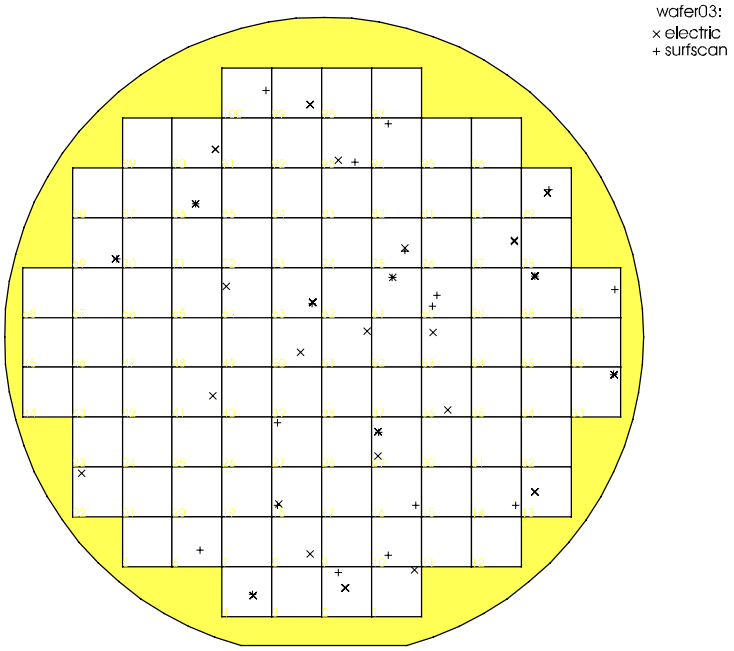

Fig. 5: Detected surfscan defects and electrical faults on wafer "03".

Now it is possible to compare the position of the detected surfscan events with the position of the electrical events inside the subchips. The following four figures get a general idea of the matching of both types of events. In the wafermaps, each electrically detected fault is marked by a "X" while each surfscan event is marked by a "+". If a problem on the wafer was detected by both measurement techniques, both symbols get over ("*").

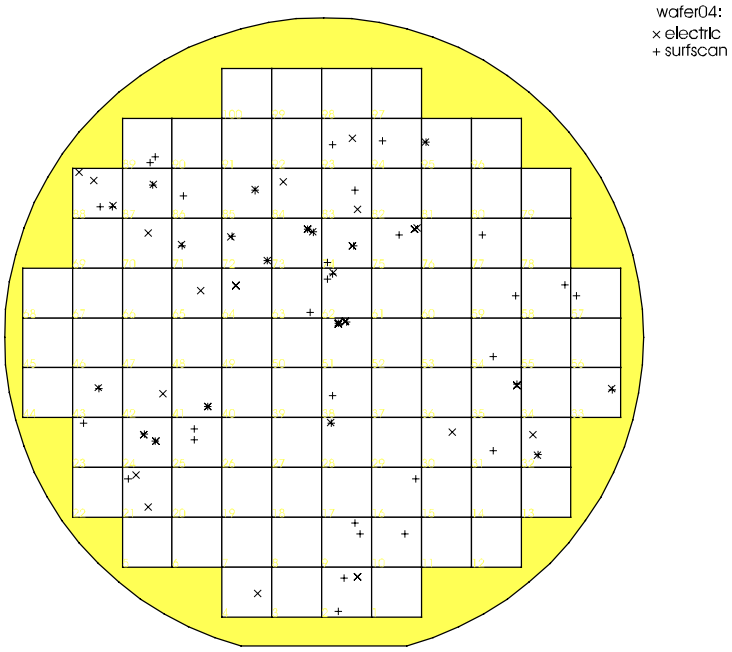

Fig. 6: Detected surfscan defects and electrical faults on wafer "04".

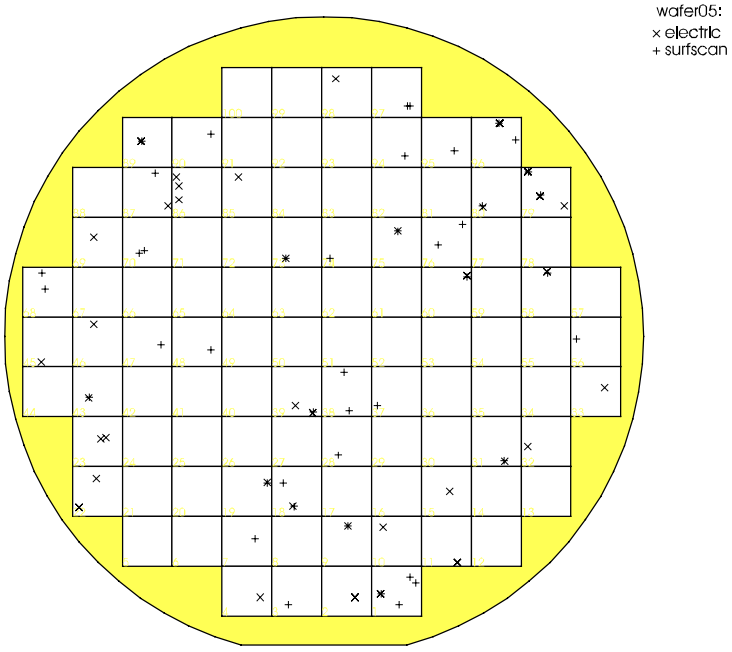

Fig. 7: Detected surfscan defects and electrical faults on wafer "05".

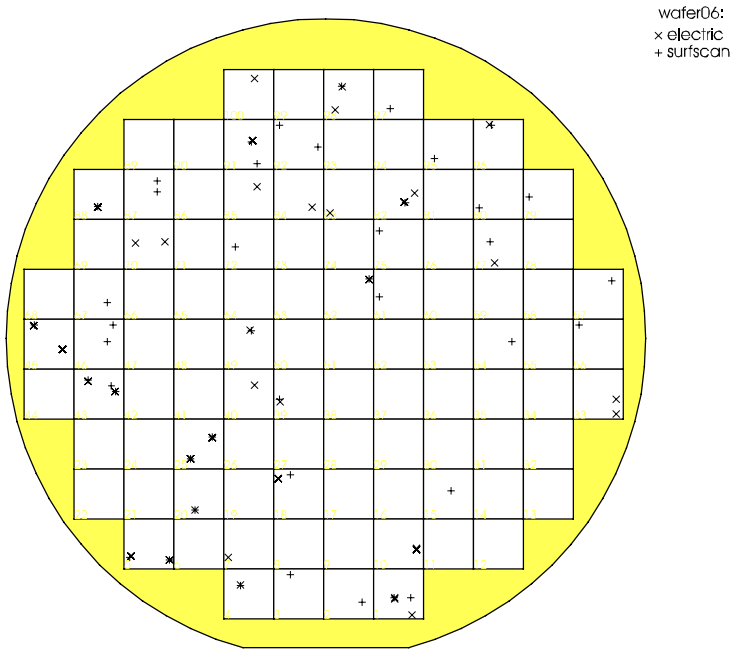

Fig. 8: Detected surfscan defects and electrical faults on wafer "06".

It can be seen, that there are a lot of identical positions on each wafer. We summarize the percentage of matching events in the following figure. The first curve (electric) gives the percentage of matching electrical events referring to the total number of electrical events per wafer. The second curve (surfscan) shows the percentage of matching surfscan events referring to the total number of surfscan events per wafer. Just about one third of the events describe the same problem on a wafer. Is this enough, to conclude further correlations?

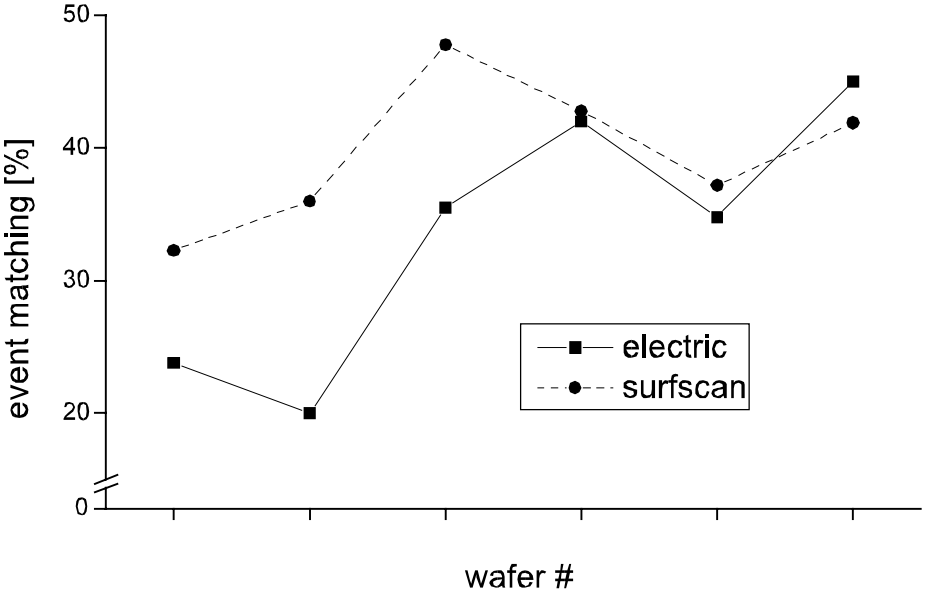

Fig. 9: Percentage of matching events in lot "A".

4 CORRELATIONS

First, we look at the total number of events. Figure 10 shows the frequency of all electrical events (independent of the defective interconnection metal layer) and the surfscan events found in the "metal-1" layer of lot "A". The number of events seems to be the same for three wafers only.

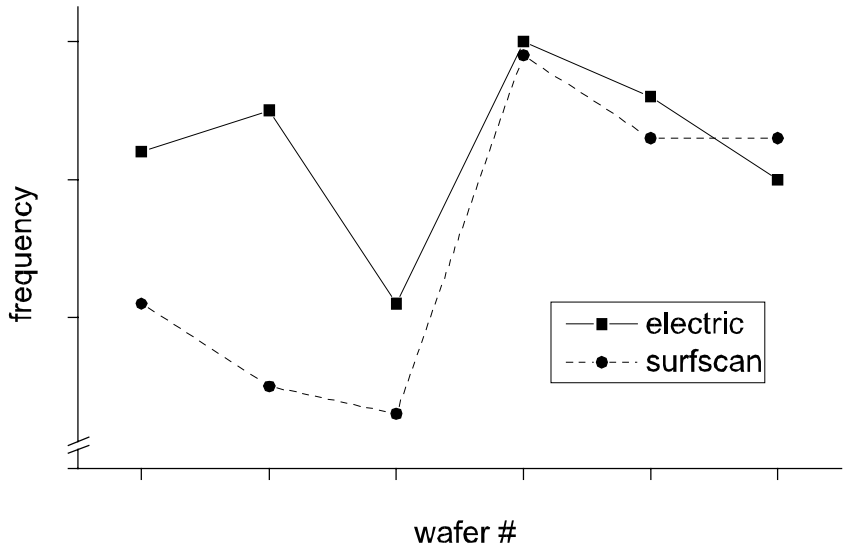

Fig. 10: Number of detected surfscan defects and electrical faults in lot "A".

The next step is a comparison of yield determined by electrical measurements and yield based on the surfscan events. The following figure 11 gives the result for lot "A". Neither the absolute yield values match, nor the corse of both yield curves fit. The investigation of the distribution of the electrical faults among the interconnection layers results in the following: The "metal-1" layer was involved in less than 30% of all electrical events only. But, the layer "metal-2" was involved in most electrical faults. So it seems to be more suitable to select surfscan data based on laser scattering after process steps to manufacture the "metal-2" layer.

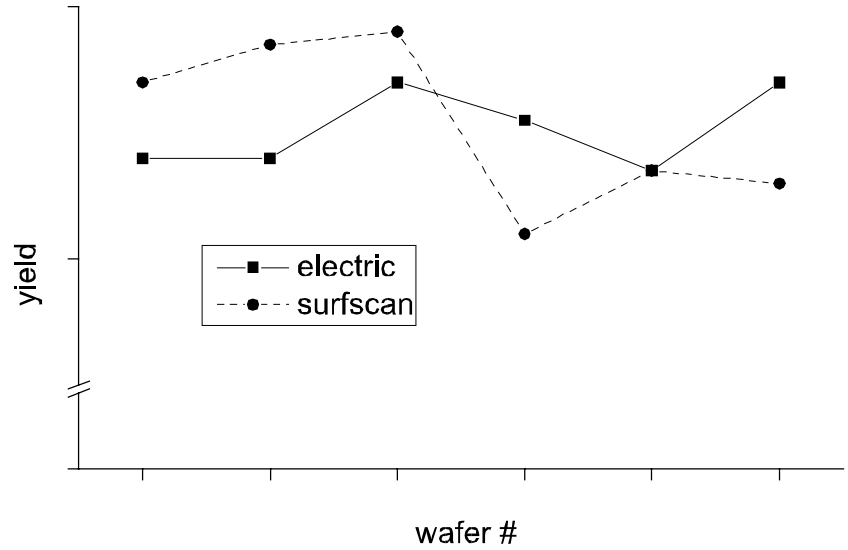

Fig. 11: Comparison of electrical yield and yield based on detected surfscan defects in lot "A".

So, the "metal-2" layer was inspected twice during manufacturing of lot "B", once before etching (level-ID: R23) and once after etching (level-ID: R01). Figure 12 gives the total number of events. It can be seen that the surfscan curve "R23" marks the upper limit of electrical detectable faults while the surfscan curve "R01" marks the lower limit of electrical detectable faults.

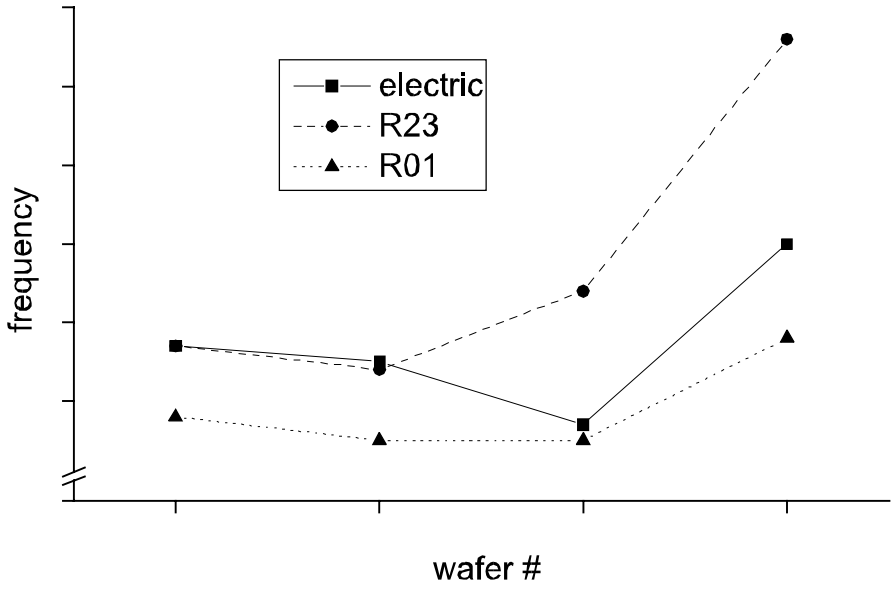

Fig. 12: Number of detected surfscan defects and electrical faults in lot "B".

Again we determined the electrical yield and compared it to both yields based on the surfscan events of the "metal-2" layer. The following figure 13 clearly shows a range of electrical yield limited by both surfscan yield curves. The surfscan yield curve based on the data before etching gives the lower yield limit while the surfscan yield curve based on the data after etching gives the upper yield limit. Due to the etching process, some defects will be eliminated together with the underlying metal. So, the total number of events will be smaller after the etching process step.

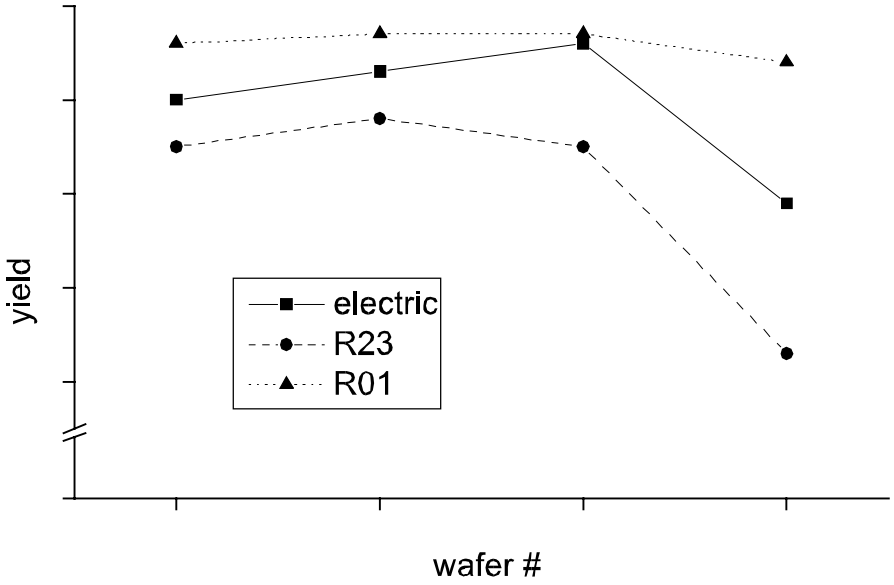

Fig. 13: Comparison of electrical yield and yield based on detected surfscan defects in lot "B".

5 CONCLUSION

Our results show that the defect density per measured surfscan layer is higher than the defect density of electrical faults focused on the same layer only. But there are some data of selected surfscan layers which fit to the total number of electrical faults among all layers. This enables the determination of a yield range based on these selected surfscan data where the total electrical yield has to be inside. In most cases, data from laser scattering systems will point out process specific machine errors which leads to a simplified fault analysis. A precise yield prediction is possible, if and only if surfscan data are used from selected layers. Now, the future step will be a more accurate wafer yield prediction of product chips based on selected surfscan data. Results from test structures will lead the way how to select the right surfscan layers.

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