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A Digital Tester Based Measurement Methodology for Process Control in Multilevel Metallization Systems

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ABSTRACT

The control of metallization layers' integrity gain more importance increasing the total number of metallization layers. Therefore, an electrical measurement procedure has to separate defectless test structure elements from faulty test structure elements. To decrease the number of test procedures and test equipment, this binary decision will be made parallel to the functional test of product chips using the same digital test system to measure test structure elements too. In addition, the geometrical arrangement of the test structure layout elements will also be transformed to a binary description. As a result of this, novel algorithms will now enable the direct comparison of both binary data sets to extract test structure faults like opens and shorts as well as process specific defect parameters.

Keywords: IC manufacturing, process control, metallization, test structures, digital tester, defect parameter extraction, defect statistics

2 INTRODUCTION

Today's complexity of integrated circuits requires multilevel metallization systems to connect all circuit cells and devices. Due to the occurrence of defects, test structures gain more importance to control the metallization. To receive dependable values of defect parameters, the vast amount of test structure data in various combinations in multilevel metallization must be analyzed. To measure the resistance of these test structures commonly analog or DC parametric test systems are applied, using a measurement frequency below 1 Hz [BCKJ91], [MiHF92], [RoBF92].

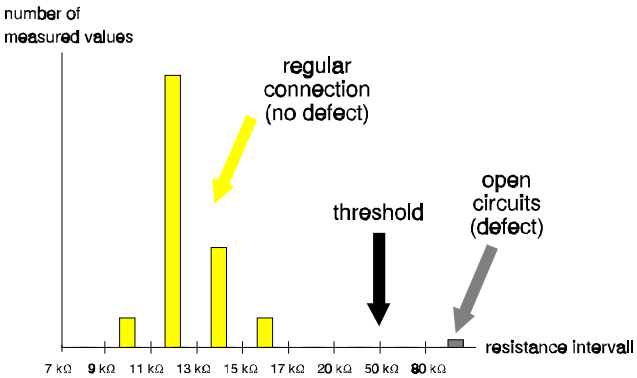


Fig. 1: Histogram of analogly measured line resistances.

The resistance values of about 100 equally designed serpentine structures have been measured. In the histogram of figure 1 two clusters can be distinguished clearly. One of these clusters contains the resistance values of the faultless serpentine structures. The other cluster is due to the serpentine structures with defects causing open circuit faults. In [MiHF92] a similar distribution was obtained. In our case, an electrical test must only decide whether the test structure contains a defect or not. So, in general a digital tester should be sufficient, if the tester parameters are adjusted in a way that these two clusters will be assigned either to the boolean value "0" or the boolean value "1".

Section 3 deals with the function of a digital tester. Section 4 presents the measurement methodology and the analysis procedures. Section 5 describes some experimental results and finally section 6 concludes the paper.

3 DIGITAL TESTER

The results of experiments (ref. section 2) have shown that applying a digital tester is feasible. A digital tester has important advantages. First, the measurement frequency of a digital tester is normally many times higher than the frequency used during analog 2- or 4-point measurements. So the evaluation of test structures can be much faster. Furthermore, every measured value needs only one bit which reduces the storage requirements. Also, a data reduction is possible already during the electrical measurements since the measured binary data can be easily compared to reference values. Finally, using a digital tester simplifies in-line process control because test chips and product chips can be measured in the same way and with the same measuring equipment.

A tester is required with bidirectional channels which can send a stimulus voltage V_s as well as receive a response voltage V_m. A bidirectional channel in stimulus mode consists of a voltage source and an internal resistance R_s. A bidirectional channel in response mode consists of a level sense at a terminating resistor R_r

A tester channel in stimulus mode can force a voltage to the connected pad. Forcing a positive voltage means to force the boolean value "1". Modern digital test systems can simulate a termination resistance by forcing a current through the response channel. The corresponding driver voltage could be positive or negative. So it is possible to force a stimulus channel with boolean "0" also. The tester channel in response mode can measure a voltage assigned to a boolean value corresponding to the threshold voltage. A measured voltage below the threshold voltage will be assigned to the boolean value "0" and a measured voltage above the threshold voltage will be assigned to the boolean value "1". The following figure shows the different states of a tester channel.

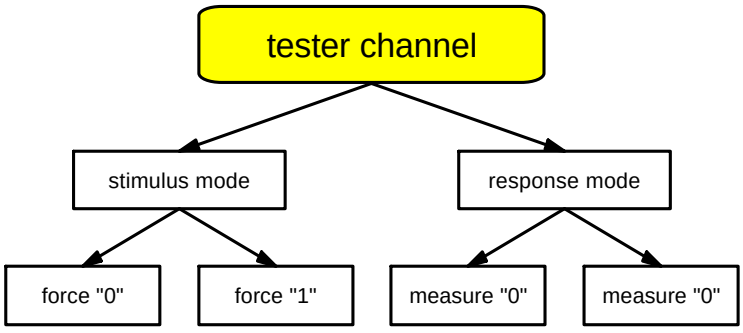


Fig. 2: Description of digital tester states.

4 MEASUREMENT METHODOLOGY

To achieve an efficient digital measurement methodology, the following steps are introduced. First the test structure design has to be transformed to a binary description (ref. section 4.1). The tester adaption describes the determination of parameters to provide the test procedure (ref. section 4.2). After the test run the measured data will be analyzed to get information about process specific faults and defects (ref. section 4.3).

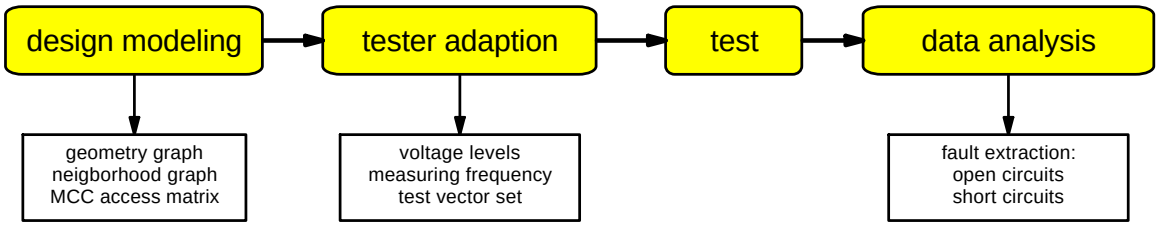


Fig. 3: Procedure to digitally measure and analyze test structures.

4.1 Design modeling

The current quality evaluation of the IC manufacturing process requires continuous observation of the process specific defect parameters like the density of metal shorts, opens and open vias as well as stacked vias. These parameters are usually determined by analyzing the following test structures, coming through the whole technological process [IpSa77] [LYWM86] [Walk87] [BCKJ91] [Bueh83]. The comb structure (fig. 4a) is used to detect metal shorts. Metal opens are determined by investigating serpentine lines (fig. 4b) and via strings (fig. 4c), which combine the metal links on two different metal layers, helping to find open vias.

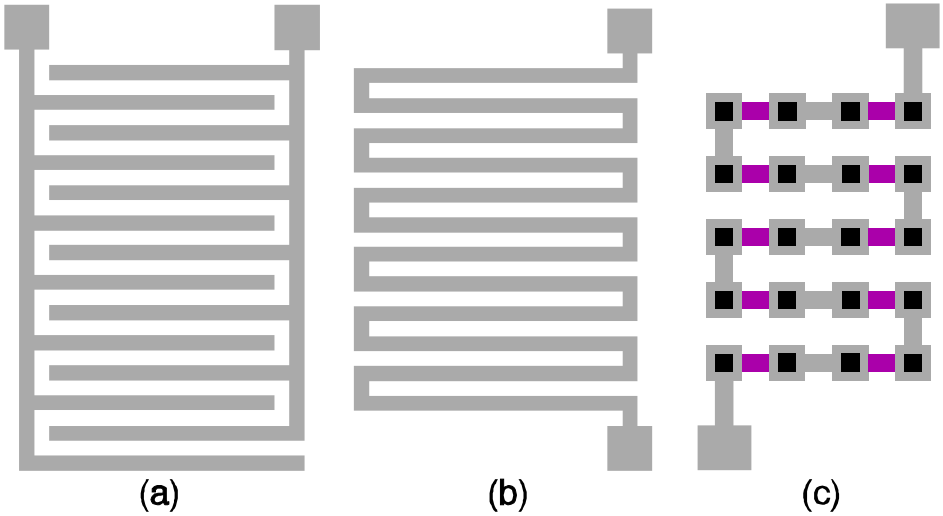
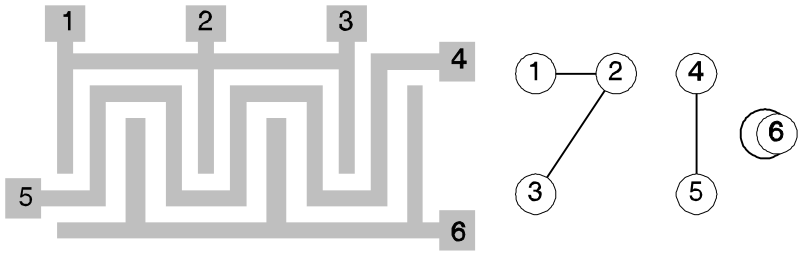


Fig. 4: Basic test structures for metallization systems ((a) comb; (b) serpentine; (c) via string).

To realize an efficient digital data analysis, it is necessary to transfer the layout data of test structures to data which are comparable to the binary data set of a digital tester. Therefore, the layout data of these different test structures have to be modeled with the *geometry graph* and the *neighborhood graph*.

4.1.1 Geometry graph

The identification of open circuit and short circuit defects requires information about the geometry of layout elements inside a test chip. These layout elements can be modeled with a geometry graph. The following table explains the geometry graph.



Node of graph:	**Edge of graph:**
Measuring point (pad of the test structure)	CC: All conductive layout elements (e. g. serpentine line between two measuring points. **Rules:** CCs which are only connected to one measuring point will be modeled as loops.

Tab. 1: Description of the geometry graph [HeWe94].

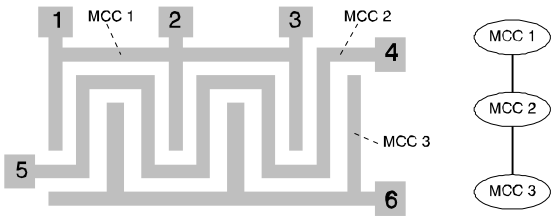
The geometry graph will be transformed to the matrix GEO where the top-down row index and the left-right column index represent the nodes of the geometry graph. Only if there is an edge between two nodes i and j the matrix elements $geo_{i,j}$ and $geo_{j,i}$ will be given the boolean value "1". The boolean value "0" is given to all other elements of the matrix.

$$GEO = \begin{pmatrix} 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \quad (1)$$

4.1.2 Neighborhood graph

The localization of short circuit defects requires additional information about the neighborhood relationship between differently connected layout elements. Generally a test structure contains a set of CCs which are possibly arranged in different layers. The following table 2 explains the neighborhood graph. Also the neighborhood graph will be transformed to a matrix NBH where the top-down row index and the left-right column index represent the MCCs. Only if there is an edge between two nodes i and j the matrix elements $nbh_{i,j}$ and $nbh_{j,i}$ will be given the value "1". The value "0" is given to all other elements of the matrix.

$$NBH = \begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{pmatrix} \quad (2)$$



Node of graph:	**Edge of graph:**
MCC: A maximal set of conductive components that are connected to each other. **Rules:** Every node of the neighborhood graph corresponds to a subset of nodes of the geometry graph and edges of the geometry graph	Neighborhood relationship between two different MCCs (undesigned shorts). **Rules:** Two nodes MCC_1, MCC_2 are connected by an edge if somewhere inside the test structure layout elements of MCC_1 and MCC_2 are adjacent with only nonconducting material between them.

Tab. 2: Description of the neighborhood graph [HeSt94] [HeWe94].

4.1.3 MCC access matrix

The assignment of the MCC indices of the neighborhood graph to the measuring point indices of the geometry graph will be described in the MCC-access matrix (MCA). The top-down row index represents the increasing indices of the MCCs while the left-right column index represents the increasing measuring point index of the geometry graph. Is there a conductive connection between an MCC in row i and a measuring point in column j, the matrix element $mca_{i,j}$ is given the value "1". A matrix element is assigned to the value "0" if there is no conductive connection.

$$MCA = \begin{pmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \tag{3}$$

4.2 Tester adaption

A binary tester data set is the result of measured voltages, currents, and resistances inside test structures. To achieve a complete adaption of a digital tester to the test structure conditions, the stimulus voltage V_s, the threshold voltage V_{th} and the measuring frequency f_m have to be adjusted corresponding to the resistance of the test structure elements. In case of test structure elements in multilevel metallization layers the following assumptions simplify the calculation of the tester voltage levels:

parameter	assumption
determination of R_{min}	smallest resistance between two measuring points
determination of R_{max}	largest resistance between two measuring points
determination of I_{max}	maximum current of smallest test structure element
terminating resistance of tester R_r	$R_r >> R_{max}$
no. of measuring points per MCC	≤ 5

Tab. 3: Assumptions of test structure parameters inside metallization layers.

So, the stimulus voltage V_s, the threshold voltage V_{th} and the measuring frequency f_m will be adjusted using the following equations:

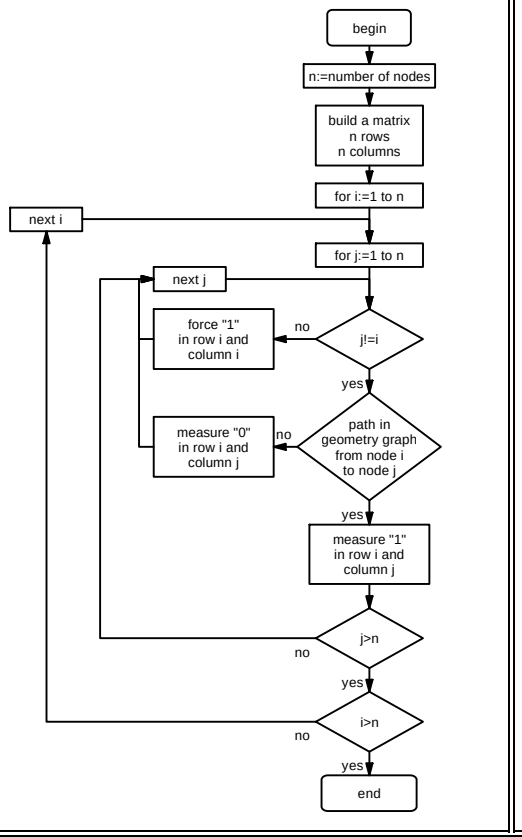
tester parameter	value
V_s (stimulus voltage)	$V_s = \frac{R_{min}}{I_{max}}$
V_{th} (threshold voltage)	$V_{th} \approx 0.2 \cdot V_s$
f_{max} (measuring frequency)	$f_{max} \approx 10\ kHz$

Tab. 4: Adjustment of the digital tester values.

Complex test structures having more than 5 measuring points per MCC or high resistance layers (e. g. polysilicon) require more detailed calculations which can be found in [HeWe95c].

4.2.1 Test vector set

A test structure without any active semiconductor devices like transistors or diodes will completely be tested forcing the boolean value "1" once at each node of the corresponding geometry graph while all other tester channels are in response mode. Due to the edges of the geometry graph the nodes which are in response mode receive either boolean "0" or boolean "1". The following table shows the generation algorithm for the test vector set and a sample test vector matrix.



$$WOM = \begin{pmatrix} 1 & H & H & L & L & L \\ H & 1 & H & L & L & L \\ H & H & 1 & L & L & L \\ L & L & L & 1 & H & L \\ L & L & L & H & 1 & L \\ L & L & L & L & L & 1 \end{pmatrix} \quad (4)$$

WOM : *Walking one* test vector matrix
L : Measure "0"
H : Measure "1"
0 : Force "0"
1 : Force "1"

Tab. 5: Test vector set generation.

If this type of test vector set called *walking one* is used, not only each column of the matrix can be assigned to one specific node of the geometry graph, but also each row of the matrix will be assigned to one specific node of the geometry graph. Hence, every measured "1" in the matrix represents an edge between $node_{row}$ and $node_{column}$. For that, a walking one test vector set is required to directly compare the test data set to the graph matrices.

4.3 Data analysis

The run of a digital test yields the information about the connections between the measuring points of a test chip. The digital information of the tester will be stored in a response test matrix (TEST). The arrangement of rows and columns is identical to the test vector set WOM introduced in section 4.2.1. The response test matrix of a faultless test structure is called *golden device* (GLD).

$$TEST = GLD = \begin{pmatrix} 1 & H & H & L & L & L \\ H & 1 & H & L & L & L \\ H & H & 1 & L & L & L \\ L & L & L & 1 & H & L \\ L & L & L & H & 1 & L \\ L & L & L & L & L & 1 \end{pmatrix} \tag{5}$$

In case of faults, the digital tester will mark the position in the matrix with a special sign. In our case the sign "." means the tester did measure a boolean "1" in case of a boolean "0". For further analysis, these values should be replaced by the boolean values according to the following table.

tester directive	tester response in case of no faults		tester response in case of faults	
	tester specific sign	corresponding boolean value	tester specific sign	corresponding boolean value
measure "0"	L	0	.	1
measure "1"	H	1	/	0

Tab. 6: Data translation table.

The following figure shows a faulty test structure and its sample test data including the translation to binary data only.

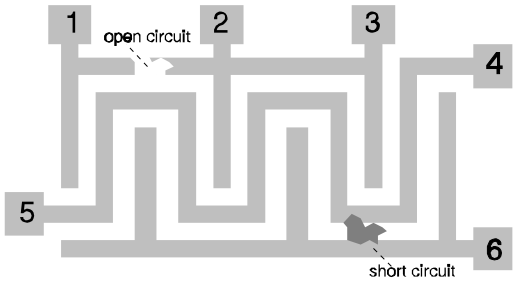


Fig. 5: Faulty test structure.

$$TEST = \begin{pmatrix} 1 & / & / & L & L & L \\ / & 1 & H & L & L & L \\ / & H & 1 & L & L & L \\ L & L & L & 1 & H & . \\ L & L & L & H & 1 & . \\ L & L & L & . & . & 1 \end{pmatrix} \rightarrow \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{pmatrix} \tag{6}$$

To find all open circuits and short circuits, two basic matrix algorithms will be applied. The resulting quadratic matrices contain redundant information ($a_{i,j} = a_{j,i}$), so that only half of the matrix is sufficient to extract the number of faults. The following sections describe how to find open circuits and short circuits where the following boolean matrix operations are used:

symbol	meaning
^{T}	$C = A^T$ where: $c_{i,j} = a_{j,i}$
$\overline{\ }$ (bit by bit: inversion)	$C = \overline{A}$ where: $c_{i,j} = \begin{cases} 0 & \text{if: } a_{i,j} = 1 \\ 1 & \text{if: } a_{j,i} = 0 \end{cases}$
$\wedge$ (bit by bit: AND)	$C = A \wedge B$ where: $c_{i,j} = a_{i,j} \wedge b_{i,j}$
$\cdot$ (product of matrices)	$C = A \cdot B$ where: $c_{i,j} = \bigvee_{k=1}^{m} (a_{i,k} \wedge b_{k,j})$ where : $a_{i,k} \in \mathbb{R}_{n,m} \wedge b_{k,j} \in \mathbb{R}_{m,r} \wedge c_{i,j} \in \mathbb{R}_{n,r}$

Tab. 7: Boolean operations for matrices containing boolean elements.

4.3.1 Open circuits

The open circuit matrix OPEN is created by an AND operation of GLD and the inverted TEST matrix. After that a bit by bit AND operation with the matrix of the geometry graph GEO yields the open circuit matrix.

$$\text{OPEN} = \left(\text{GLD} \wedge \overline{\text{TEST}} \right) \wedge \text{GEO} \tag{7}$$

A boolean value "1" in the OPEN matrix represents an open circuit between two pads. The following equation shows the OPEN matrix of our sample test structure.

$$\text{OPEN} = \begin{pmatrix} 1&1&1&0&0&0 \\ 1&1&1&0&0&0 \\ 1&1&1&0&0&0 \\ 0&0&0&1&1&0 \\ 0&0&0&1&1&0 \\ 0&0&0&0&0&1 \end{pmatrix} \wedge \begin{pmatrix} 0&1&1&1&1&1 \\ 1&0&0&1&1&1 \\ 1&0&0&1&1&1 \\ 1&1&1&0&0&0 \\ 1&1&1&0&0&0 \\ 1&1&1&0&0&0 \end{pmatrix} \wedge \begin{pmatrix} 1&1&0&0&0&0 \\ 1&1&1&0&0&0 \\ 0&1&1&0&0&0 \\ 0&0&0&1&1&0 \\ 0&0&0&1&1&0 \\ 0&0&0&0&0&1 \end{pmatrix} = \begin{pmatrix} 0&1&0&0&0&0 \\ 1&0&0&0&0&0 \\ 0&0&0&0&0&0 \\ 0&0&0&0&0&0 \\ 0&0&0&0&0&0 \\ 0&0&0&0&0&0 \end{pmatrix} \tag{8}$$

In this matrix we find a boolean "1" in row 1 and column 2 that means an open circuit between node 1 and node 2.

4.3.2 Short circuits

The short circuit matrix SHORT is created as follows:

$$\text{SHORT} = \left[\left[\text{MCA} \cdot \text{TEST} \right] \cdot \text{MCA}^T \right] \wedge \text{NBH} \tag{9}$$

The following equation shows the SHORT matrix of our sample tester data.

$$\mathrm{SHORT} = \left[\left[\left[\begin{pmatrix} 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{pmatrix}\right] \cdot \begin{pmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix}\right] \wedge \begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{pmatrix} \qquad (10)$$

A boolean value "1" in the SHORT matrix represents a short circuit between two MCCs. In this example a short circuit was detected between MCC_2 and MCC_3.

5 EXPERIMENTAL RESULTS

All these algorithms including the generation of the golden device have been implemented in a program system called VIADUCT (**V**ersatile Automatic **I**dentification **A**nalysis of **D**efects from **U**ndesigned Open and Short **C**ircuits in **T**est Structures). To validate the procedure of data measurement, about 1000 test chips with different test structures, designed inside a boundary pad frame of 40 pads, were manufactured at the *Institut für Mikroelektronik Stuttgart, Germany*. The test structure design bases on a crosswise arrangement of lines in two metal layers as can be seen in figure 6.

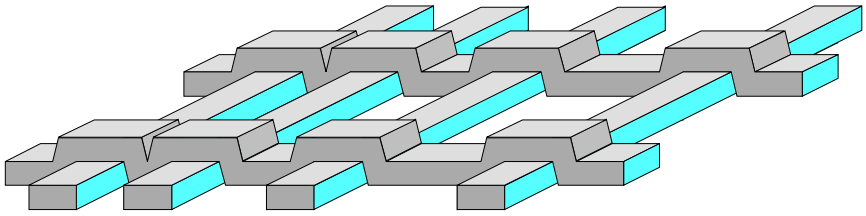


Fig. 6: Test structure design.

The topography of the underlying layers is represented by parallel lines with different spaces, which varies logarithmically. Figure 7 shows the distribution of the metal-2 short circuits, where the number of defects is proportional to the line width.

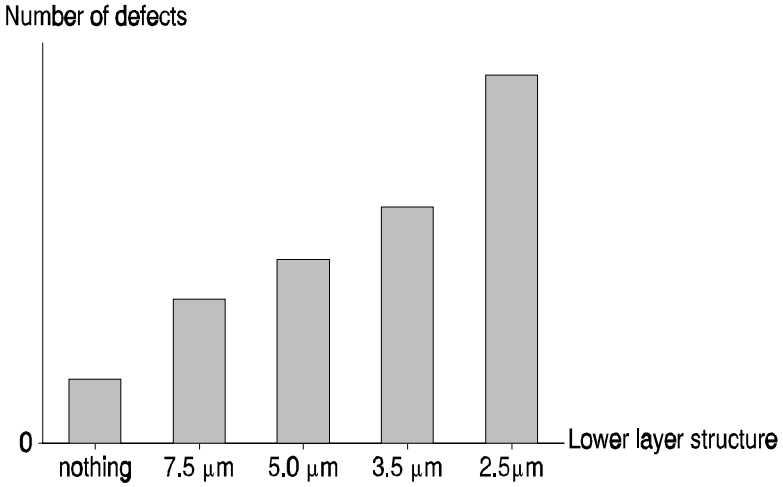


Fig. 7: Number of metal-2 short circuits.

The overall distribution of the metal-2 open circuits can be seen in figure 8, where the number of defects is proportional to the line width. The distributions of the metal-2 open circuits being dependent on the lower layer structure and the line width can be seen in the figures 9 and 10, where different minima and maxima appear.

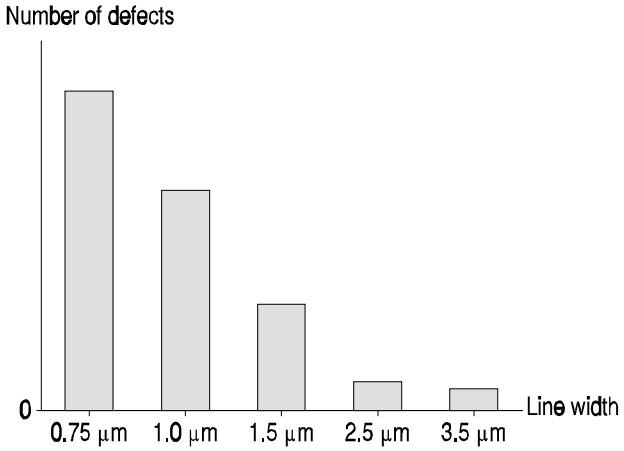


Fig. 8: Overall number of metal-2 open circuits dependent on the line width.

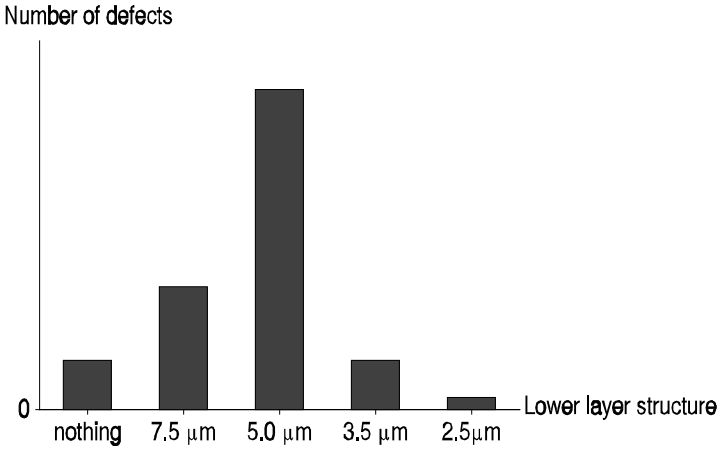


Fig. 9: Number of metal-2 open circuits in 0.75 µm lines dependent on the lower layer structure.

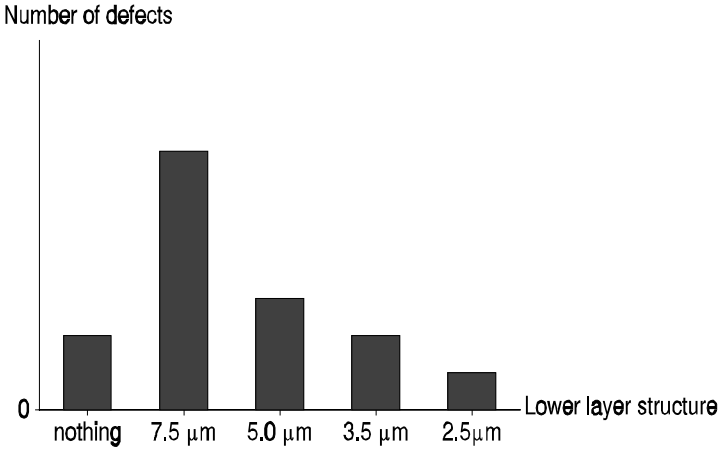


Fig. 10: Number of metal-2 open circuits in 1.5 µm lines dependent on the lower layer structure.

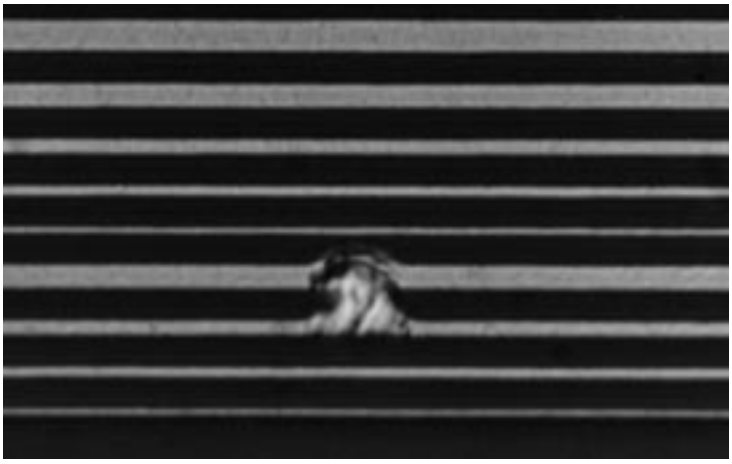


Fig. 11: Detected short circuit defect.

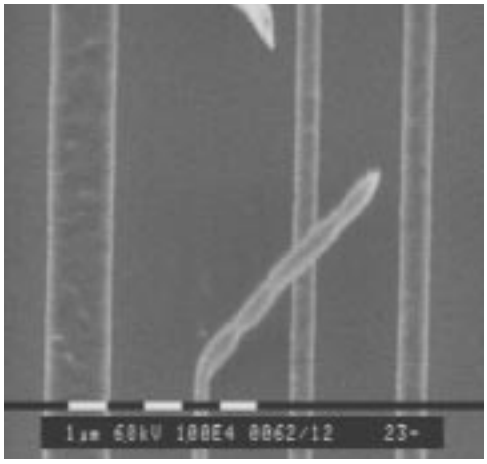


Fig. 12: Detected open circuit defect.

6 CONCLUSION

In this paper a novel measurement strategy for the evaluation of process specific defect parameters is proposed. First, test structure designs have to be modeled and transformed to binary data. To get accurate results the digital tester voltage levels and measurement frequency has to be adjusted corresponding to test structure resistances. Finally novel matrix algorithms extract open and short circuits from the tester response data set. Experimental results confirm the high dependability of the proposed measurement methodology. Using a digital tester reduces the costs to analyze test structures.

Decrease of equipment costs:
In the proposed approach the equipment costs reduction is achieved by manufacturing test vehicles inside standard boundary pad frames. So, standard probe cards and standard measuring equipment will be used.

Decrease of personnel costs:
The personnel costs reduction is achieved by manufacturing the test vehicles side by side with product chips. The measurement is accomplished automatically during the functional test of the product chips. The results are calculated within a few seconds, so that sufficient statistics can be obtained.

Decrease of time:
The decrease of measuring time is achieved by using a high speed digital tester with the measuring frequency f_m. A test vehicle with n boundary pads is completely tested in n/f_m seconds. The decrease of analyzing time is achieved by comparing the measured data to reference data. This yields all detected open and short circuits.

7 ACKNOWLEDGMENTS

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