

Wafer Level Defect Density Distribution Using Checkerboard Test Structures

Christopher Hess, Larg H. Weiland

Institute of Computer Design and Fault Tolerance (Prof. Dr. D. Schmid)
University of Karlsruhe, P. O. Box 6980, 76128 Karlsruhe, Germany
Phone: +49-721-6084217, FAX: +49-721-370455, <http://goethe.ira.uka.de/ddg>

Abstract - Defect density distributions play an important role in process control and yield prediction. To improve the accuracy in modeling defect density distributions we present a wafer level methodology to analyze defect data measured anywhere on a wafer. So, the inspected area may be limited to test structures that just cover a fraction of each wafer. For that, imaginary wafermaps are generated for a variety of different chip areas to calculate a yield-to-area dependency. Based on these calculations a Micro Density Distribution (MDD) will be determined for each wafer that reflects the degree of defect clustering. The single MDDs per wafer may be summarized to also provide a General Defect Density Distribution per lot or any other sample size.

1 INTRODUCTION

TODAY'S complexity of integrated circuits requires more and more conducting backend layers to connect all circuit cells and devices. Undesigned layout objects (**defects**) can occur during the manufacturing process. Dependent on the layout, defects can become the cause of electrically measurable **faults** which are responsible for manufacturing related malfunctions of chips. So, defect density distributions are important for yield prediction and to control quality of process steps and product chips. For each wafer, a single defect density value will be determined as the total number of defects on the wafer divided by the total area of the wafer. To determine a defect density distribution, many wafers have to be investigated. So, a defect density distribution reflects the wafer to wafer density variations or the lot to lot density variations, respectively.

Especially in yield modeling also chip to chip density variations are discussed - better known as defect clustering. For that, more than just one defect density value per wafer is required. So, the total wafer area has to be divided in area segments each providing an individual defect density value. To get area segments that are nearly independent of known defect cluster effects, we have developed a methodology to calculate a wafer level **Micro Density Distribution (MDD)**.

To determine wafer level defect density distributions, it is necessary to locate each detected defect on the wafer. Optical defect inspection systems provide such data but, only electrically based data represent those defects that are large enough to impact yield. For that Section 2 briefly describes the Checkerboard Test Structure design. Section 3 introduces yield-to-area calculations to obtain a segmentation of the wafer area. Sections 4 and 5 present a novel methodology to calculate and model wafer level defect density distributions. Finally we present some experimental results and conclude our approach.

2 CHECKERBOARD TEST STRUCTURE

To get defect densities, simple test structures of comb and serpentine lines are commonly used [Bueh83], [LYWM86]. But, simple test structures do not provide any defect localization inside large chip areas, which are required to detect defects even if the average defect density is low. Using the **Checkerboard Test Structure (CTS)** introduced by [Hess94], [HeSt94], [HeWe95b] guarantees a large defect sensitive area inside a given pad frame.

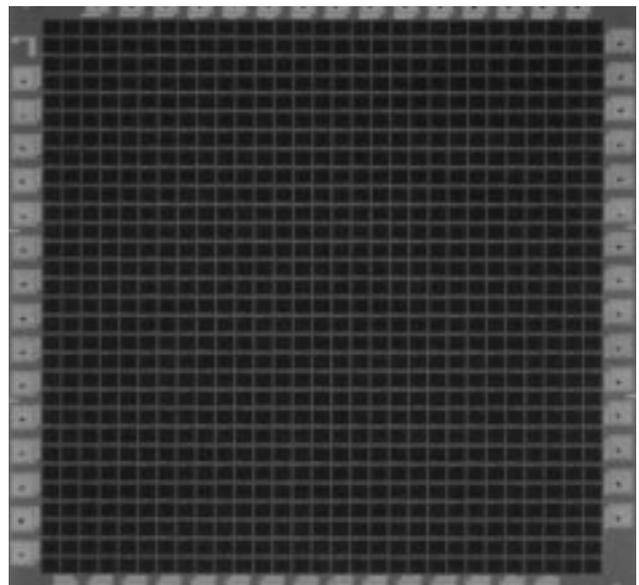


Fig. 1: Checkerboard Test Structure containing 870 subchips.

To enable precise defect localization, the Checkerboard Test Structure divides the total chip area into a large number of electrically distinguishable subchips. If a fault will be measured between 2 pads, algorithms clearly provide the subchip containing the defect that has caused the measured fault. Figure 1 shows a CTS containing 870 subchips.

3 YIELD-TO-AREA CALCULATIONS

A Checkerboard Test Structure (CTS) provides a list of defect positions. Based on a known wafermap each chip can be marked as "pass" or "fail" dependant on the absolute position of a defect. A chip is marked as "fail", if at least one defect is detected inside the chip boundaries. For a specific wafermap a yield value Y can be calculated using the following Equation:

$$Y = \frac{\text{number of pass chips}}{\text{total number of chips}} \quad (1)$$

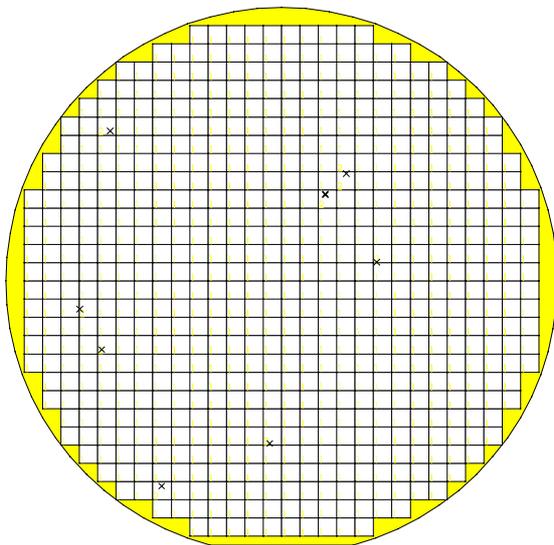


Fig. 2: Imaginary wafermap containing 648 chips.

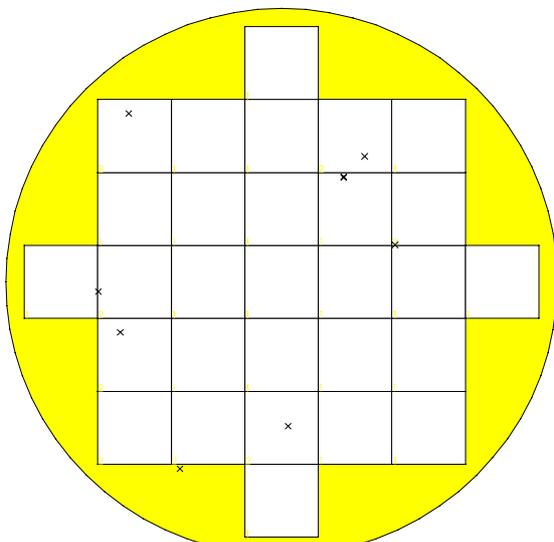


Fig. 3: Imaginary wafermap containing 29 chips.

By generating an imaginary wafermap based on a given chip area A and projecting it on the original wafer, we can again calculate a yield value using the same defect list given by the data of the CTS. The Figures 2 and 3 show two different imaginary wafermaps. In each wafermap, black symbols mark the defects detected inside the Checkerboard Test Structures. For a series of imaginary wafermaps, the yield will be determined dependent on the chip area. This results in a **Yield-to-Area Curve** as can be seen in the following Figure.

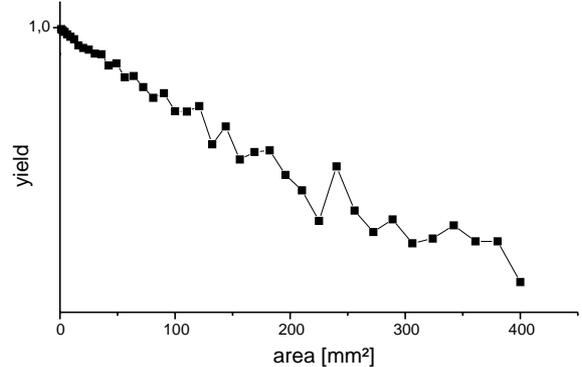


Fig. 4: Yield-to-area curve of electrically detected defects on a wafer.

4 MICRO DENSITY DISTRIBUTION (MDD)

Based on a given imaginary chip area A a defect density value D can be calculated using the following Equation:

$$D = \frac{1 - Y}{A} \quad (2)$$

Y : yield

A : area of a single imaginary chip

D : defect density

This Equation assumes that the wafer area is completely covered by defect sensitive test structures. But, if test structures are combined with product chips or placed inside the sawing lines they just cover a fraction of the complete wafer area. So, there will be an influence on the calculation of the defect density values. For example, the following Figure shows a map of 4 by 4 reticles just containing a limited test chip area beside product chips. The black boxes inside the test chips mark detected defects. Assuming that the test chip area is 1cm^2 we can determine a defect density value using Equation (2) which yields $D=0.25$.

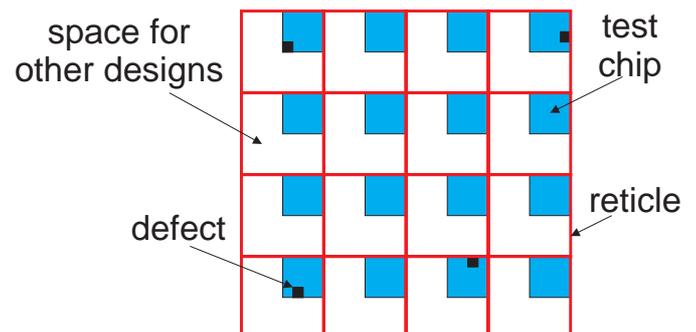


Fig. 5: Dividing reticles into test chip area and product chip area.

We now generate four different imaginary wafermaps as can be seen in the following Figure.

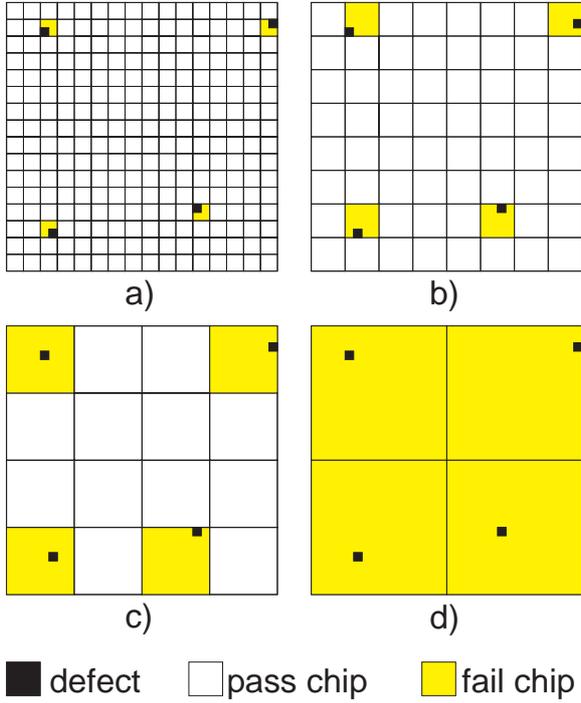


Fig. 6: Different imaginary wafermaps.

Based on these wafermaps Equation (2) results in the following four defect density values:

- The imaginary wafermap (a) has 256 chips with a chip area of 0.5²cm which yields a defect density of D=0,0625.
- The imaginary wafermap (b) has 64 chips with a chip area of 1.0²cm which yields a defect density of D=0,0625.
- The imaginary wafermap (c) has 16 chips with a chip area of 2.0²cm which yields a defect density of D=0,0625.
- The imaginary wafermap (d) has 4 chips with a chip area of 4.0²cm which yields a defect density of D=0,0625.

It is obvious that these defect density values are too small, because they are based on defect data that were measured on just 1/4 of the reticle area. To get accurate defect density values an area factor γ has to be added to the defect density Equation (2). The factor γ represents the area covered by defect sensitive test structures in comparison to the complete reticle area.

$$D = \frac{1 - Y}{\gamma \cdot A} \quad (3)$$

In our example we just inspected a quarter of the reticle area ($\gamma=0.25$), so that the defect density value will be $D=0.25$ which corresponds to the measured defect density value within the original wafermap.

Generally, the yield based on different imaginary wafermaps will decrease by increasing the imaginary chip area. This may have a detrimental influence on Equation (3) which will be investigated regarding the following Figure containing two different maps with different chip areas.

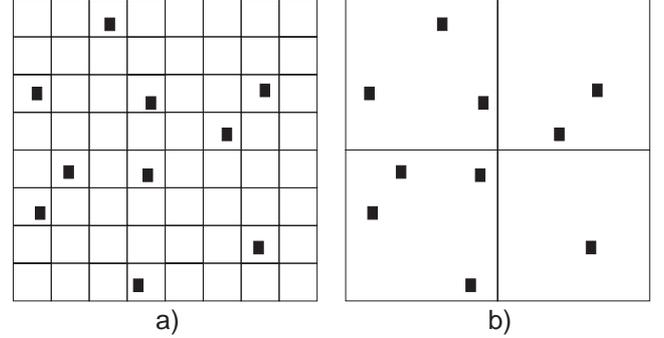


Fig. 7: Different imaginary wafermaps.

The defect density calculated by Equation (3) will remain true as long as no more than one defect will be in a "fail" chip as can be seen on the left side of the Figure. The right side of the Figure shows chips containing more than one defect. In this case, defects are hidden so that Equation (3) yields defect density values that are too small. To prevent this detrimental effect, the chip area of the imaginary wafermaps has to be limited, so that a "fail" chip does not contain more than one defect. For that, the average defect density \bar{D}_n of n calculated values D_i has to be within the limit of approximation (4). The factor ϵ has to be selected dependent on the average number of defects per wafer. A high number of defects requires a low ϵ value.

$$\gamma \cdot A_n \cdot \bar{D}_n < \epsilon \quad \text{where: } 0.5 \leq \epsilon < 1.0 \quad (4)$$

$$\text{where: } \bar{D}_n = \frac{1}{n} \sum_{i=1}^n D_i$$

A_n : chip area corresponding to defect density D_n

To get a set of defect density values per wafer, it is important to start calculating the defect density D_i within the yield-to-area curve for the smallest available chip area A_j . Then the chip area has to be increased as long as the fail chips just contain one defect (ref. Equation (4)). So, it is possible to determine the so called **Micro Density Distribution (MDD)** by counting the occurrence of defect density values D_i per density interval which can be seen in the following Figure 8. To get comparable defect density distributions within different layers on a wafer, we use the probability density of defects by normalizing the curve which means that the sum of all occurrence values has to be set to "1". In addition to that, we also determine the overall defect density on a wafer as the total number of defects on a wafer divided by the total inspected area of the wafer. Figure 8 contains this value as additional small vertical peak.

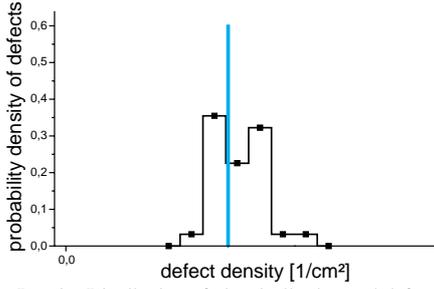


Fig. 8: Micro Density Distribution of electrically detected defects on a wafer.

5 GENERAL DENSITY DISTRIBUTION (GDD)

To get a **General Density Distribution (GDD)** of all wafers in a lot, we have to summarize the single MDDs per wafer. Equation (5) will be used to obtain such a GDD.

$$h_x = \frac{1}{s} \sum_{i=1}^s h_{x,i} \quad (5)$$

h_x : probability density value of the defect density interval x of the General Density Distribution

$h_{x,i}$: probability density value of the defect density interval x of the MDD of wafer i

s : number of wafers

This results in a normalized GDD over all wafers of a lot where the sum of all probability values h_x is 1.

6 EXPERIMENTAL RESULTS

At Elmos, Elektronik in MOS-Technologie GmbH in Dortmund, Germany several Checkerboard Test Structures (CTS) were designed to control defect appearance inside the interconnection layers. The CTS covers 1/6 of the reticle area. To verify the procedure to determine an MDD based General Density Distribution we first divided a wafermap into center and boundary reticles as can be seen in the following Figure.

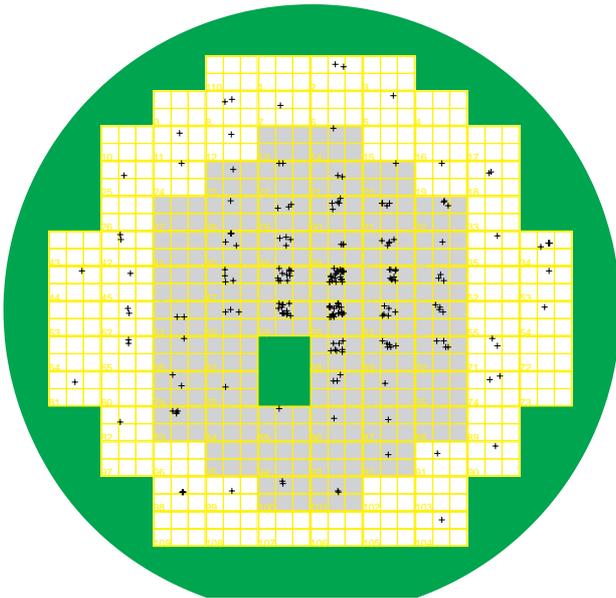


Fig. 9: Arrangement of reticles into center (grey) and boundary reticles (white) on a wafermap including all defects of a complete lot.

The wafermap also contains all defects marked as "X" that occurred within a complete lot. Now, we separately determined the MDDs of all wafers for the center reticles and the boundary reticles. Summarizing the single MDDs to a GDD results in the bars of the following Figure.

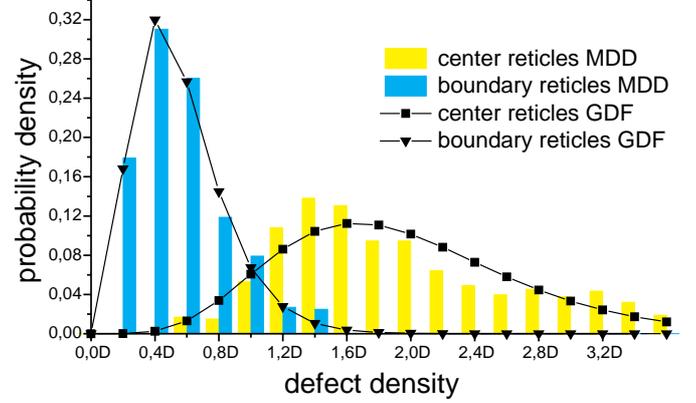


Fig. 10: Comparison of MDD based GDDs of center and boundary reticles including the modeled GDFs.

The chart also includes modeled GDDs using the Gamma Distribution Function (GDF) as described in the Appendix. The wafermap shows that we have a concentration of defects in the center of the wafer. As expected we get a higher defect density for the center reticle GDDs.

In a second experiment we looked to sets of reticles that nearly contain the same number of defects per set. Therefore we partitioned all reticles into a checkered arrangement which can be seen as grey and white reticles in Figure 11.

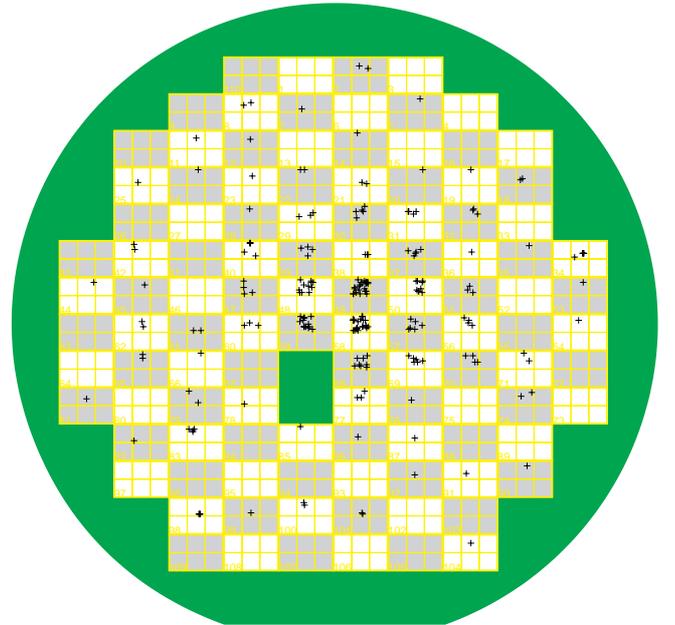


Fig. 11: Checkered arrangement of reticles on a wafermap including all defects of a complete lot.

Again, we determined the single MDDs for each wafer. The GDD and also the modeled Gamma Distribution Function can be seen in Figure 12.

APPENDIX

MODELING DEFECT DENSITY DISTRIBUTIONS

The most popular function for modeling defect density distributions proposed by [OkNS72] and [Stap73] is the **Gamma Distribution Function (GDF)**. The form of $f(D)$ is

$$f(D) = \frac{1}{\Gamma(\alpha) \cdot \beta^\alpha} \cdot D^{(\alpha-1)} \cdot e^{-\frac{D}{\beta}} \quad (6)$$

The parameter α is related to the variance σ^2 of the defect density D . The coefficient β has been interpreted [Ferr89] as the coupling coefficient of the occurrence of the defects. The parameters α and β can be calculated using the following two Equations:

$$\alpha = \frac{D_0^2}{\sigma^2} \quad (7)$$

$$\beta = \frac{\sigma^2}{D_0} \quad (8)$$

The average defect density is calculated by:

$$D_0 = \frac{1}{n} \sum D_i \quad (9)$$

D_i : defect density value of imaginary wafermap i
 n : number of imaginary wafermaps

And finally the variance σ^2 can be calculated using the following equation:

$$\sigma^2 = \frac{1}{n} \left(\sum D_i^2 \right) - D_0^2 \quad (10)$$

The GDF should be normalized by solving the gamma function $\Gamma(\alpha)$

$$\Gamma(\alpha) = \int_0^{\infty} x^{\alpha-1} \cdot e^{-x} dx \quad (11)$$

so that the area under the GDF is 1.

$$\int_0^{\infty} f(D) = 1 \quad (12)$$

ACKNOWLEDGMENT

Parts of this research were supported by *Deutsche Forschungsgemeinschaft (DFG)*, Schm623/3. The authors thank R. Bornefeld, M. Prött and C. Strauch (ELMOS, Dortmund, Germany) for advice and assistance with manufacturing and testing procedures.

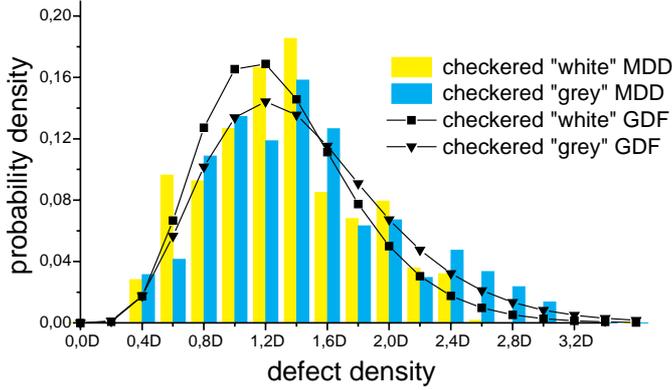


Fig. 12: Comparison of MDD based GDDs of checkered reticles including the modeled GDFs.

As expected, the GDDs are nearly uniform. Finally, the following Figure compares all four Gamma Distribution Functions. It can be seen that the MDD based GDD detects clustered defects. So, the defect density distribution within the boundary reticles is below average while the defect density distribution within the center reticles is above average.

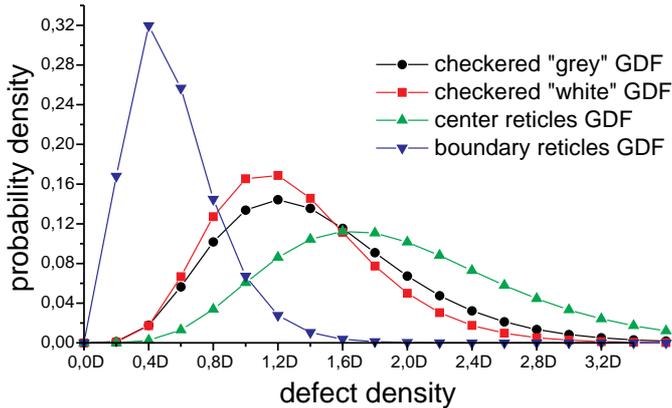


Fig. 13: Comparison of gamma distribution functions (GDF).

7 CONCLUSION

The described method to obtain several defect density values per wafer enables the determination of a single wafer defect density distribution called Micro Density Distribution (MDD). So, chip to chip variations of clustered defect will be evaluated, even if defects will be inspected within test structures that just cover a fraction of the complete wafer area.

Furthermore, all MDDs may be summarized to investigate wafer to wafer and lot to lot variations. An MDD based defect density distribution is sensitive to any defect clustering. The high number of defect density values improves the significance of defect density distribution modeling for yield prediction. The methodology is also applicable to defects detected by optical measurements, but electrically detected defects are more related to product chip yield.

REFERENCES

- [Bueh83] Buehler, M. G.
Microelectronic Test Chips for VLSI Electronics
VLSI Electronics Microstructure Science, pp. 529-576, Vol 9,
Chap.9, Academic Press, 1983
- [Ferr89] Ferris-Prabhu, A. V.
Defects, Faults and Semiconductor Yield
Defect and Fault Tolerance in VLSI Systems, Vol. 1, pp. 129-137
I. Koren, ed. Plenum Press, New York, 1989
- [Hess94] Hess, C.
Strategy to Optimize the Development, Use, and Dimension of
Test Structures to Control Defect Appearance in Backend Process
Steps
Proc. Advanced Semiconductor Manufacturing Conference
(ASMC), pp. 282-289, Boston (USA), 1994
- [HeSt94] Hess, C., Ströle, A.
Modeling of Real Defect Outlines and Defect Parameter
Extraction Using a Checkerboard Test Structure to Localize
Defects
IEEE Transactions on Semiconductor Manufacturing, pp. 284-
292, Vol. 7, No. 3, 1994
- [HeWe95b] Hess, C., Weiland, L. H.
Defect Parameter Extraction in Backend Process Steps using a
Multilayer Checkerboard Test Structure
Proc. International Conference on Microelectronic Test Structures
(ICMTS), pp. 51-56, Nara (Japan), 1995
- [LYWM86] Lukaszek, W., Yarbrough, W., Walker, T., Meindl J.
CMOS Test Chip Design for Process Problem Debugging and
Yield Prediction Experiments
Solid State Technology, pp. 87-92, March 1986
- [OkNS72] Okabe, T. Nagata, M., Shimada, S.
Analysis of Yield of Integrated Circuits and a New Expression of
the Yield
Electrical Engineering in Japan, pp. 135-141, Vol. 92, Dec. 1972
- [Stap73] Stapper, C. H.
Defect Density Distribution for LSI Yield Calculations
IEEE Transactions on Electron Devices, July 1973