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Issues on Short Circuits in Large On-Chip Power MOS-Transistors Using a Modified Checkerboard Test Structure

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***Abstract* — To control random quality deviation of large on-chip power MOS-transistors, we have developed a modified checkerboard test structure. Using this structure, the complete chip area is divided into distinguishable subchips, each containing one large area power MOS-transistor. The fast digital measurements and the precise localization of transistor short circuits guarantee a fast process classification and enable additional electrical and optical defect parameter extraction.**

1 Introduction

More and more former external devices will be included on One-Chip solutions to shrink product size, to decrease the number of devices on PCBs and to improve product and system reliability. During the past few years ELMOS in Dortmund, Germany has improved its manufacturing technology to include large power MOS-transistors with up to 1A drain source current combined with an extremely low leakage current. So, it is possible to have the control circuits and power circuits for e. g. motor-drivers and voltage regulators on just one chip.

The performance of these novel products has to be investigated to shorten process development time and to guarantee the constantly high product quality. One reason for random yield loss may be particle defects. For this reason, a novel test structure has to be designed that includes as many as possible electrically distinguishable large area (0.5mm² to 2.0mm²) power MOS-transistor.

The following section gives the major principles to design a modified checkerboard test structure. Section 3 deals with the test procedure. The localization procedure is presented in Section 4 and Section 5 gives an overview about the automation framework. Section 6 presents some experimental results and finally we conclude our approach.

2 Checkerboard Test Structure

A special test structure is required to enable an efficient electrical test of short circuits of large area power MOS-transistors. It should provide a *large defect sensitive area* to detect defects, even if the average defect density is low. A *precise defect localization* inside the chip area will enable the investigation of the short circuits. Furthermore, the localization also simplifies the optical and electrical determination of defect parameters.

Two major methods to organize test chips are known, the "2 by N" probe-pad array [Bueh79] and standard boundary pads. The defect sensitive area inside a "2 by N" array is relatively small so that the large sensitive area inside the boundary pads seems to be more suitable. But here the number of pads is relatively small so that methods are required to separate defects. Checkerboard Test structures described at [Hess94] and [HWLS96] enable a precise separation and localization of defects by partitioning the whole chip area into a large number of subchips. The following Figure 1 shows the frame of the designed checkerboard test structure.

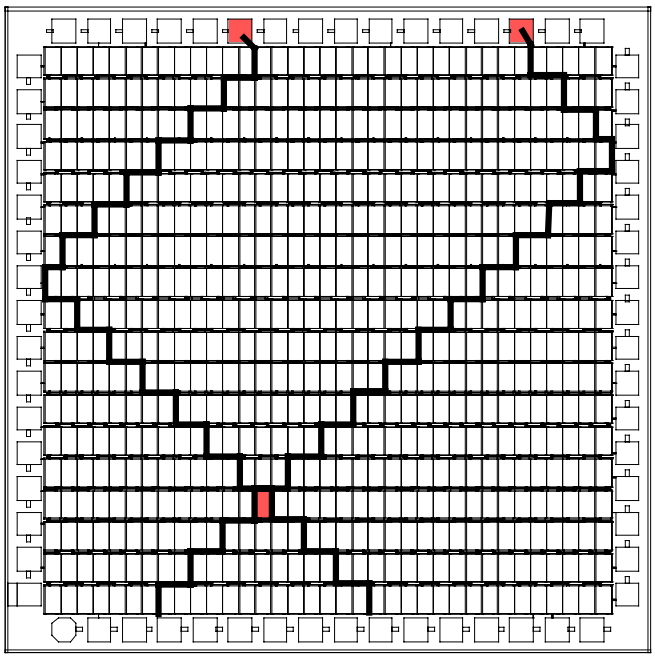


Fig. 1: Modified checkerboard test structure with 630 subchips each containing one power MOS-transistor.

In that Figure, for example, all test structure lines connected to two pads are highlighted. They are adjacent in one single subchip only, which is the key to the defect localization facility.

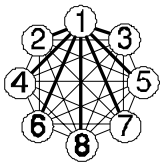
The checkerboard test structure bases on the 2D-permutation procedure described in [HeSt94], [HeWe95b] that arranges all possible ½·**m**·(**m**-1) neighborhood relationships of test structure lines inside a test chip. So, all pairs of test structure lines will be in the rows of the 2D-matrix just once (ref. Table 1).

Equations to determine the elements **a[i,j]** of the 2D-matrix, where the number **m** of lines has to be even

$$a[i,j] := \begin{cases} j \mid 2\cdot i-2 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i \le \frac{m-j-2}{2} \\ 2\cdot m-j-2\cdot i+3 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i > \frac{m-j}{2}-2 \\ 2\cdot i-j-1 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i > \frac{j+1}{2} \\ j-2\cdot i+2 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i \le \frac{j+1}{2} \end{cases} \quad (1)$$

i : row index of the 2D-matrix
j : column index of the 2D-matrix
m : number of pads

Example for **m**=8 lines



1	2	3	4	5	6	7	8
2	4	1	6	3	8	5	7
4	6	2	8	1	7	3	5
6	8	4	7	2	5	1	3

Fig. 2:
Left: Complete neighborhood graph (ref. [HeWe94])
Nodes: Test structure lines
Edges: Two nodes are connected by an edge if test structure elements connected to these test structure lines are adjacent anywhere inside a subchip with only nonconducting material between them.
Right: 2D-matrix, where the gray boxes mark the pairs to test structure line "1".

Tab. 1: 2D-permutation procedure [HeSt94], [HeWe95b].

2.1 Modified Checkerboard Test Structure

Now, the existing checkerboard test structure design has to be modified to investigate power MOS-transistors. An undesigned short circuit defect is only detectable between test structure layout objects connected to electrically distinguishable pads. For that, we will implement a single transistor in a subchip, because each subchip contains a unique set of two test structure lines. One line is connected to the drain of the power MOS-transistor while the other line is connected to the source of the transistor. The gates of all transistors are connected together. Therefore the checkerboard test structure is covered by a metal-2 grid, so that in each subchip the gate could be connected. The following Figure shows the connection of the power MOS-transistor inside a subchip. The drain of the power MOS-transistor is connected to the right test structure line "1" (metal-1) and the source is connected to the left test structure line "2" (metal-1). The gate connection can be seen at the right border of the subchip (metal-2).

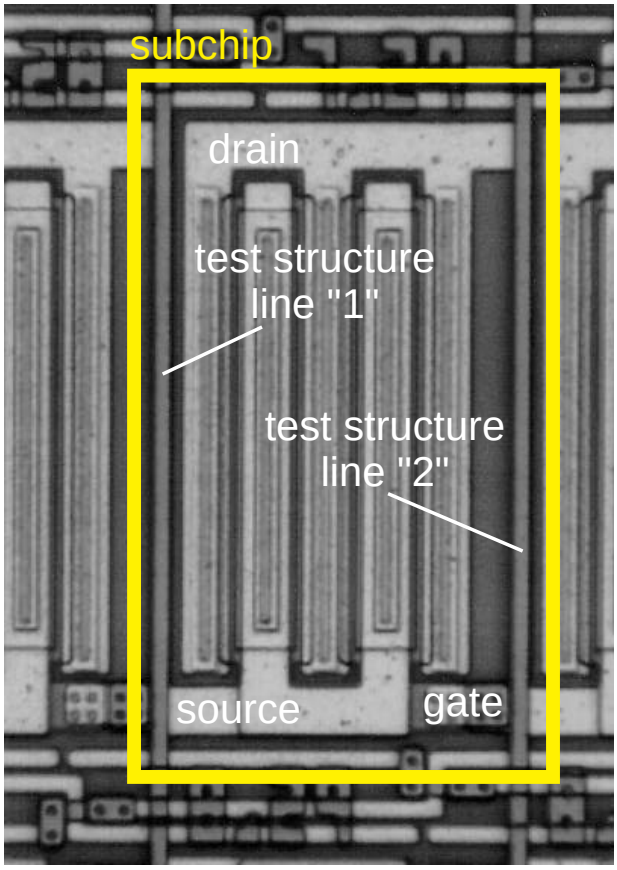


Fig. 3: Connection of the power MOS-transistor.

3 Test Procedure

The test structure will be measured using a digital tester with bidirectional channels. For the test procedure all gates are set to ground (0 V) which cuts off all transistors. For a complete test cycle a walking one will be sent to all test structure lines. So, a positive voltage $\mathbf{V_s}$ will be forced once to one specific test structure line, while its response is measured at all other test structure lines. The threshold voltage $\mathbf{V_{th}}$ of the digital tester is used to separate the logic **"0"** and logic **"1"** level of the measured response voltage.

Due to the walking one each transistor is tested twice - once by forcing the source and once by forcing the drain. According to the following table one of the four cases could happen during the measuring procedure.

case	gate	drain	source	detected type of fault
1	0	force "1"	measure "0"	no fault
	0	measure "0"	force "1"	
2	0	force "1"	measure "1"	short circuit current flow in one direction only (transistor fault)
	0	measure "0"	force "1"	
3	0	force "1"	measure "0"	short circuit current flow in one direction only (transistor fault)
	0	measure "1"	force "1"	
4	0	force "1"	measure "1"	short circuit (particle or transistor fault)
	0	measure "1"	force "1"	

Tab. 2: Possible measuring results. The gray shaded boxes represent the stimulus channels.

4 Localization Of Defects

If a short circuit occurs, two test structure lines are connected. Since we know in which subchips these two lines **(p,q)** are neighbored we can conclude to the transistor (subchip) that contains the defect. Figure 4 contains the localization procedure for $\mathbf{1 \le p < q \le m}$, where **m** stands for the total number of test structure lines. The functions used in the flowchart are given by the following table.

$$f(x) := \begin{cases} \frac{x}{2} & \text{if } \frac{x}{2} \in \mathbb{N} \ \wedge \ 1 < x \le m \\ m - \left\lfloor \frac{x-1}{2} \right\rfloor & \text{if } \frac{x+1}{2} \in \mathbb{N} \ \wedge \ 1 \le x < m \end{cases} \quad (2)$$

$$g(x) := \begin{cases} ((x-1) \bmod m) + 1 & \text{if } x > 0 \\ (x \bmod m) + m & \text{if } x \le 0 \end{cases} \quad (3)$$

Tab. 3: Functions used in the localization flowchart.

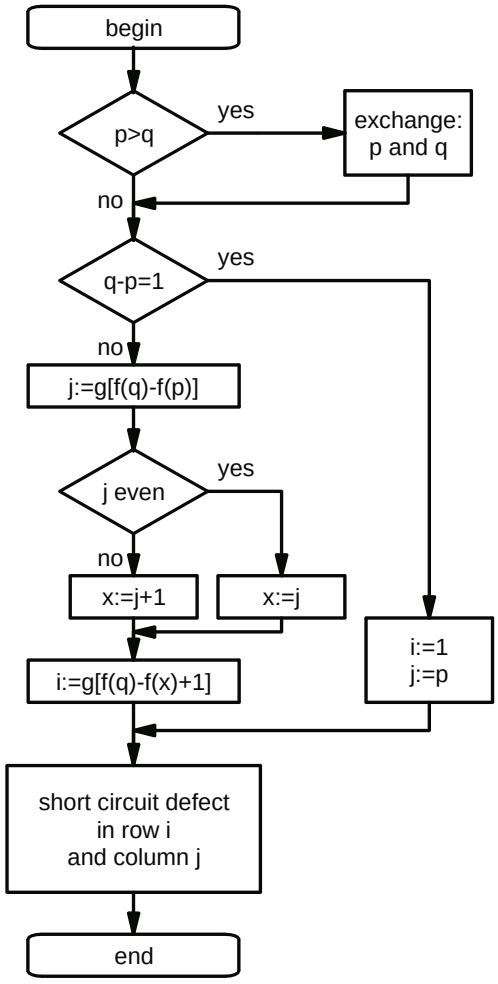


Fig. 4: Flowchart of localization procedure.

5 Automation Framework

The modified checkerboard test structure was developed with our unified automation framework to generate and analyze test chips for systematic and random defect monitoring. The test structure can be used to control VLSI-backend manufacturing, independent of specific semiconductor technology process steps. The framework is divided into the pre-manufacturing test chip generation and the post-manufacturing management of test procedures, data analysis, and statistical analysis which can be seen in the following Figure.

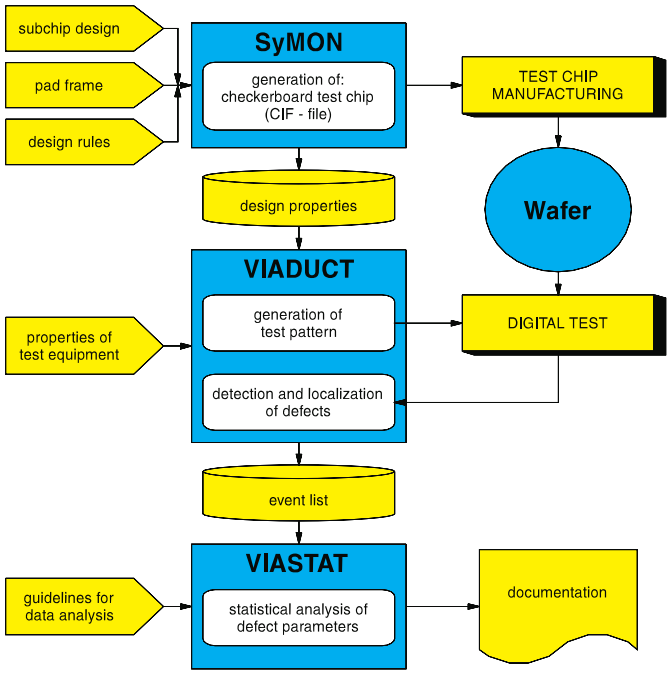


Fig. 5: Automation framework.

5.1 Generation of Checkerboard Test Chips Using SyMON

To investigate systematic problems as well as random defects, SyMON (**Sy**nthesis of **M**icroelectr**on**ic Test Chips) provides an automated design of Checkerboard Test Chips (**CTC**s) to control interconnection layers without requiring any active semiconductor devices and without any limitation to the number of layers. A CIF file will be generated according to layer definitions, design rules, and a given pad frame. Each subchip will be filled with a given subchip design or with standard test structures like meandrous lines or comb structures. Using SyMON, we designed the modified checkerboard test structure in just a few hours, which would normally have taken over 2 weeks.

5.2 Test Procedures and Data Analysis Using VIADUCT

During the manufacturing of the test chips, VIADUCT (**V**ersatile Automatic **I**dentification **A**nalysis of **D**efects from **U**ndesigned Open and Short **C**ircuits in **T**est Structures) will provide the preset of the tester parameters and the generation of the test pattern of a golden device. The manufactured test chips will be tested using a digital tester, so that product chips and test chips will be measured with the same tester equipment. If faults are detected, the tester yields a fail memory file comparing the measured data to the golden device data set. The analysis of the tester data provides the detection, identification and localization of defects. These information will be stored in a so-called *event list*. The measurement procedure and the event list generation just take a couple of minutes.

5.3 Statistical Data Analysis Using VIASTAT

According to guidelines how to perform defect statistics, VIASTAT provides statistical documentation about defect parameters. Also, the statistical data analysis just takes a couple of seconds. The following section gives an overview of possible statistical documentation.

6 Experimental Results

A modified checkerboard test structure was designed and manufactured at ELMOS in Dortmund, Germany, to control defect appearance in power MOS-transistors. This test structure has 630 distinguishable subchips each containing one power MOS-transistor. Figure 6 shows a detail view of the lower right corner of the manufactured test structure. Figure 7 shows a subchip containing one power MOS-transistor.

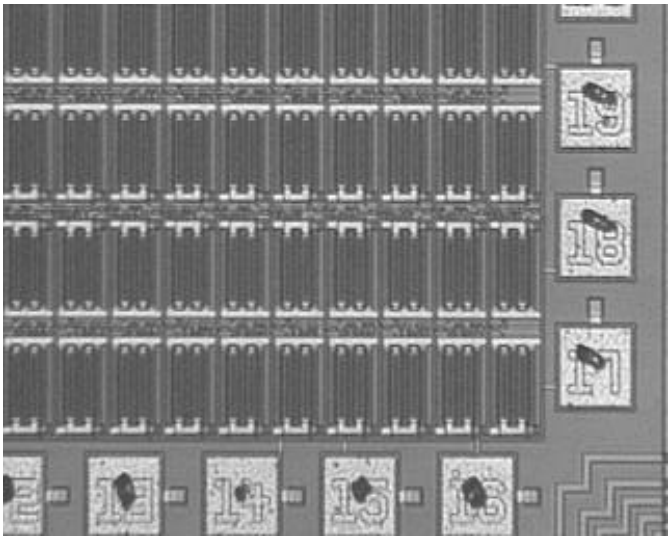


Fig. 6: Modified checkerboard test structure containing power MOS-transistors, manufactured at ELMOS.

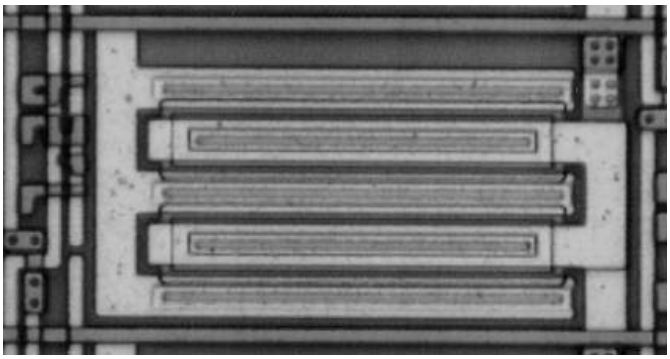


Fig. 7: One power MOS-transistor inside a subchip.

All in all, two lots with 25 wafers were manufactured each containing 109 modified checkerboard test structures. So, 3,433,500 large power MOS-transistors were analyzed using digital tester based measurements followed by a defect detection and localization procedure. The Figures 8 to 11 show detected defects causing short circuits. A wafermap containing four defects can be seen in Figure 12, where each defect is marked by "X" and the indices of the subchip row and column.

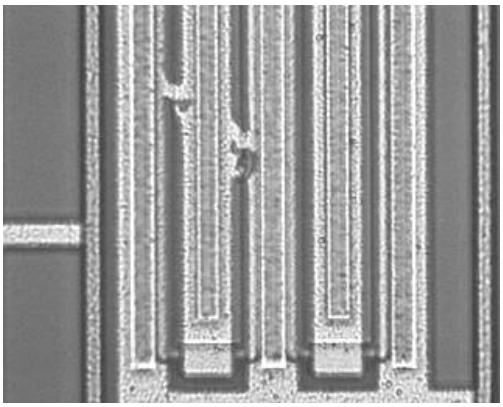


Fig. 8: Particle defect that caused a short circuit.

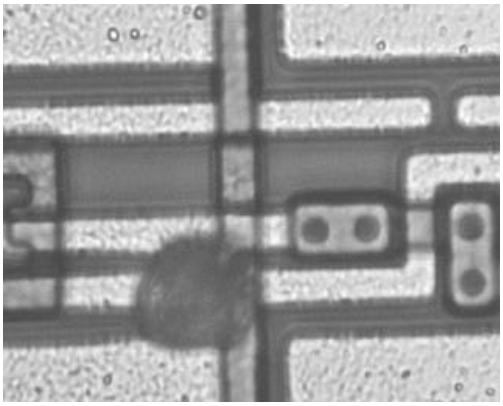


Fig. 9: Particle defect that caused a short circuit.

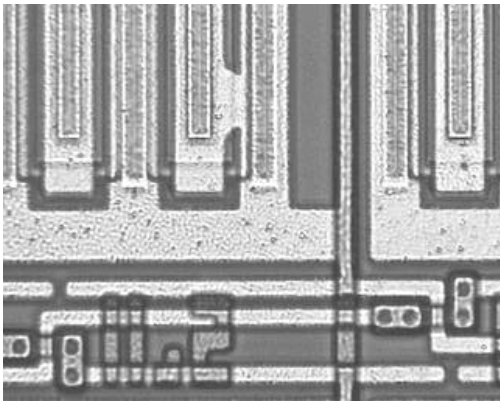


Fig. 10: Particle defect that caused a short circuit.

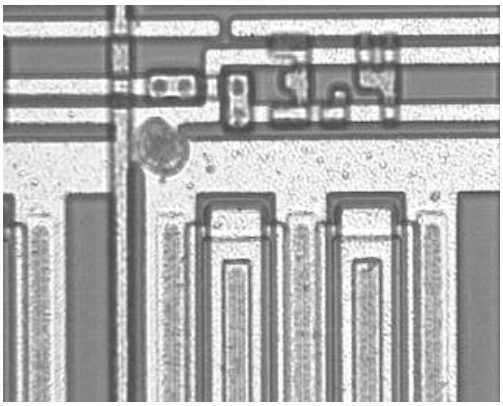


Fig. 11: Particle defect that caused a short circuit.

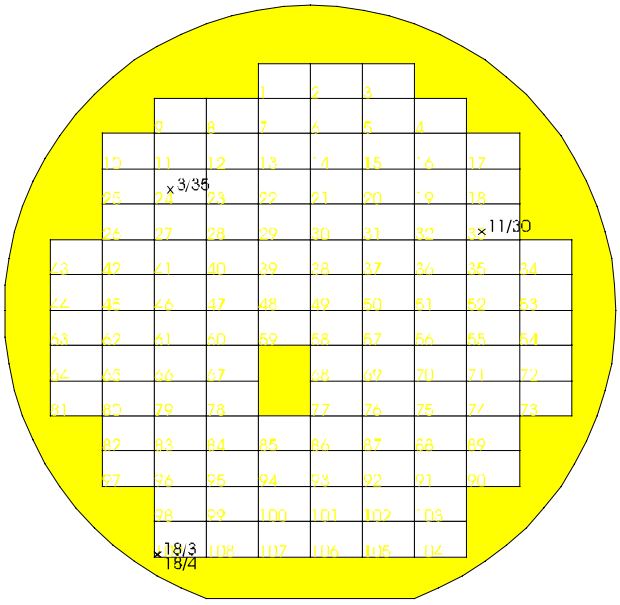


Fig. 12: Wafermap.

The following Figures 13 and 14 give the distribution of the digitally measured short circuits and the yield distribution of the test chips containing the modified checkerboard test structure of lot "A" and "B".

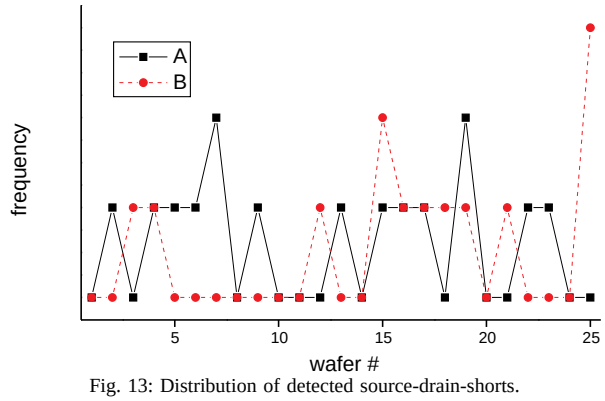


Fig. 13: Distribution of detected source-drain-shorts.

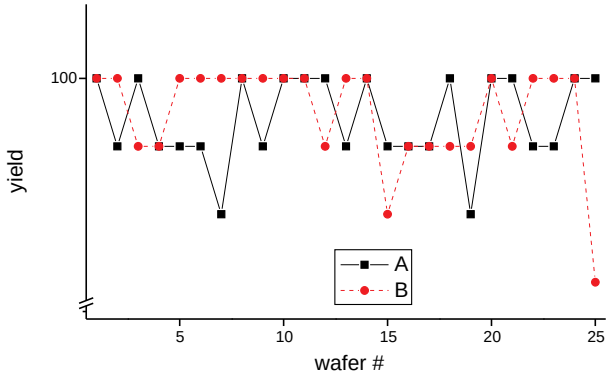


Fig. 14: Yield distribution of test chips.

All electrically detected short circuits were optically inspected. The following table gives the percentage of visible defects and not visible defects.

lot	visible	not visible
A	61 %	39 %
B	29 %	71 %

Tab. 4: Percentage of visible defects.

7 Conclusion

The described method to place power MOS-transistors inside checkered subchips enables an efficient inspection of short circuit defects inside the transistors. The modified checkerboard test structure guarantees a defect detection and a precise defect localization to enable a process classification and further optical defect inspection. The usage of a digital tester provides a fast measurement and data analysis procedure. The systematically designed checkerboard framework enables a machine-assisted generation of test chips.

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