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Control of Application Specific Interconnection on Gate Arrays Using an Active Checkerboard Test Structure

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***Abstract* — To control interconnection layers' integrity on application specific gate arrays, a novel active checkerboard test structure (ACTS) is presented. Here, the total gate array area will be divided into distinguishable small subchips, each containing basic layout elements like different sized serpentine lines or via strings. The precise separation and localization of these test structure elements inside the subchips enable versatile classification of interconnection faults, additional defect parameter extraction, and defect statistics.**

1 Introduction

Many chip manufacturers offer gate arrays as application specific integrated circuits (ASICs) if the total number of ordered chips is limited and a short time to market is required. Only layout elements inside the interconnection metal layers are responsible for customized circuit designs. So, one reason for chip specific yield is based on layout specific density of metal layers which will be determined using calculations of the critical area [Stap83], [Ferr85], [Maly90]. The other reason are defects that cause typical interconnection faults inside a layer (**intra**layer short) and also between adjacent layers (**inter**layer shorts). Generally basic geometrical layout elements like comb lines and serpentine lines are placed inside a "2 by N" probe-pad array to investigate defect appearance in interconnection process steps [IpSa77], [Bueh83], [LYWM86]. But, only boundary pads are available on gate arrays. So, especially designed test structures are required to separate defects inside interconnection process steps that provide:

- *Large defect sensitive area* to detect random defects even if the defect density is low.
- *Layer sensitive defect separation* to assign electrically detected defects to a specific layer.
- *Precise defect localization* to simplify optical defect parameter extraction.
- Minimize influence of *active semiconductor devices* in test structures especially to control backend process steps.

The following section gives the major principles to separate short circuits and open circuits inside a layer. Section 3 generalizes this procedure to numerous unlimited conducting layers and describes the principles to design a test structure on gate arrays. Section 4 deals with the principles to extract defect parameters. Finally some experimental results are presented.

2 Single-Layer Diode Checkerboard Test Structure

An obvious approach to the separation and localization of defects is to partition the chip area into a large number of subchips, each containing electrically separable test structure layout elements. The checkerboard test structure based on the 2D-permutation procedure described in [HeSt94], [HeWe95b] enables the separation and localization of short circuit defects inside a large chip area even if the number of boundary pads is limited.

equations to determine the elements of the 2D-matrix, where the number *m* of permutation lines has to be even

$$a[i,j]:=\begin{cases} j+2\cdot i-2 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i\le\frac{m-j+2}{2} \\ 2\cdot m-j-2\cdot i+3 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i>\frac{m-j+2}{2} \\ 2\cdot i-j-1 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i>\frac{j-1}{2} \\ j-2\cdot i \quad 2 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i\le\frac{j-1}{2} \end{cases} \quad (1)$$

i,j : row index, column index of the 2D-matrix

example for *m*=8 permutation lines

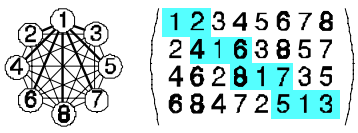

Fig. 1:
Left: Complete neighborhood graph introduced by [HeWe94] (nodes: Permutation lines; edges: Two nodes are connected by an edge if test structure elements connected to these permutation lines are adjacent anywhere inside a subchip with only nonconducting material between them).
Right: 2D-matrix
(gray boxes mark pairs to permutation line "1").

Tab. 1: 2D-permutation procedure.

An undesigned short circuit defect is only detectable between test structure layout objects connected to electrically distinguishable pads. So, all test structure layout objects that are

connected to one single pad are called a *permutation line*. To increase the number of separable short circuits, all possible ½·*m*·(*m*-1) neighborhood relationships of permutation lines have to be arranged inside a test chip in a way that each permutation line is once adjacent to every other permutation line with only nonconducting material between them. The 2D-permutation procedure described in Table 1 arranges all pairs of permutation lines without crossing each other in the rows of a matrix so that each pair of permutation lines exists once.

The diode checkerboard test structure (DCTS) of [HeWe94a] combines this technique with a diode array, so that also open circuits are separable and locatable inside large chip areas. Starting point is a diode-array on the left side of Figure 2. Here, the vertical lines are the *permutation lines* and the horizontal lines are called *collecting lines*, because they collect the voltage information send to a single permutation line. Now, every second line of diodes will be mirrored and moved which results in the construction in the middle of the figure. Finally the permutation lines have to be permutated corresponding to the 2D-permutation procedure.

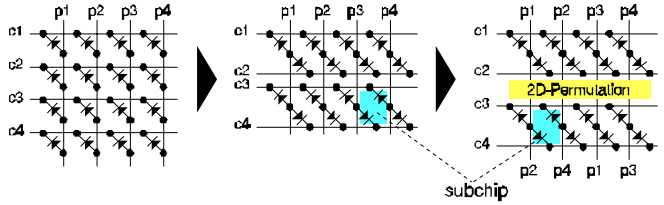

Fig. 2: Principle of the DCTS as a mixture of a diode array and the 2D permutation procedure (p: permutation line; c: collecting line).

But, this DCTS is limited to one permuted conducting layer. In addition, a checkerboard test structure on a gate array has to fulfill the following conditions:

- No *limitation of layers* to design a test chip in numerous permuted conducting interconnection metal layers.
- *Flexible design principle* to enable test chips on various designs of underlying gate arrays.
- The gate array *transistors* should be used instead of diodes.

3 Multi-Layer Active Checkerboard Test Structure

First the basic design principle will be described in the following subsection. Then, Subsection 3.2 introduces the usage of transistors to get distinguishable test structure lines inside the subchips. Subsection 3.3 deals with the arrangement of test structure layout objects inside a single subchip and finally some notes are given to connect boundary pads.

3.1 Design Principle without Limitation of Layers

To enable numerous layer test chip design, the distribution of permutation lines and collecting lines will be modified. The subset of permutation lines - designed in Figure 2 for just a single layer - has to be distributed among a given number *k* of layers in a way that each layer gets *m* independent permutation lines itself. According to Figure 2, the total number of collecting lines on the test chip still remains on *m*. So, the principle shown in Figure 2 will be individually done per layer.

Finally, all single layer designs will be arranged one above another where you have the same collecting lines for all layers but individual permutation lines per layer (ref. Fig. 3).

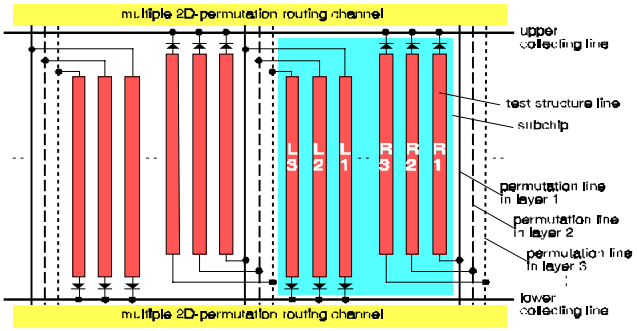

Fig. 3: Design principle of connections inside a subchip.

The checkered arrangement of subchips and the usage of active semiconductor devices is responsible for the naming of the **Active Checkerboard Test Structure (ACTS)**. There are two ways to implement a test structure line inside a layer of a subchip.

1. One test structure line is implemented between the right permutation line and the upper collecting line while the other test structure line is placed between the left permutation line and the lower collecting line (principle shown in Figure 3).

2. One test structure line is implemented between the right permutation line and the lower collecting line while the other test structure line is placed between the left permutation line and the upper collecting line.

It is important that the type of implementation is **identical** for all subchips inside a single subchip row. So, it is prohibited to implement different subchip columns as can be seen on the right side of Figure 4. But, it is permitted to change the arrangement per subchip row illustrated on the left side of Figure 4. Also, the arrangement can vary between different layers.

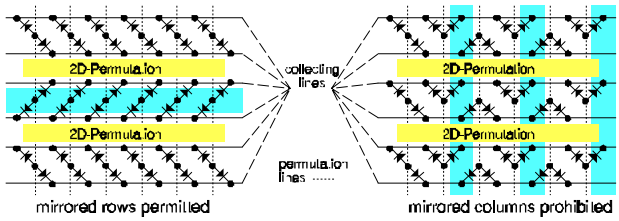

Fig. 4: Limits to arrange diodes per layer inside a subchip.

The stacked arrangement of permutation lines requires novel routing channels to connect all permutation lines between adjacent subchip rows. Based on the routing principle presented in [HeWe95b] an advanced channel design now enables multiple 2D permutation in a single routing channel based on 2 horizontal lines only. If at least 2 conducting layers are manufactured, all pads are completely connected to all routing layout elements of the conducting layers manufactured so far. For that, starting with the 2nd conducting metal layer, in-process measurements are possible after each metallization process step to eliminate wafers with systematic problems earliest possible. A library of these versatile routing channels is available at the Institute of Computer Design and Fault Tolerance. There are no

limits to the number of layers and also no limits to dimension the subchip size, so that an ACTS can be designed on every available gate array. For that, it is important that the extension of the smallest repeating unit of a gate array has to be a common divisor of the horizontal and vertical extension of a subchip, to enable identical test structure designs inside the subchips. This also includes the extension of implemented routing channels. So, sometimes it is better not to use all available pads to make full use of a given gate array area.

number *m* of permutation lines per layer	$m = \frac{n}{k + 1}$ where $\frac{m}{2} \in \mathbb{N}$ n : no. of pads k : no. of conducting interconnection layers	(2)
number of subchips	$\frac{m}{2} \cdot (m - 1)$	(3)
number of test structure lines	$k \cdot m \cdot (m - 1)$	(4)

Tab. 2: Dimension of ACTS.

3.2 Transistors instead of Diodes

Gate arrays consist of a regular arrangement of p-channel and n-channel transistors. The diodes of Figure 3 provide an unidirectional current flow to prevent the connection of the different test structure lines inside the subchips. Also, the switching character of transistors can select specific test structure lines. For that, the diodes will be replaced by transistors as can be seen in Figure 5. The number of collecting lines will be reduced to a single line between two subchip rows if both types of transistors are used. For that, the threshold voltage $-V_{th\_p}$ of the p-channel transistor should be similar to the threshold voltage V_{th_n} of the n-channel transistor. The reduced number of collecting lines increases the number of available permutation lines replacing Equation (2).

$$m = \frac{2 \cdot n - 1}{2 \cdot k + 1} \quad \text{where} \quad \frac{m}{2} \in \mathbb{N} \qquad \textbf{(5)}$$

The gate channel voltage in this circuit is small to prevent electrostatic discharge damage. Furthermore a series and parallel connection minimize the influence transistor faults might have on the defect data of the test structure lines. In some border-subchips, single transistor circuits are individually measurable without serpentine test structure lines.

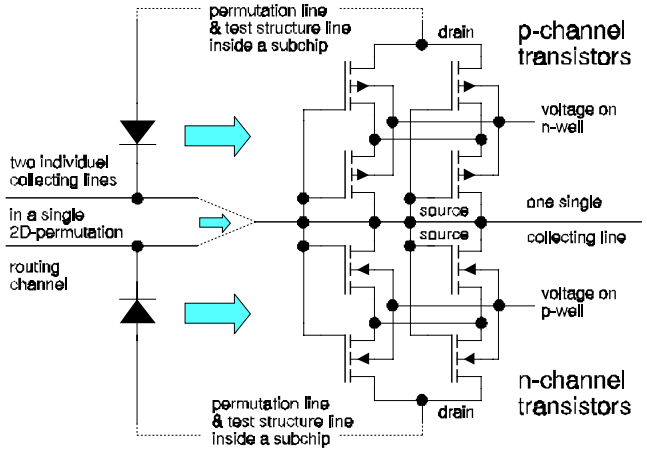

Fig. 5: Transistors replacing diodes.

A test structure line will be implemented between a permutation line and a single transistor circuit according to Figure 3. In this way, it is important that each permutation line is connected to each collecting line exactly twice - **once** via a n-channel transistor circuit and **once** via a p-channel transistor.

3.3 Contents of subchips

The test structure lines (vertical gray boxes inside a subchip of Figure 3) stand for defect sensitive basic test structures elements like different sized serpentine lines, via strings and contact strings. Even woven via strings described in [HeWe95a] are possible, because each test structure line may be adjacent to every other test structure line inside a subchip. Each subchip contains a unique set of connected permutation and collecting lines, so that all test structure layout elements inside the subchips are clearly distinguishable to detect open circuits.

But, to clearly detect short circuits inside a subchip, also all three-dimensional neighborhood relationships between test structure lines of different layers should be unique on the total area of the test chip. The following Figure 6 shows two neighborhood graphs of the test structure lines inside a subchip. The 2D-permutation procedure of Table 1 only provides a clear separation and localization of short circuits for the neighborhood relationships shown on the left neighborhood graph. So, the test structure elements should be arranged inside the subchip in a way that minimizes the neighborhood relationships shown in the right neighborhood graph. Often, this is of no consequence because defects that results in short circuits connect more than just two test structure lines. So, at least one edges of the left neighborhood graph is involved too.

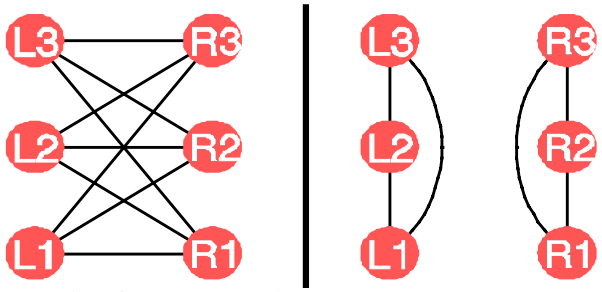

Fig. 6: left: Defined localization of adjacent test structure lines.
right: Undefined localization of adjacent test structure lines.

3.4 Connection to Pads

All collecting lines and each subset of permutation lines per layer have to be connected to given boundary pads. The index of the collecting lines increases top to bottom starting with the value "1". Each collecting line will only be placed at the left and right boundaries, so that they should connect to given boundary pads first. The connection of the permutation lines to the pads will be done, using the indices of the 2D-matrix, calculated using Equation (1). Each permutation line is placed twice at a boundary row of the 2D-matrix and once at a boundary column of the 2D-matrix. Typically, the pad routing requires about the same area than an average 2D-permutation routing channel between two subchip rows. So, more than 90% of the area inside the boundary pads will be completely filled with defect sensitive structures.

4 Defect Parameter Extraction

Generally, open and short circuits are detectable, testing the resistance between different pads. Since we know in which subchip the defective test structure lines are designed, we can conclude to the subchip containing the defect. The localization enables an optical inspection to also determine the causes why a defect has occurred.

To measure the resistance of the test structures, a digital tester will be used, because the electrical test must only decide whether there is a defect or not. If both types of transistors are connected to a single collecting line, different types of faults will be detected using the following three measurement steps:

1. To detect short circuits, cut off all transistors while sending a walking one to all permutation lines. So a stimulus voltage V_{s_perm} is once forced to each permutation line while its response voltage is measured at all other permutation lines (ref. [HeWe95b]). A negative load-voltage is required for all measuring tester channels.
2. To detect open circuits in test structure lines connected to n-channel-transistors, cut off all p-channel-transistors while sending a walking one to all n-channel-transistors. So a stimulus voltage V_{s_col} is once forced to the n-channel-transistors of each collecting line while its response voltage is measured at all permutation lines. A negative load-voltage is required for all measuring tester channels.
3. To detect open circuits in test structure lines connected to p-channel-transistors, cut off all n-channel-transistors while sending a walking one to all p-channel-transistors. This is possible only by using inverse binary stimulus and response values or voltages, respectively. So an inverse stimulus voltage V_{s_col} is once forced to the p-channel-transistors of each collecting line while its response voltage is measured at all permutation lines. A positive load-voltage is required for all measuring tester channels.

The following table gives some voltage calculations for the measurement procedure where $V_{th} := -V_{th\_p} \approx V_{th\_n}$ (V_{th_p}: threshold voltage of the p-channel transistor; V_{th_n}: threshold voltage of the n-channel transistor).

measuring sequence	p-chan.-transistor	n-chan.-transistor	voltage on p-well V_p	voltage on n-well V_n	collecting voltage V_{s_col}	permutation voltage V_{s_perm}
1: shorts	off	off	0V	$2\cdot V_{th}$	V_{th}	$V_n + V_{p\_n}$
2: opens at n-chan.-tr.	off	off	0V	$2\cdot V_{th}$	V_{th}	measure only
	off	on			$2.66\cdot V_{th}$	
3: opens at p-chan.-tr.	off	off	$0.66\cdot V_{th}$	$2.66\cdot V_{th}$	$1.66\cdot V_{th}$	measure only
	on	off			0V	

Tab. 3: Measuring sequences where gray shaded boxes mark inverse binary values (V_{p_n}: process specific voltage drop at p-n diode).

The tester threshold voltage is set corresponding to [HeWe95c] including the additional drain-source voltage drop at the transistor circuit of Figure 5. The measured binary values are assigned to possible defects according to Table 4.

measuring sequence	measured value		expected value in reference data	detected type of defect
	voltage	binary		
1: shorts & 2: opens at n-chan.-tr.	$V_{measured} \geq V_{threshold}$	1	0	short circuit
	$V_{measured} \geq V_{threshold}$	1	1	defectless
	$V_{measured} < V_{threshold}$	0	0	defectless
	$V_{measured} < V_{threshold}$	0	1	open circuit
3: opens at n-chan.-tr.	$V_{measured} < V_{threshold}$	0	0*	defectless
	$V_{measured} \geq V_{threshold}$	1	0*	open circuit

Tab. 4: Data conversion where gray shaded boxes mark inverse binary values (* binary "1" is never expected).

If unexpected fail values occur during a measuring step, the complete data set of the test chip will be stored in a fail memory matrix. Then, the row and column indices have to be brought into line with the increasing indices of the permutation lines (ref. corresponding 2D-matrix) or collecting lines, respectively. Now, [HeWe95d] offer algorithms to extract all fail values of a measured response matrix, if the models of [HeWe94] are used to describe test structures. In addition to that, the following table extracts the permutation line index and the collecting line index of all fail values.

measuring sequence	columns of measured response matrix	rows of measured response matrix
1: shorts	permutation line index: p $(1 \leq p \leq m\cdot k)$	permutation line index: q $(1 \leq q \leq m\cdot k)$
2: opens at n-chan.-tr. & 3: opens at p-chan.-tr.	permutation line index: p $(1 \leq p \leq m\cdot k)$	collecting line index: q $(1 \leq q \leq \frac{m}{2}+1)$

Tab. 5: Extraction of fail value pair indices (p,q) out of the three measured response data matrices corresponding to the three measuring steps.

Each permutation line is implemented in a specific layer. So, the layers L_p and L_q will be determined for all fail value pairs (p,q) where L_q:=0 is chosen for collecting lines. Finally, each pair (p,q) will be localized inside a test chip using the flow charts of Figure 7, 8 and 9 where the following equations occur.

$$f(x) := \begin{cases} \frac{x}{2} & \text{if } \frac{x}{2} \in \mathbb{N} \ \wedge \ 1 < x \leq m \\ m - \left\lfloor \frac{x-1}{2} \right\rfloor & \text{if } \frac{x+1}{2} \in \mathbb{N} \ \wedge \ 1 \leq x < m \end{cases} \quad \textbf{(6)}$$

$$h(x) = \overline{f}(x) := \begin{cases} 2 \cdot x & \text{if } 0 < x \leq \frac{m}{2} \\ (m-x)\cdot 2 - 1 & \text{if } \frac{m}{2} < x \leq m \end{cases} \quad \textbf{(7)}$$

$$g(x) := \begin{cases} ((x-1) \bmod m) - 1 & \text{if } x > 0 \\ (x \bmod m) \dotplus m & \text{if } x \leq 0 \end{cases} \quad \textbf{(8)}$$

Tab. 6: Functions used in the localization sub-routines.

The gray shaded branch in the flow chart of Figure 7 corresponds to n-channel transistors connected to the upper collecting line of a subchip. If p-channel transistors are connected to the upper collecting line, the gray shaded branch has to be replaced by "open at p-channel transistor".

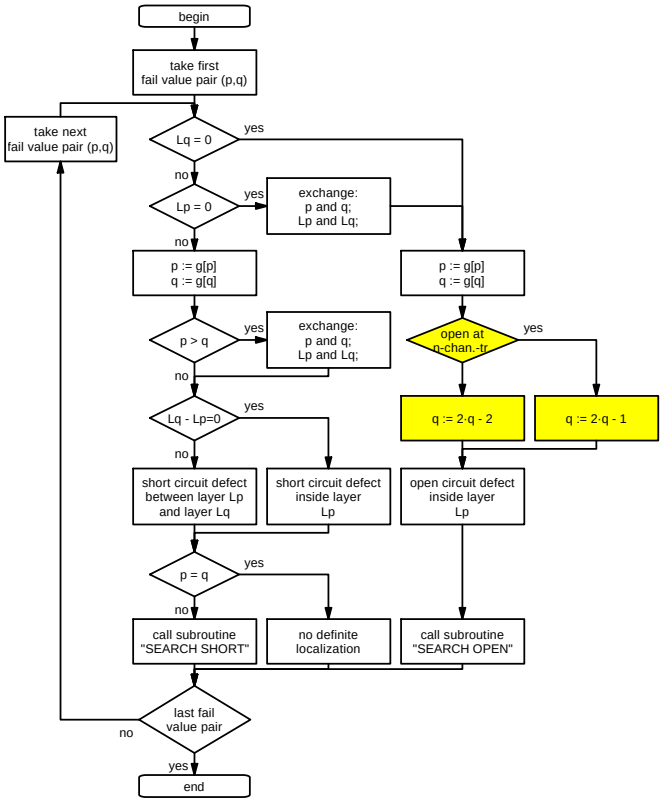

Fig. 7: Procedure to localize defects that results in electrically detectable faults

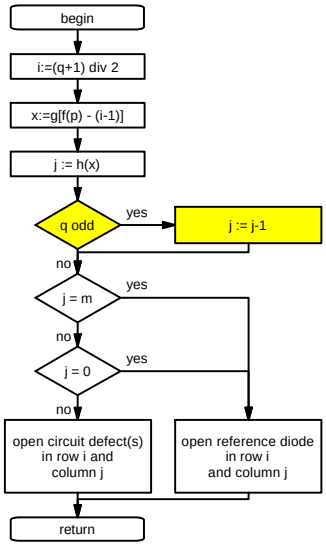

Fig. 8: Sub-routine "SEARCH OPEN".

The gray shaded branch in the flow chart of Figure 8 will apply, if inside a layer of a subchip one test structure line is implemented between the right permutation line and the lower collecting line while the other test structure line is placed between the left permutation line and the upper collecting line. If one test structure line is implemented between the right permutation line and the upper collecting line while the other test structure line is placed between the left permutation line and the lower permutation line, the gray shaded branch has to be replaced by "q even".

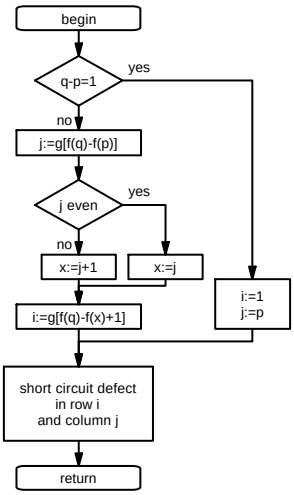

Fig. 9: Sub-routine "SEARCH SHORT".

5 Experimental Results

At Thesys Gesellschaft für Mikroelektronik mbH in Erfurt Germany, an active checkerboard test structure was designed to control defect appearance in a single poly, double metal 1.5µm HCMOS 6-inch p-well process. The ACTS has 72 permutation lines (36 lines per interconnection metal layer), and a total of 18 collecting lines connected to transistors of the underlying gate array. The gate array THA10075 consists of 37485 gates (299880 transistors) on a chip size of 11.7mm x 11.7mm. All in all 630 distinguishable subchips with an active area of 100mm² contain serpentine lines, via and contact strings. Figure 10 shows details of test structure elements inside a subchip and Figure 11 a part of the test chip layout. If a defect occurs and causes a fault, test structure lines are interrupted or connected to each other. Since we know in which subchips the test structure lines are implemented, we can conclude to the subchips containing the defects.

Figures 12 and 13 give the distribution of the digitally measured defects among the different layers. Following [HeWe95a], the influence of short circuits on data of open circuits was investigated again. In Figure 14 can be seen, that 18% of all open circuits have short circuits nearby, but only 6% of all short circuits have neighbored open circuits. Finally Figures 15 and 16 show two localized defects.

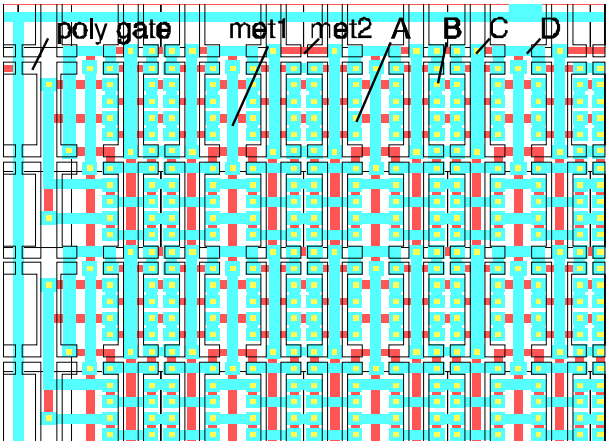

Fig. 10: Four via strings (A, B, C, D) of a weave test structure inside a subchip.

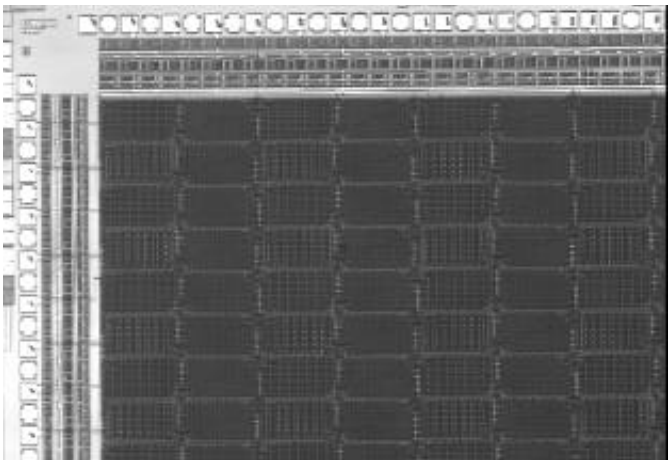

Fig. 11: Upper left Corner of a manufactured ACTS.

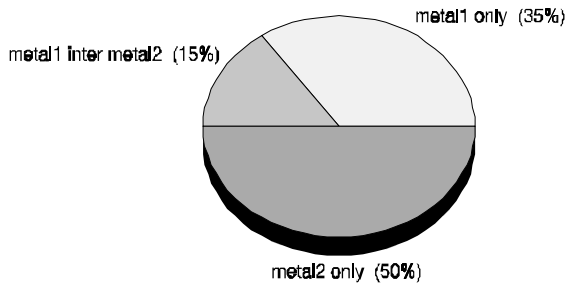

Fig. 12: Distribution of electrically detected short circuits inside and inbetween 2-metal layers.

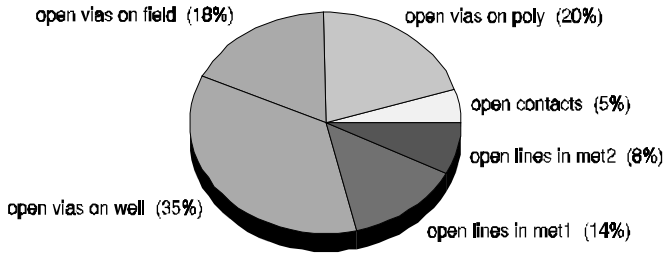

Fig. 13: Distribution of electrically detected open circuits inside and inbetween 2-metal layers.

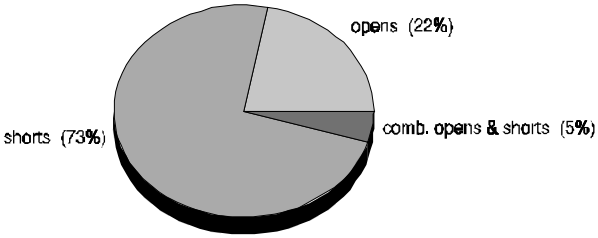

Fig. 14: Distribution of isolated and combined faults.

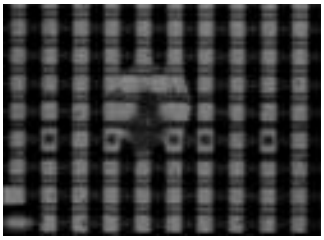

Fig. 15: Detected short circuit defect.

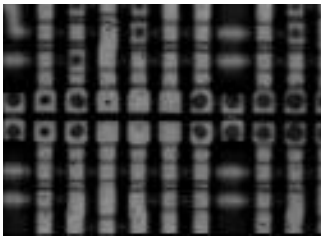

Fig. 16: Detected open vias.

6 Conclusion

The described method to place test structure layout elements inside checkered subchips enables an efficient inspection of defects that occur anywhere in the application specific interconnection of gate arrays. The flexible dimension of the active checkerboard test structure provides a universal design on any underlying gate array structure. There are no requirements on the transistor design and the number of interconnection layers is unlimited. The ACTS detects systematic problems as well as random defects due to its extensive defect sensitive area. However, the multiple 2D permutation procedure guarantees a precise separation and localization of interconnection faults to enable the classification of process specific defects and further optical defect inspection. The systematically designed checkerboard framework enables a machine-assisted generation of test chips.

Acknowledgment

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