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Resistance Modeling of Test Structures for Accurate Fault Detection in Backend Process Steps Using a Digital Tester

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***Abstract* – A methodology is presented to enable the usage of a digital tester for an accurate detection of open circuits as well as short circuits in test structures to control backend process steps. Therefore, a novel graph model will be introduced to calculate the resistance values of test structures containing defects. The paper gives a comprehensive description of the procedure to adjust the tester parameters to those test structures.**

1 Introduction

To measure the resistance of a test structure, commonly analog or DC parametric tester are applied, using a measurement frequency below 1 Hz [BCKJ91], [MiHF92], [RoBF92]. In the context of this paper, an electrical test must only decide whether the test structure contains a defect or not. So in general a digital tester should be sufficient. Hence, a tester is required with bidirectional channels which can send a stimulus voltage V_s as well as receive a response voltage V_m.

A digital tester has important advantages. First, the measurement frequency of a digital tester is normally many times higher than the frequency used during analog 2- or 4-point measurements. So the evaluation of test structures can be much faster. Furthermore, every measured value needs only one bit which reduces the storage requirements. Also, a data reduction is possible already during the electrical measurements since the measured binary data can be easily compared to reference values. Finally, using a digital tester simplifies in-line process control because test chips and product chips can be measured in the same way and with the same measuring equipment.

The following section deals with the modeling of test structures. Section 3 describes the way a digital tester works and section 4 presents the adaption of the digital tester to test structures. Section 5 gives some experimental results and Section 6 concludes the paper.

2 Modeling Of Test Structures

To enable the defect detection out of binary tester data sets, it is necessary to model the geometry of layout objects inside a test chip with a *geometry graph* [HeWe94]. A node stands for a measuring point. An edge represents all conductive layout objects (**conductive component (CC)**) between measuring points. All conductive components that are connected to each other are called a **maximal conductive component (MCC)**. The parameter *n* stands for the number of nodes per MCC. Normally, test structures for backend process steps consist of numerous MCCs placed over the whole chip area. The MCCs are replaced by lines formed as combs or serpentines and strings of contacts or vias [IpSa77], [Bueh83], [LYWM86]. The following figure shows some test structures and their geometry graphs.

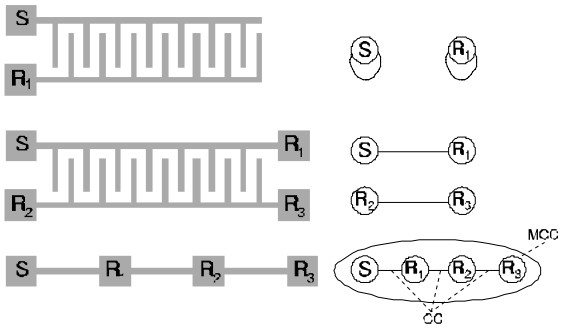


Fig. 1: Test structures used in backend process steps and their geometry graph.

A binary tester data set is the result of measured voltages, currents, and resistances inside test structures. Therefore, also the resistance information of each CC has to be modeled. For that, the geometry graph will be expanded to the *resistance graph*. Here, each edge is labeled with the resistance of the corresponding CC. In other words, the resistance graph is the abstraction of the equivalent circuit diagram of the test structure or the geometry graph with new labeled edges. The following figure shows the mentioned graphs. For the adaption of the digital tester we need the resistance information of each

CC (R_c) as well as the equivalent circuit diagram of the test structure in case of the presence of defects.

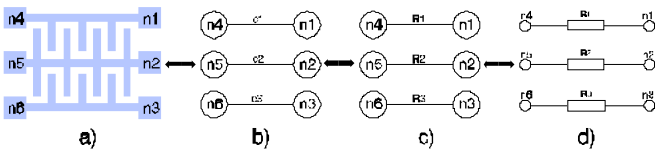


Fig. 2: a) Test structure. b) Geometry graph. c) Resistance graph. d) Equivalent circuit diagram.

3 The Digital Tester

For the measurement procedure a digital tester with bidirectional tester channels is required (ref. [HeWe94]). A bidirectional channel in stimulus mode consists of a voltage source and an internal resistance R_s. A bidirectional channel in response mode consists of a level sense at a terminating resistor R_r (ref. Figure 3). A test structure without any active semiconductor devices like transistors or diodes will completely be tested using a "walking one" as test vector set over all pads. So, every bidirectional tester channel that is connected to a pad of the test structure is once in the stimulus mode while every other channel is in the response mode. To get accurate results from the digital tester, the threshold voltage V_t and stimulus voltage V_s has to be adjusted.

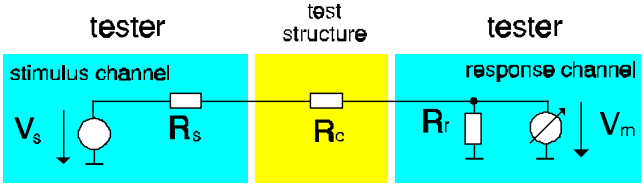


Fig. 3: The digital tester.

The threshold voltage V_t separates the two defined tester states: Logic "0" and logic "1". A measured voltage V_m below the threshold voltage at a response channel of the digital tester is assigned to logic "0". In contrast to that, a voltage above the threshold voltage is assigned to logic "1". Dependent on the expected logical value, the measured voltage V_m can be assigned to a detected open circuit or short circuit, respectively. The following figure shows the dependency of detected defects on the measured voltage V_m.

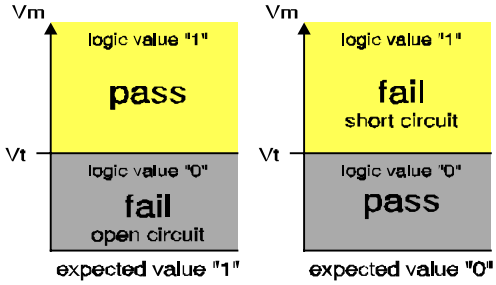


Fig. 4: Detected defects dependent on the measured voltage V_m at a response channel according to the threshold voltage V_t.

If a digital tester will be used to detect defects inside test structures, the tester properties must fulfill the requirements summarized in the following table.

channel	bidirectional
stimulus voltage V_s	adjustable
threshold voltage V_t	adjustable
measuring frequency f_{max}	adjustable (10kHz - 100kHz)
terminating resistor R_r (channel in response mode)	has to be known
internal resistance R_s (channel in stimulus mode)	has to be known

Tab. 1: Digital tester properties.

4 Adaption Of The Digital Tester

To achieve the adaption of the tester, we make some assumptions that are suitable for test structures especially used in backend process steps.

- Only types of test structures corresponding to the *three basic geometry graphs* shown in Figure 1 are considered, but there is no limitation on the number of MCCs (k) and number of nodes (n), respectively.
- The *resistance of a short circuit* has to be smaller than the resistance of a CC ($R_{short} << R_c$).
- The *resistance of a CC* has to be smaller than the resistance of the terminating resistor R_r. ($R_c << R_r$).
- Nodes which are labeled with S (stimulus node) or R (response node) could be replaced by the *equivalent circuit diagram of the stimulus or response channel* (ref. Figure 3).

Before the threshold voltage will be calculated, the values of the CC resistance R_c, the stimulus voltage V_s and measuring frequency f_m have to be determined. This will be done in the following sub-sections.

4.1 Determination of the CC Resistance R_c

The resistance R_c of a single CC (conductive component designed between two measuring points) can be determined with the following equation. For the calculation of the line resistance a sum over all layers is necessary, because $R_\square$ is a layer specific resistance. The experimental results will show that this way of calculating R_C is sufficient.

$$R_c = \alpha \cdot \left(\sum^{layer} \frac{R_\square \cdot L}{W} + \sum R_{via} + \sum R_{contact} \right) \quad \textbf{(1)}$$

L, W : length and width of a test structure line
$R_\square$: layer specific square resistance
R_{via}, $R_{contact}$: via and contact resistance
α : manufacturing tolerance (α>1)

4.2 Determination of the Stimulus Voltage V_s

The stimulus voltage V_s will set to a value corresponding to the maximal current I_{max} and the smallest resistance R_{C_min} of all CCs inside the test structure. So, I_{max} and R_{C_min} have not be determined out of the same CC.

$$V_s = R_{c\_min} \cdot 3 \cdot I_{max} \quad (2)$$

I_{max} : maximal current according to existing design rules

The peak current is approximately 3 times the average current I_{max} introduced in existing design rules. This can be done, because the current flow through the test structure is limited to a very short period of time (10µs to 100µs). To determine I_{max}, it is necessary to calculate the average current flow through each test structure line dimension per layer, each via size and each contact size, separately. The smallest of these current values has to be selected and set to I_{max} in equation 2.

4.3 Determination of the Measuring Frequency f_m

To avoid capacitive influences, the measuring frequency f_m has to be adjusted to a value between 10kHz and 100kHz. Experimental results have shown that this value of f_m is suitable [HeSt94], [HeWe94a].

4.4 Determination of the Threshold Voltage V_t

Before the threshold voltage can be calculated, the geometry graph of the test structure containing a defect has to be analyzed.

4.4.1 The Maximal Resistance Path (MRP)

One or more short circuits connect different MCCs. These short circuits build a new geometry graph (ref. Figure 5). The way how short circuits connect different MCCs is unknown. So the resistance values of the edges of the corresponding resistance graph cannot be determined. Figure 5a, b and c illustrates three possibilities, how a short circuit can connect different MCCs. Inside these graphs, all additional edges are marked as dashed lines.

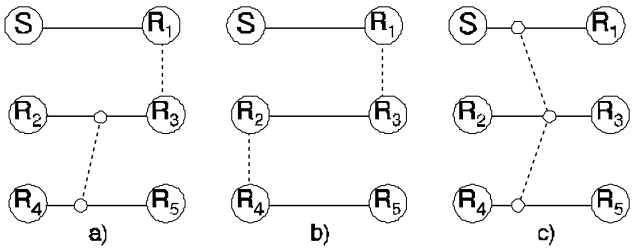


Fig. 5: Possibilities to connect different MCCs.

To detect these short circuits, at least one response channel has to indicate a binary "1" value. For that the adjusted threshold voltage V_t has to be smaller than the measured voltage V_m. In order to adjust the threshold voltage V_t, it is necessary to determine the *smallest* value of all possible measured response voltages. Using a walking one as test vector set to detect short circuits, it is sufficient only to consider the *direct short circuit path* between a stimulus node and a response node without passing other (measuring) nodes of the resistance graph. To get the smallest response voltage, it is necessary to determine the worst case resistance situation on this direct short circuit path, even if also open circuits occur and short circuits connects more than just two MCCs.

For that, five different cases have to be investigated.

(a1) A direct short circuit path starts or ends in a node of the resistance graph. This node is located at the end of an MCC (ref. case (a1) of Figure 6).

(a2) A direct short circuit path starts or ends in a node of the resistance graph. This node is located in the middle of an MCC (ref. (a2) of Figure 6).

(b1) A direct short circuit path starts or ends in the middle between two nodes, so that the resistance between the short circuit and each node is equal ½·R_c. This edge is located near the end of an MCC (ref. (b1) of Figure 6).

(b2) A direct short circuit path starts or ends in the middle between two nodes, so that the resistance between the short circuit and each node is equal ½·R_c. This edge is located in the middle of an MCC (ref. (b2) of Figure 6).

(c1) A direct short circuit path starts or ends at the far end of an edge, which is separated from the next node by an open circuit. The separated node is located at the end of an MCC (ref. (c1) of Figure 6).

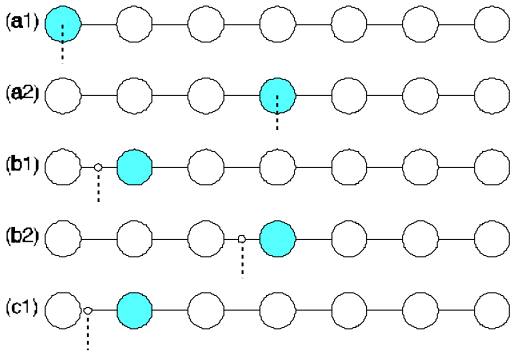


Fig. 6: Location of short circuits, where the gray nodes represent the selected stimulus or response node, respectively.

Now, all possible combinations of the placement of the direct short circuit path between the stimulus and response nodes have to be compared. As a result of this, the smallest voltage V_m will be measured at a response node placed in case (b2) while the stimulus voltage V_s is driven via a node placed in case (c1). If a short circuit connects more than two MCCs, the connection to the third and all other MCCs has to be modeled as a direct short circuit path in case (a2) to get the smallest possible response voltage. This construction will be named **maximal resistance path (MRP)**.

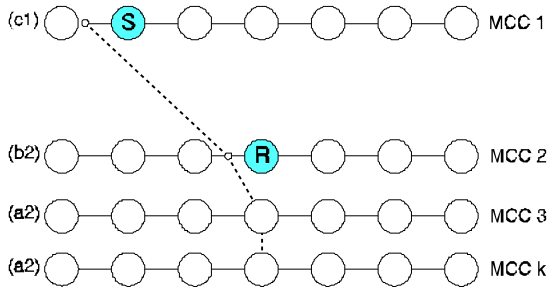


Fig. 7: Maximal resistance path (MRP), where all white nodes are also response nodes.

If all these types of complex short circuits will be taken into account, open circuits will be detected too. Open circuits only separate two connected nodes inside a single MCC and therefore open circuits will be measured between measuring points of one single MCC only.

4.4.2 The Threshold Voltage

To detect all possible open and short circuits, the threshold voltage V_t has to be adjusted to the MRP of Figure 7. For that, the graph of the MRP (ref. Figure 8, left) will be transformed into the equivalent circuit diagram. To calculate the threshold voltage, the recurrent network as can be seen on the right side of Figure 8 has to be determined for any values of k (number of connected MCCs), n (number of nodes per MCC), the stimulus voltage V_s, the internal resistance R_s, the CC resistance R_c and the terminating resistor R_r.

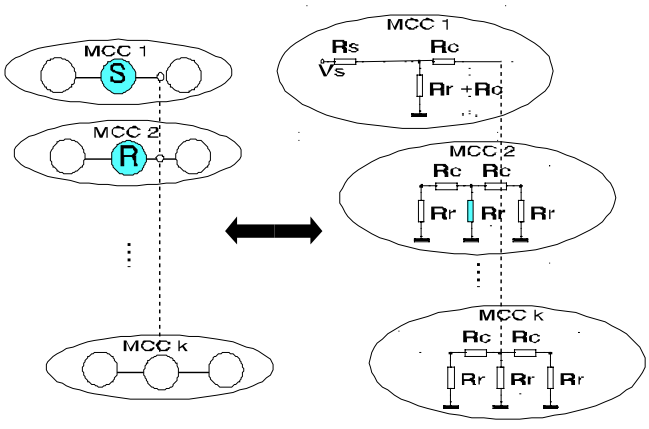


Fig. 8: Equivalent circuit diagram of k connected MCCs with n=3 nodes.

This can be done with the following flow charts where the basic algorithm is implemented as can be seen in the flow chart of Figure 9. The calculation of a recurrent network is implemented in the sub-procedure **NETWORK** (ref. flow chart of Figure 10). This algorithm calculates the total resistance (*r_total*) and the resistance ratio (V_t) of a single recurrent network with a series resistance *r_ser* and a parallel resistance *r_par*. E. g. the parameters of a network drawn on the right side of Figure 11 will be calculated by calling this sub-procedure twice.

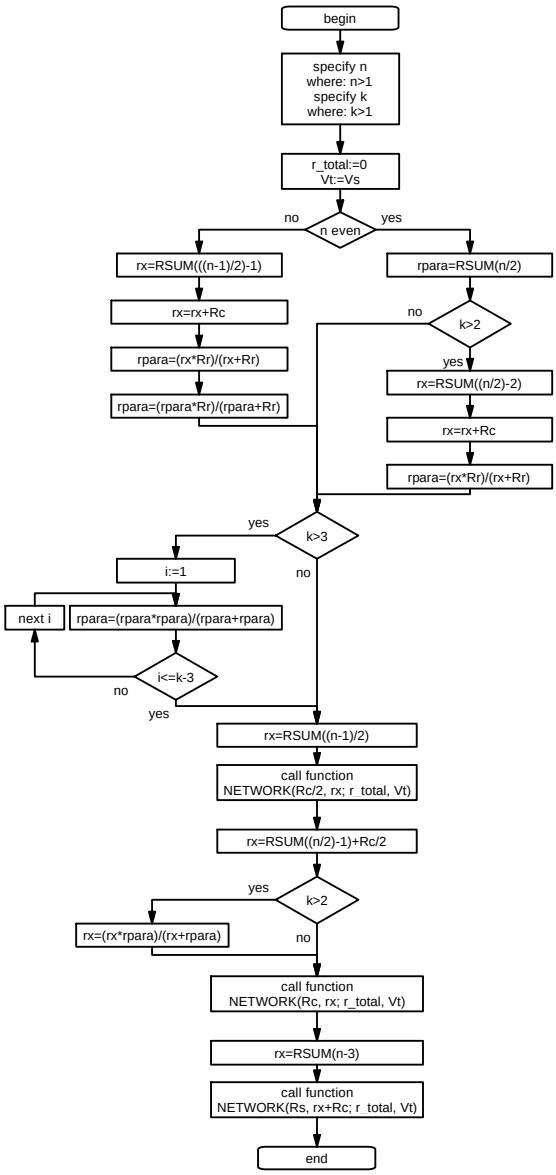


Fig. 9: Basic algorithm to calculate the threshold voltage.

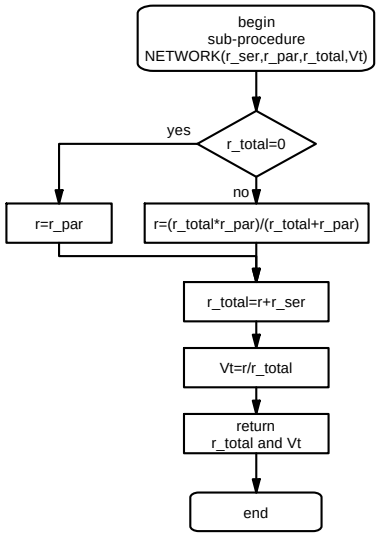


Fig. 10: Sub-procedure NETWORK.

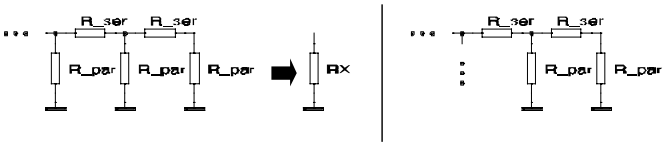


Fig. 11: Basic resistance networks.

The total resistance R_X of a network as can be seen on the left side of Figure 11 will be calculated by calling the sub-procedure **RSUM** (ref. flow chart of figure 12). The parameter *j* specifies the number of series resistances *r_ser*. The series resistance *r_ser* itself is set to the value of the CC resistance R_c and the parallel resistance *r_par* is set to the value of the terminating resistor R_r.

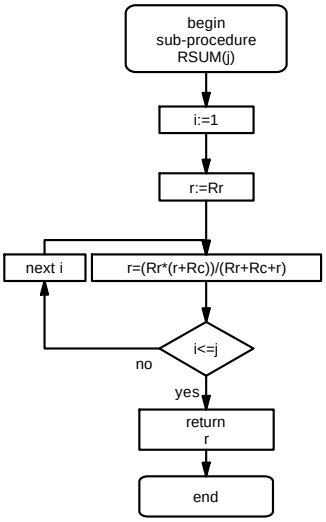


Fig. 12: Sub-procedure RSUM.

The following figure shows some calculated values of threshold voltage V_t according to different numbers of nodes (*n*) and different numbers of connected MCCs (*k*). In this case the stimulus voltage V_s, the internal resistance R_s, the CC resistance R_c and the terminating resistor R_r are constant.

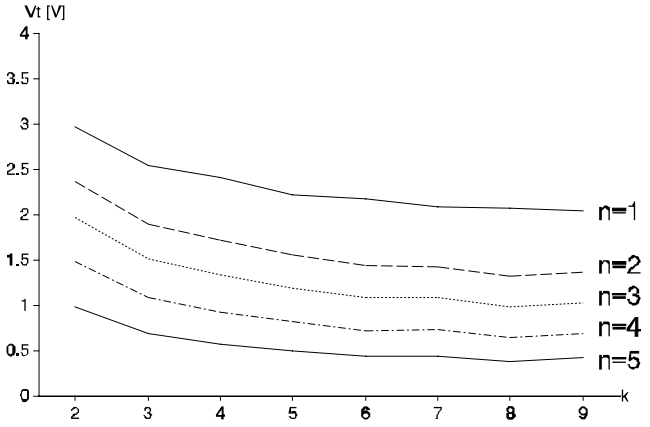


Fig. 13: Calculation of V_t for V_s=5V, R_s=100Ω, R_c=2kΩ and R_r=10kΩ and different numbers of k and n.

The number of edges on each side of the "middle" response node is not equal according to an even or odd number *n* of nodes per MCC. As a result of this, a zigzag pitch of the lines can be seen. In case of open circuits, the threshold voltage should be set to a value of at least *k*=2.

5 Experimental Results

About 800 test structures with different line width, space and length were manufactured at the *Institute for Microelectronics Stuttgart, Germany* to validate the digital measuring procedure and the modeling of the resistance graph. The following table summarizes the distribution of the different sized lines.

name of line	width [µm]	length [mm]	calculated resistance [kΩ] (α=1.0)	calculated resistance [kΩ] (α=1.15)
6e	3.0	187.2	3.74	4.30
5e	2.0	187.2	5.62	6.46
4e	1.5	187.2	7.49	8.61
3e	1.0	187.2	11.23	12.91
2e	0.75	187.2	14.98	17.23
1e	0.5	187.2	22.46	25.83
5d	2.0	89.8	2.69	3.09
4d	1.5	89.8	3.59	4.13
3d	1.0	89.8	5.39	6.20
2d	0.75	89.8	7.18	8.26
1d	0.5	89.8	10.78	12.40
4c	1.5	40.6	1.62	1.86
3c	1.0	40.6	2.44	2.81
2c	0.75	40.6	3.25	3.74
1c	0.5	40.6	4.87	5.60
3b	1.0	15.8	0.95	1.09
2b	0.75	15.8	1.26	1.45
1b	0.5	15.8	1.90	2.19
2a	0.75	3.3	0.26	0.30
1a	0.5	3.3	0.40	0.46

Tab. 2: Distribution of 20 different sized test structure lines inside a manufactured test chip.

To validate the adaption procedure, all lines were measured three times. First an analog tester was used to determine the distribution of the line resistances. Figure 14 shows the distribution of the measured values of one specific line dimension.

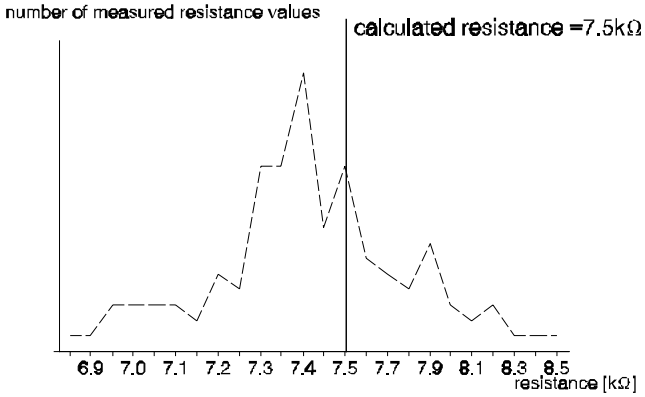


Fig. 14: Distribution of measured resistance values for line "4e".

Secondly, the digital tester was used to determine the defects, where the calculated CC resistance values of Table 2 (ref. also vertical line of Figure 14) were the starting point of the tester adaption procedure. Thirdly, a final analog test, which now also aims on defects, yields exactly the same number of defects for all different sized lines. The following figure shows the distribution of detected open circuit defects according to the line length.

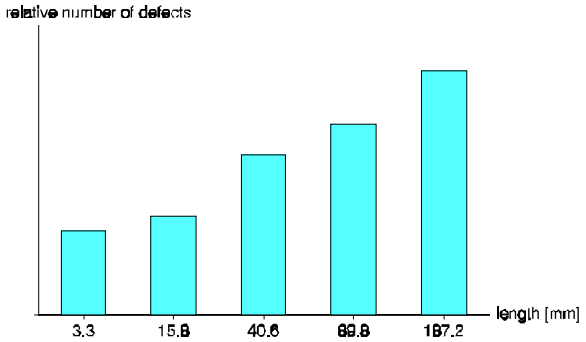
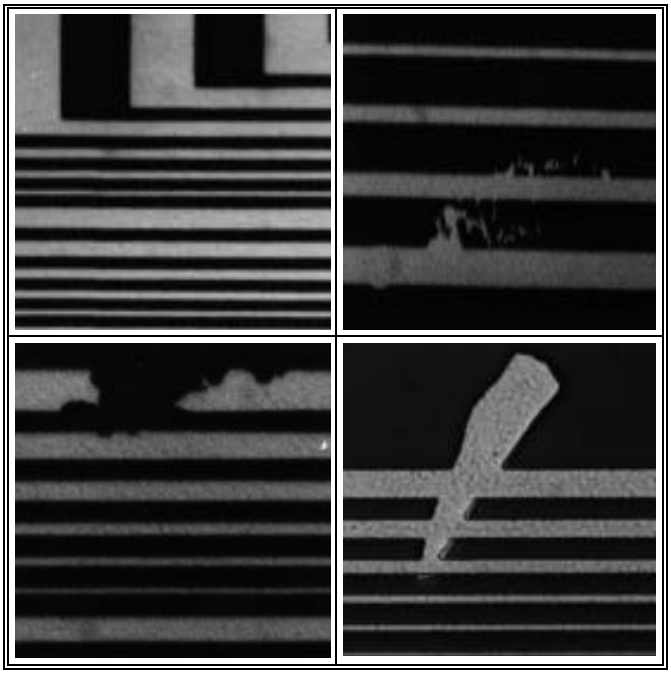


Fig. 15: Distribution of detected open circuits in 0,5µm lines dependent on their length.

Finally Table 3 gives some test structure details and electrically detected defects.



Tab. 3: Detail view of the test structures and some electrically detected defects.

6 Conclusion

The described methodology enables the use of a digital tester for accurate fault detection. The major advantage is a massive reduction of measurement data which provide a simplified and fast machine-assisted data analysis (ref. [HeWe94]).

The adjustment of the tester parameters requires a precise calculation of the resistances inside test structures containing defects. The introduced adjustment procedures base on novel test structure resistance models and the determination of the worst case measurement voltages. Finally, presented calculation algorithms enable a machine assisted tester adjustment.

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