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Influence of Short Circuits on Data of Contact & Via Open Circuits Determined by a Novel Weave Test Structure

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***Abstract* — The influence that short circuits have on contact hole open circuits and via hole open circuits in regular string test structures will be investigated. To detect open circuits as well as short circuits in adjacent conducting layers of backend process steps, a novel *weave test structure* (WTS) is presented. Numerous contact strings or via strings are arranged inside boundary pads like a woven piece of cloth. So, also short circuits between different strings are electrically detectable.**

1 Introduction

Due to the increasing number of conducting polysilicon and metal layers, especially designed test structures without any active semiconductor devices gain more importance to control layers' integrity manufactured in backend process steps. Large defect sensitive areas are required to determine systematic problems as well as random defects even if the defect density is very low. Two major types of defects are responsible for the malfunction of chips:

- *Short circuits* inside a layer (**intra**layer short) and also between adjacent layers (**inter**layer shorts).
- Contact hole *open circuits* (open contacts) and via hole *open circuits* (open vias).

[Hess93], [HeSt94] and [HeWe95] describe an efficient method to investigate short circuits using different types of checkerboard test structures, where comb lines are arranged in an array of distinguishable subchips. The diode checkerboard test structure introduced by [HeWe94a] enables also the detection of open circuits, but here additional diodes are required. [IpSa77] and [MiHF92] uses strings of vias or contacts to investigate open contacts and open vias. But these strings cannot detect any shorts that might cover open failures. So, our goal is the development of a test structure which aims on open contacts, open vias, and short circuits anywhere in two adjacent conducting layers.

The following Section 2 describes the design principle of the novel weave test structure. Section 3 deals with the defect parameter extraction procedures. After that, test structure measurement results are presented in Section 4 that show the influence of short circuits on measured data of test structures designed to detect open contacts and vias.

2 Principle Design of a Weave Test Structure

The novel weave test structure bases on a crosswise arrangement of contact strings or via strings, respectively. The following figure shows on the left side the connection of the vias in the structures used by [IpSa77] and [MiHF92]. On the right side, our approach to connect the vias can be seen.

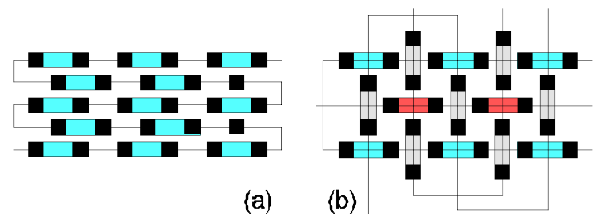

Fig. 1: (a) Via string used by [IpSa77] and [MiHF92].
(b) Novel woven via strings.

Due to this arrangement the via strings have to cross each other in a woven way illustrated in the following figure.

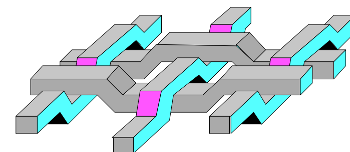

Fig. 2: Woven arrangement of different contact strings or via strings, respectively.

The strings will be arranged inside given boundary pads, where each string will be placed between two pads to enable an electrical test to detect open and short circuits. So, for a given frame of p boundary pads a maximum of $n=\frac{p}{2}$ electrically isolated strings will be implemented inside a test chip. For that, all n strings (index: $\{1,2,..,\frac{p}{2}\}$) will be divided into h_{max}

horizontal strings (index $h \in \{1,2,..,m\}$) and v_{max} vertical strings (index $v \in \{m+1,m+2,..,n\}$), where $h_{max}+v_{max}=n$ and $1<m<n$. Figure 3 separately shows the horizontal and vertical strings. The different line styles mark electrically isolated strings.

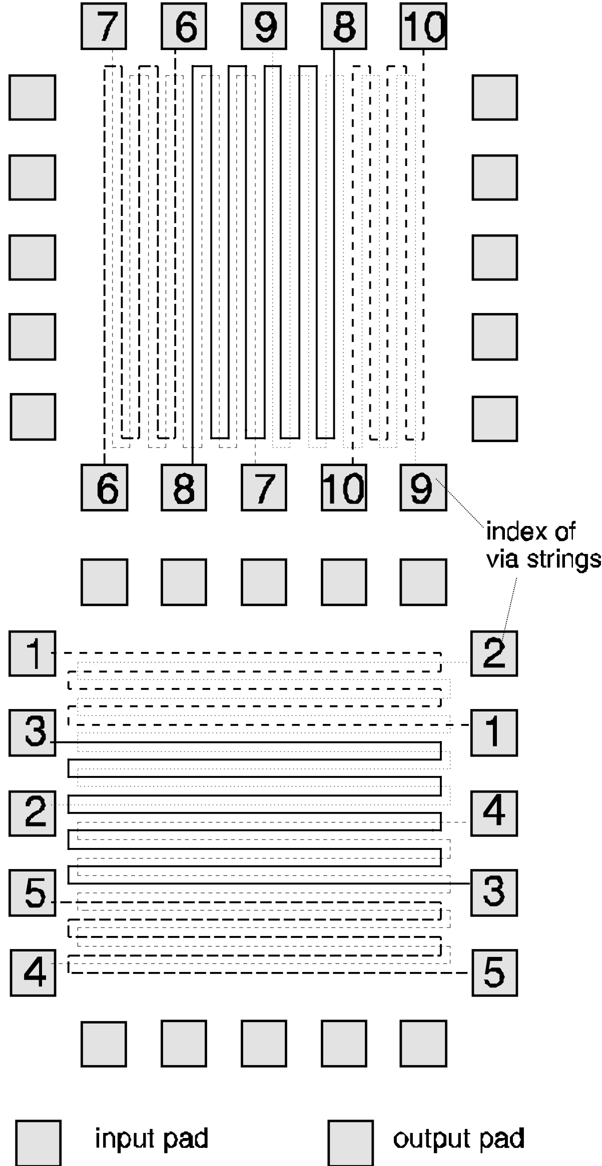

Fig. 3: Top: Vertical via strings.
Bottom: Horizontal via strings.

All horizontal and all vertical strings will be woven as illustrated on the left side of Figure 4. This procedure to arrange the strings yields subchips each containing a unique set of adjacent and electrically isolated strings. The right side of Figure 4 shows the subchip array and its row indices r and column indices c. All indices (h,v & r,c) increases left to right or top to bottom, respectively. So, for example the subchip $(r,c)=(2,3)$ contains the horizontal strings $h=2$ & $h=3$ as well as the vertical strings $v=8$ & $v=9$. The total number of subchips is $(h_{max}-1)\cdot(v_{max}-1)$. Not only quadratic arrangements but also rectangular arrangements inside boundary pads could be designed.

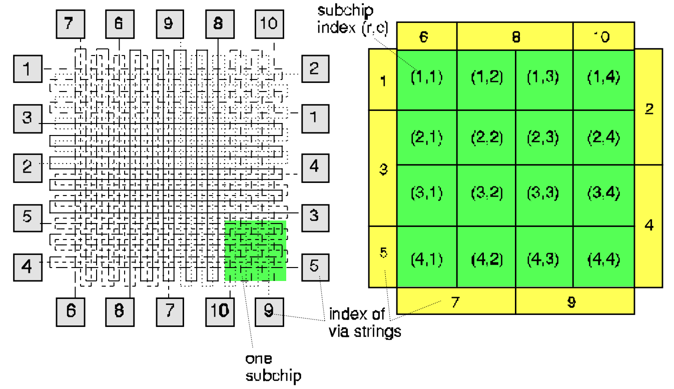

Fig. 4: Left side: Vertical & horizontal via strings.
Right side: Subchips and their containing electrically isolated strings.

3 Defect Parameter Extraction

Generally, open and short circuits are detectable, testing the resistance between different pads or strings, respectively. Since we know in which subchip the affected strings are designed, we can conclude to the subchip containing the defect. The localization facilitates an optical inspection to determine also the defect containing layer.

To measure the resistance of the test structures, a digital tester will be used, because the electrical test must only decide whether there is a defect or not. The measured values are assigned to possible defects according to the following table.

measured value		expected value in reference data	detected type of defect
voltage	binary		
$V_{measured} < V_{threshold}$	0	0	defectless
$V_{measured} < V_{threshold}$	0	1	open circuit
$V_{measured} \geq V_{threshold}$	1	0	short circuit
$V_{measured} \geq V_{threshold}$	1	1	defectless

Tab. 1: Data conversion (adjustment of threshold voltage ref. [HeWe95c]).

To detect the defects inside a test chip, a "walking-one" over all input-pads is sufficient while measuring the voltage responses at all output-pads.

```
          string index (j)
          00000000011111111112
          12345678901234567890
     i= 01 10000000000000000000  * horizontal
        02 01000000000000000000  * via strings
        03 00100000000000000000  *
        04 00010000000000000000  *
        05 00001000000000000000  *
        06 00000100000000000000  *
        07 00000010000000000000  *
        08 00000001000000000000  *
        09 00000000100000000000  *
        10 00000000010000000000  *
        11 00000000001000000000  # vertical
        12 00000000000100000000  # via strings
        13 00000000000010000000  #
        14 00000000000001000000  #
        15 00000000000000100000  #
        16 00000000000000010000  #
        17 00000000000000001000  #
        18 00000000000000000100  #
        19 00000000000000000010  #
        20 00000000000000000001  #
```

Tab. 2: Reference data of a defectless test chip where $n=20$ and $m=10$.

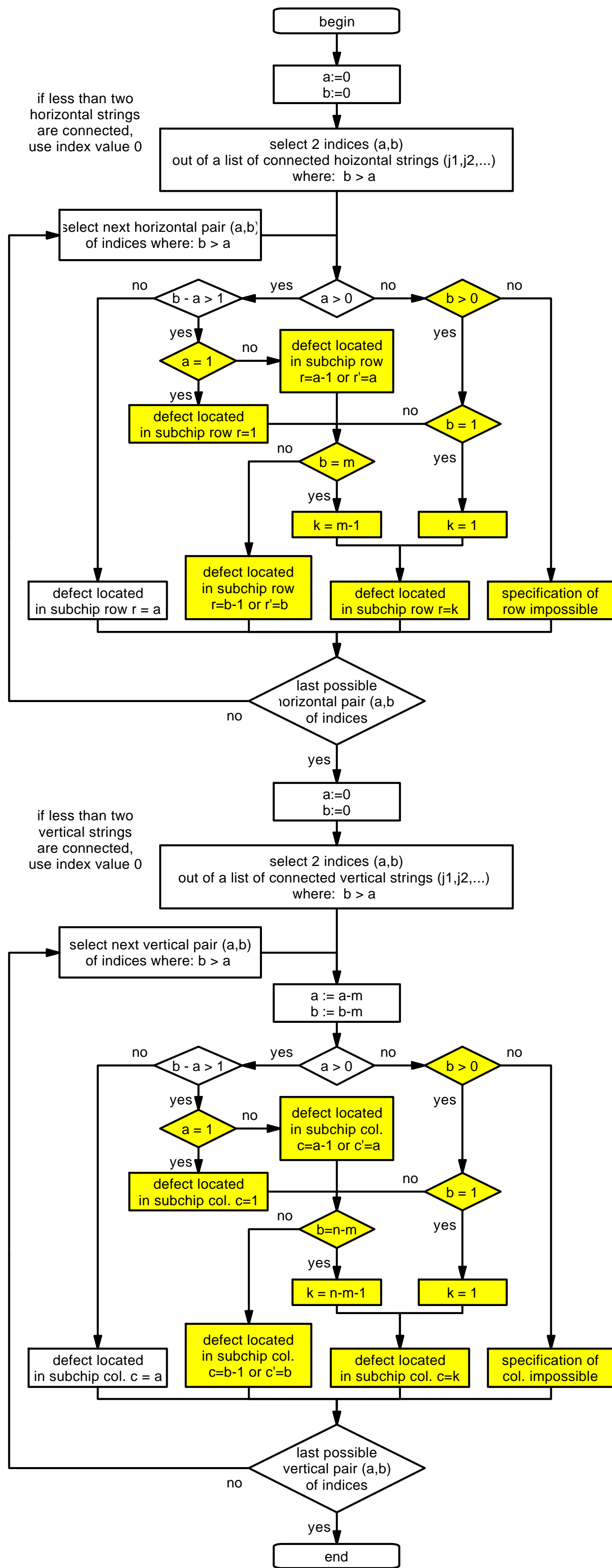

Fig. 5: Principle to localize defects, that results in short circuits.

Table 2 contains a defectless reference response data set, where the row index i represents the test vector number and the column index j represents the sequence of output pads brought into line with the increasing string index. So, the string index (h or v) is always equal to the data set index j.

If unexpected "1" values occur in one row i of a measured response data set, the defect or defects that result in this measured short circuit will be localized using the flow chart of Figure 5. Here, the column indices $j1,j2,...$ of all "1" values in row i have to be taken into account. For that, it is necessary to determine two subsets, one containing all indices $j \leq m$ of the connected horizontal strings and the other containing all indices $j > m$ of the connected vertical strings. Then the subchip indices (r,c) of all possible pairs of indices (a,b) have to be determined separately. The white boxes represent the major path inside the flow chart, while the other paths handle special cases with a probability of occurrence less than 10%.

If an implemented via string connection between two pads is interrupted inside a test chip, an unexpected "0" value occurs in its measured response data set. The defect which results in the measured open circuit will be localized using the flow chart of Figure 6.

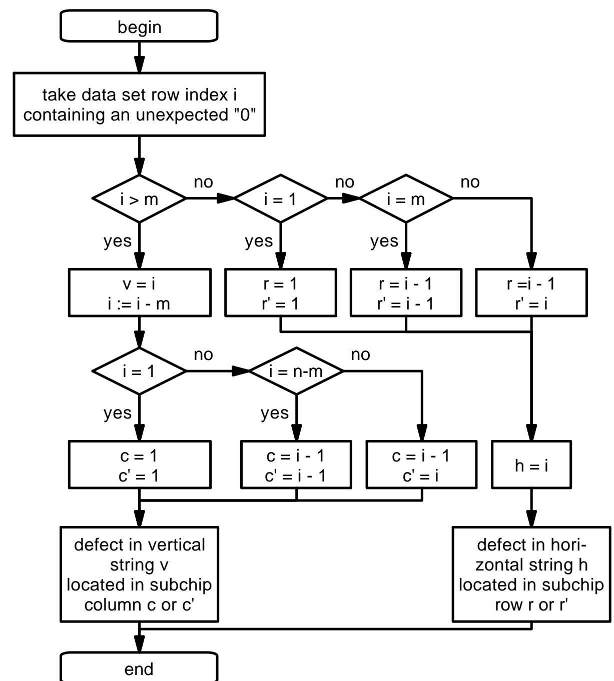

Fig. 6: Principle to localize defects, that results in open circuits.

4 Influence of Shorts on Measured Data

A weave test structure (WTS) was manufactured at the Institute for Microelectronics Stuttgart (IMS). The lithography steps were performed via electron beam direct write. The WTS has 30 via strings arranged inside 60 boundary pads, where each string has equally designed vias. All in all 8 different via dimensions were implemented as listed in Table 3. The following figure shows a part of this WTS, while some details of the woven strings can be seen in Figure 8.

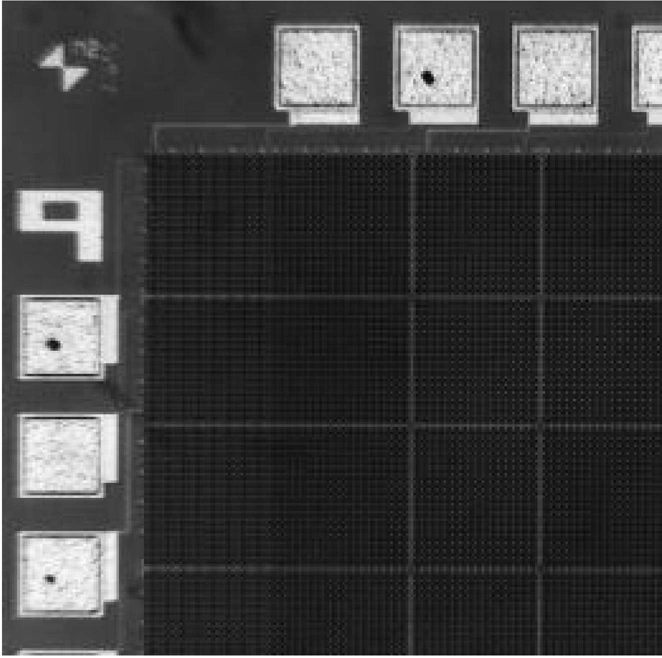

Fig. 7: Upper left corner of a WTS.

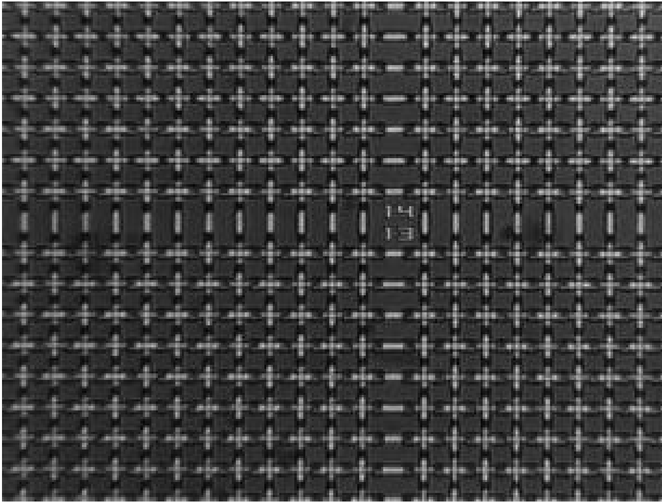

Fig. 8: Detail view of a WTS.

To get data that are comparable to each other, the number of implemented strings per size and the number of vias per string (length factor β) have to be taken into account. To determine the length factor β, the following procedure should be used: First, we determine the relative frequency f_i of interrupted strings individually counted per string for one specific via size (e. g. 1 interrupted string out of 6 implemented strings per chip yields f_i=0.17). Then we individually count the number of interrupts per series connection of two strings. Finally, we individually determine the number of interrupts per series connection of three strings. Figure 9 shows the influence of the number of vias per string on the relative frequency of interrupted via strings.

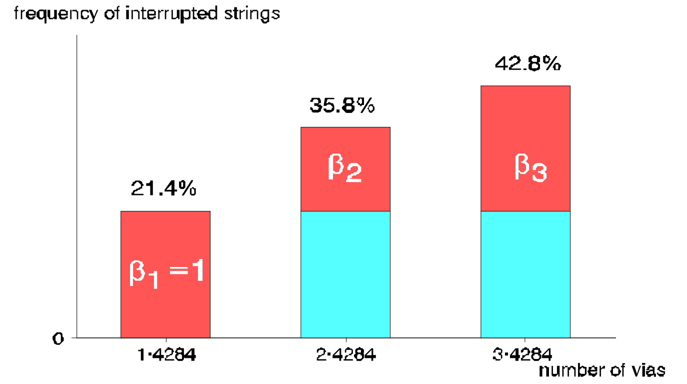

Fig. 9: Distribution of interrupted strings dependent on the number of vias (sum of percentage values = 100%).

This distribution follows the expected binomial distribution, where the relative frequency increases with a factor β=*1.67* while the number of vias per string is doubled. So, for 2268 vias per string compared with 4486 vias per string, the length factor β will be

$$\beta = \frac{1.67}{2} \cdot \frac{4284}{2268} = 1.58 \qquad \textbf{(1)}$$

Calculations based on other via sizes yield similar results (*1.5* < β < *1.7*). To compare all via strings inside the test chip, the shorter strings with 2268 vias are given β=*1.6*. According to the number of vias per string and the frequency of implemented strings per chip q_c, the absolute number of interrupted strings will be multiplied with the total weight factor α:

$$\alpha = \frac{\beta}{q_c} \qquad \textbf{(2)}$$

The following table summarizes the test structure properties.

via size vb [µm]	via size vl [µm]	via overlap vob [µm]	via overlap vol [µm]	number of vias per string	freq. of strings per chip q_c	length factor β	weight factor α
2.5	2.5	1.0	1.5	4284	6	1	0.17
2.0	2.0	1.0	1.0	4284	6	1	0.17
1.5	2.5	0.75	0.75	4284	5	1	0.20
1.5	2.0	0.5	0.5	4284	4	1	0.25
1.5	1.5	0.5	0.5	4284	3	1	0.33
1.0	2.0	0.5	0.5	4284	2	1	0.50
1.0	1.5	0.5	0.5	2268	2	1.6	0.80
1.0	1.0	0.5	0.5	2268	2	1.6	0.80

Tab. 3: Dimensions of manufactured via strings.

Using the weight factor α, Figure 10 gives the distribution of open vias dependent on the via size.

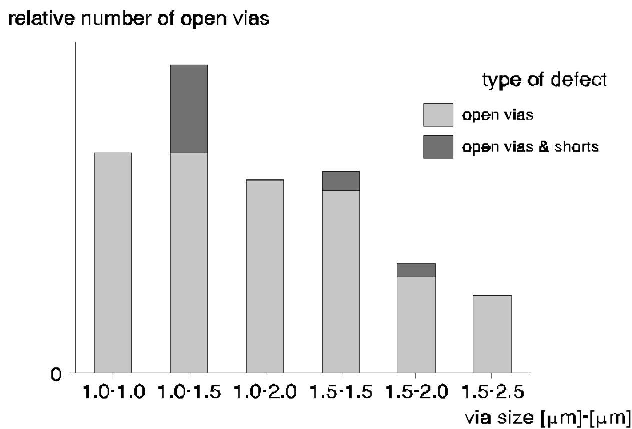

Fig. 10: Distribution of detected open vias.

The dark gray shaded bars represent all interrupted strings that are connected to other strings by a short circuit. If a test structure is used, that ignores such effects, the results may only give the distribution of the light gray bars. Figure 11 summarizes the relative error if short circuit defects will cover open circuits in via strings. The Figures 12 and 13 show two localized short circuit defects.

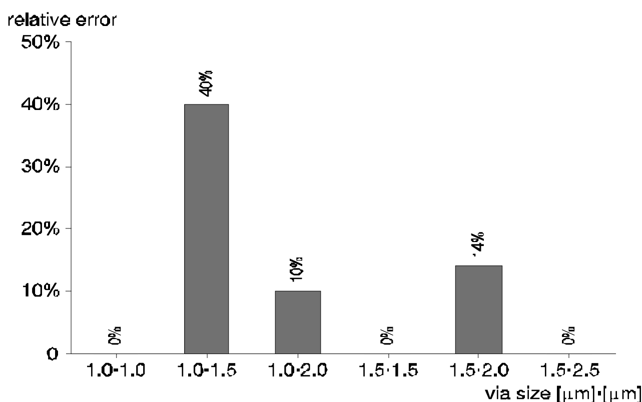

Fig. 11: Relative error caused by undetected open vias covered by short circuits.

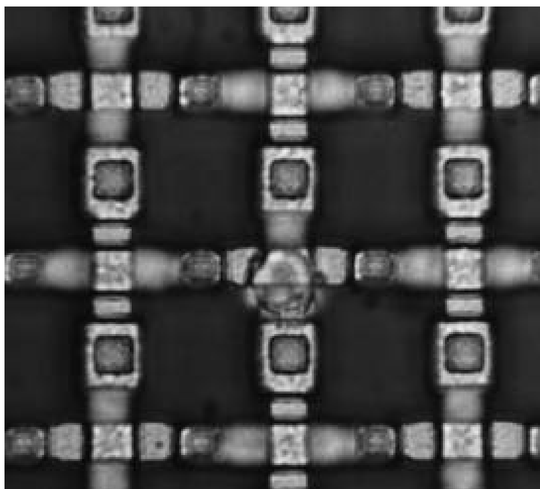

Fig. 12: Detail view of a detected defect that results in a short circuit.

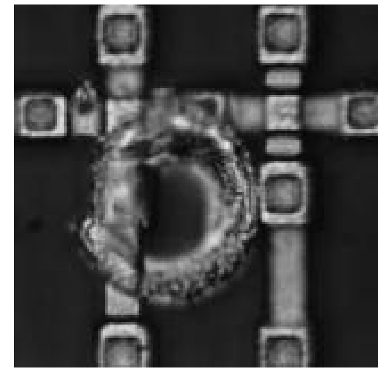

Fig. 13: Detail view of a detected defect that results in a short circuit.

Overall via sizes, about 12.5% of the interrupted strings are also connected to another string by a short circuit. The following figure shows the distribution of interrupted strings (open circuits), connected strings (short circuits), and strings where open circuits may be covered by shorts.

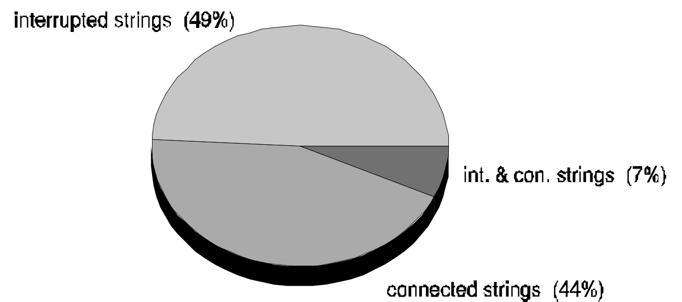

Fig. 14: Distribution of different types of faults.

This distribution also indicates the major influence of short circuits on the malfunction of product chips. Inside the WTS, the critical area of short circuits is similar to the critical area of short circuits inside a product chip, while the number of implemented vias is more than 10 times higher than on a typical product chip.

5 Conclusion

The described method to place vias or contacts as strings in a weave test structure guarantees not only a precise determination of open vias and open contacts but also the determination of the influence of short circuits. Using the localization flow charts, it is possible to conclude the subchip that contains a defect, because each via string pair can be clearly assigned to a specific subchip and its containing test structure layout objects.

Our measured data shows, that occurring short circuits cover open via strings, and therefore falsify measured data. In the course of this, accurate and correct data on open contacts and vias have to be taken out of test structures that also detects short circuits.

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