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Defect Parameter Extraction in Backend Process Steps Using a Multilayer Checkerboard Test Structure

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Abstract — **To control defect appearance in numerous conducting layers of backend process steps, a novel multilayer checkerboard test structure (MCTS) is presented. The Separation and localization of defects - causing electrically detectable intralayer short circuits as well as interlayer short circuits - will be achieved by dividing the chip area into distinguishable small subchips inside given standard boundary pads without using any active semiconductor devices. The precise localization facilitates a versatile optical defect parameter extraction.**

1 Introduction

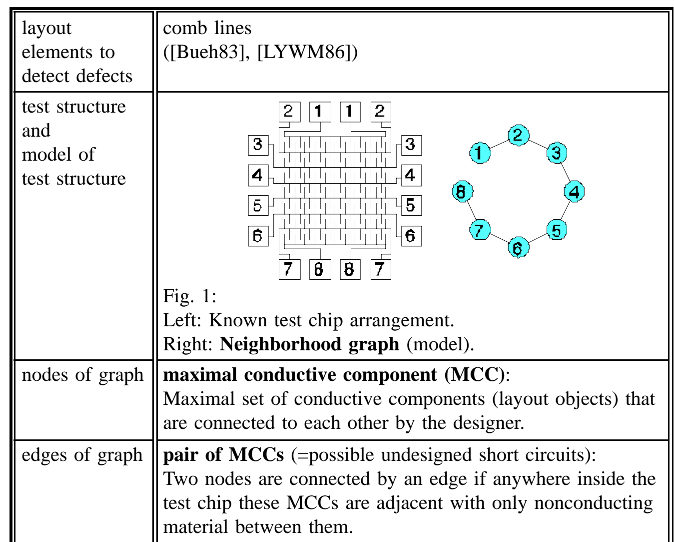
Today's complexity of integrated circuits requires more and more conducting backend layers to connect all circuit cells and devices. So, defects that cause typical backend faults inside a layer (**intra**layer short) and also between adjacent layers (**inter**layer shorts) gain more importance in defect statistics. For that, especially designed test structures to control the backend process steps for polysilicon and metal layers are in demand that combine the following partly contrasting conditions:

- *Large defect sensitive area* to detect random defects even if the defect density is low.
- *Layer sensitive defect separation* to assign electrically detected defects to a specific layer.
- *Precise defect localization* to simplify optical defect parameter extraction.
- *No active semiconductor devices* in test structures especially to control backend process steps.

Generally basic geometrical layout objects like comb lines and serpentine lines are used to investigate defect appearance in backend process steps, if no active semiconductor devices are available [IpSa77], [Bueh83], [LYWM86], [Walk87]. Two major methods to organize test chips are known, the "2 by N" probe-pad array [Bueh79] and standard boundary pads. The defect sensitive area inside a "2 by N" array is relatively small so that the large sensitive area inside the boundary pads seems to be more suitable. But here the number of pads is relatively small so that methods are required to separate defects. The following section gives the major principles to separate short circuit defects in numerous conducting layers. Section 3 describes the conversion of the theoretical separation method into an implemented test structure design. Section 4 deals with the principles to extract defect parameters. Finally some experimental results are presented.

2 Principle to Separate Defects in Numerous Conducting Layers

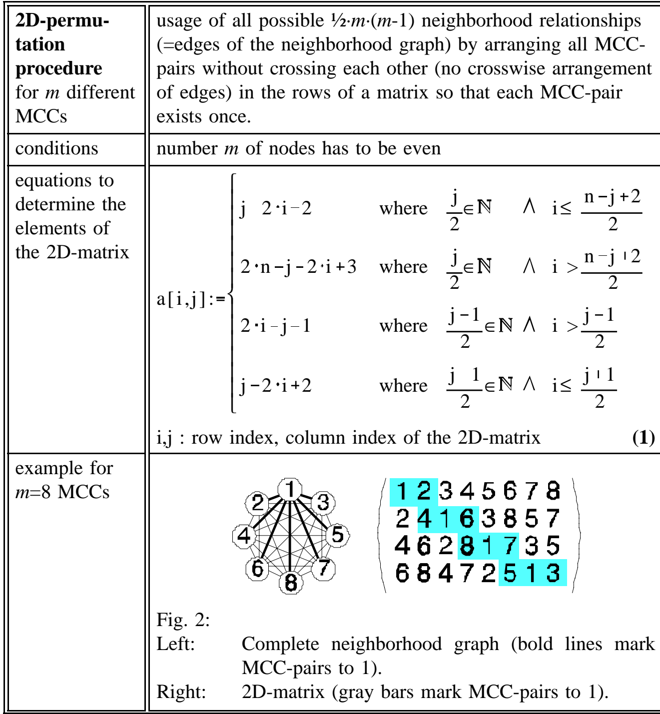
To explain the principle of defect separation, it is useful to model a test structure using the neighborhood graph introduced by [HeWe94] and [HeSt94]. The following table summarizes the model description.



layout elements to detect defects	comb lines ([Bueh83], [LYWM86])
test structure and model of test structure	Fig. 1: Left: Known test chip arrangement. Right: **Neighborhood graph** (model).
nodes of graph	**maximal conductive component (MCC)**: Maximal set of conductive components (layout objects) that are connected to each other by the designer.
edges of graph	**pair of MCCs** (=possible undesigned short circuits): Two nodes are connected by an edge if anywhere inside the test chip these MCCs are adjacent with only nonconducting material between them.

Tab. 1: Neighborhood graph to model a test structure.

An undesigned short circuit defect is only detectable between two different MCCs; therefore called **MCC-pair**. The number of different MCCs is limited to the number of pads. To increase the number of MCC-pairs or separable short circuits, respectively, all MCCs have to be arranged inside a test chip in a way that each MCC is once adjacent to every other MCC with only nonconducting material between them. The 2D-permutation procedure introduced by [HeWe92] and precisely described in [HeSt94] enables a defect separation in one conducting layer (ref. Table 2).



2D-permu-tation procedure for m different MCCs	usage of all possible $\frac{1}{2} \cdot m \cdot (m-1)$ neighborhood relationships (=edges of the neighborhood graph) by arranging all MCC-pairs without crossing each other (no crosswise arrangement of edges) in the rows of a matrix so that each MCC-pair exists once.
conditions	number m of nodes has to be even
equations to determine the elements of the 2D-matrix	$a[i,j] := \begin{cases} j \quad 2 \cdot i - 2 & \text{where } \frac{j}{2} \in \mathbb{N} \wedge i \leq \frac{n-j+2}{2} \\ 2 \cdot n - j - 2 \cdot i + 3 & \text{where } \frac{j}{2} \in \mathbb{N} \wedge i > \frac{n-j \, 2}{2} \\ 2 \cdot i - j - 1 & \text{where } \frac{j-1}{2} \in \mathbb{N} \wedge i > \frac{j-1}{2} \\ j - 2 \cdot i + 2 & \text{where } \frac{j \quad 1}{2} \in \mathbb{N} \wedge i \leq \frac{j \, 1}{2} \end{cases}$ i,j : row index, column index of the 2D-matrix **(1)**
example for m=8 MCCs	1 2 3 4 5 6 7 8 2 4 1 6 3 8 5 7 4 6 2 8 1 7 3 5 6 8 4 7 2 5 1 3 Fig. 2: Left: Complete neighborhood graph (bold lines mark MCC-pairs to 1). Right: 2D-matrix (gray bars mark MCC-pairs to 1).

Tab. 2: 2D-permutation procedure.

To enable a defect separation inside numerous layers and also between them we need an advanced permutation procedure.

2.1 Expanded Permutation Procedure

The following four Subsections describe the construction of a vector matrix that contains distinguishable MCC-pairs distributed among different layers.

2.1.1 Basic 2D-Matrix

Starting point is a set of n MCCs as can be seen on the left side of Figure 3. Having L conducting layers, a given set of MCCs (or pads) will be divided in L disjunct subsets. So each MCC will be implemented in a specific layer. The MCCs of each subset is given an index running 1 to $m = \frac{n}{L}$, where the total number m of MCCs per subchip has to be even ($\frac{1}{2} \cdot \frac{n}{L} \in \mathbb{N}$).

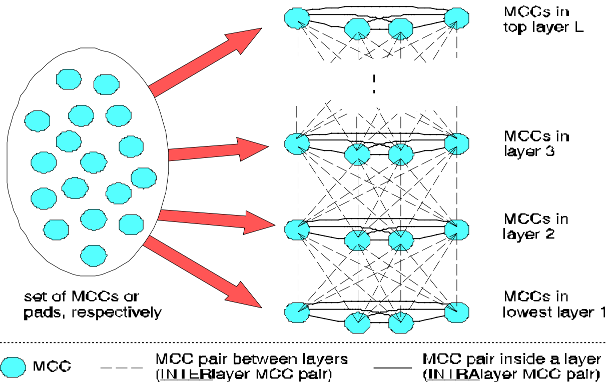


Fig. 3: Splitting up a set of MCCs in MCC subsets according to the number L of layers.

Now the 2D-permutation procedure will be applied to the m MCCs of one subset to get the **basic 2D-matrix** containing $\frac{m}{2}$ rows and m columns (ref. Table 2). To also realize all m^2 MCC-pairs between adjacent layers, we have to expand the basic 2D-matrix into two different matrices, which will be introduced next.

2.1.2 Forward Permutation Matrix (FPM)

The number m^2 of MCC-pairs between adjacent layers is nearly twice the number $\binom{m}{2}$ of MCC-pairs inside a layer. For that, the **forward permutation matrix (FPM)** will consist of m rows and m columns. Each element $f[i,j]$ of the FPM will be calculated using the following equation

$$f[i,j] = a[((i+1) \text{ div } 2),j] \qquad \textbf{(2)}$$

where a[i,j] is taken out of the basic 2D-matrix. All rows of the basic 2D-matrix are twice included inside the FPM in a top-down (*forward*) arrangement. The construction of the FPM is illustrated in Figure 4 for m=6. The left side shows the basic 2D-matrix and the right side gives the final FPM.

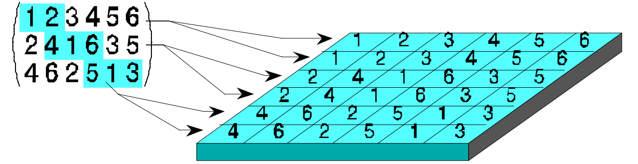


Fig. 4: Construction of forward permutation matrix (m=6).

2.1.3 Reverse Permutation Matrix (RPM)

The **reverse permutation matrix (RPM)** will consist of m rows and m columns too. Each element $r[i,j]$ of the RPM will be calculated using the following equations

$$r[i,j] := \begin{cases} a[((m-i \, 1) \text{ div } 2),(m-j \quad 1)] & \text{where } i < m \\ a[((i+1) \text{ div } 2),j] & \text{where } i \quad -m \end{cases} \qquad \textbf{(3)}$$

where a[i,j] is also taken out of the basic 2D-matrix. All rows of the basic 2D-matrix are again twice included inside the RPM, but here in a bottom-up (*reverse*) arrangement. In addition to that, the column index is mirrored in m-1 rows. The reverse construction is illustrated in Figure 5 for m=6, where the transformation of the basic 2D-matrix rows with mirrored column index is marked with dashed lines.

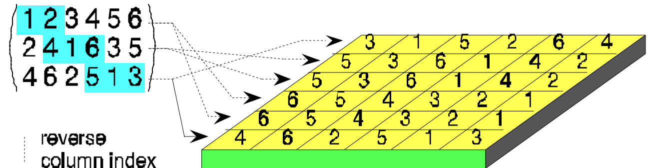


Fig. 5: Construction of reverse permutation matrix (m=6).

2.1.4 Vector Matrix

Finally, both types of expanded permutation matrices (FPM and RPM) will be alternating arranged one above another in a vector matrix. The lowest layer always starts with a FPM.

$$
V := \left(\begin{array}{cccc}
\begin{pmatrix} r[1,1] \\ \vdots \\ f[1,1] \\ r[1,1] \\ f[1,1] \end{pmatrix}_{1,1} & \begin{pmatrix} r[1,2] \\ \vdots \\ f[1,2] \\ r[1,2] \\ f[1,2] \end{pmatrix}_{1,2} & \cdots & \begin{pmatrix} r[1,j] \\ \vdots \\ f[1,j] \\ r[1,j] \\ f[1,j] \end{pmatrix}_{1,j} \\
\begin{pmatrix} r[2,1] \\ \vdots \\ f[2,1] \\ r[2,1] \\ f[2,1] \end{pmatrix}_{2,1} & \begin{pmatrix} r[2,2] \\ \vdots \\ f[2,2] \\ r[2,2] \\ f[2,2] \end{pmatrix}_{2,2} & \cdots & \begin{pmatrix} r[2,j] \\ \vdots \\ f[2,j] \\ r[2,j] \\ f[2,j] \end{pmatrix}_{2,j} \\
 & \vdots & & \\
\begin{pmatrix} r[i,1] \\ \vdots \\ f[i,1] \\ r[i,1] \\ f[i,1] \end{pmatrix}_{i,1} & \begin{pmatrix} r[i,2] \\ \vdots \\ f[i,2] \\ r[i,2] \\ f[i,2] \end{pmatrix}_{i,2} & \cdots & \begin{pmatrix} r[i,j] \\ \vdots \\ f[i,j] \\ r[i,j] \\ f[i,j] \end{pmatrix}_{i,j}
\end{array}\right) \quad (4)
$$

All MCC-pairs now exist twice inside a layer and once between adjacent layers. For n=24 MCCs, Figure 6 shows the vector matrix over L=4 layers, each containing m=6 MCCs.

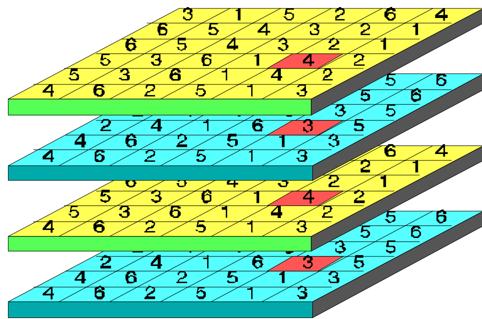


Fig. 6: Construction of expanded vector matrix (n=24, L=4, m=6).

3 Multilayer Checkerboard Test Structure (MCTS) Design

All elements (MCCs) of the vector matrix will be replaced by major lines in conducting layers according to the expanded permutation procedure. The arrows in the following figure mark the distinguishable MCC-pairs or undesigned short circuit defects, respectively.

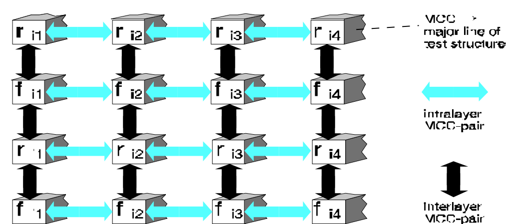


Fig. 7: MCCs of one row inside the vector matrix converted into main lines of a test structure.

The major lines will be arranged inside given boundary pads generating an array of rectangular subchips, where defect sensitive test structures will be placed consisting of basic layout objects like comb lines. Each subchip contains a unique set of MCC-pairs, so that all subchips are clearly distinguishable. The checkered arrangement of subchips is responsible for the naming of the **multilayer checkerboard test structure (MCTS)**.

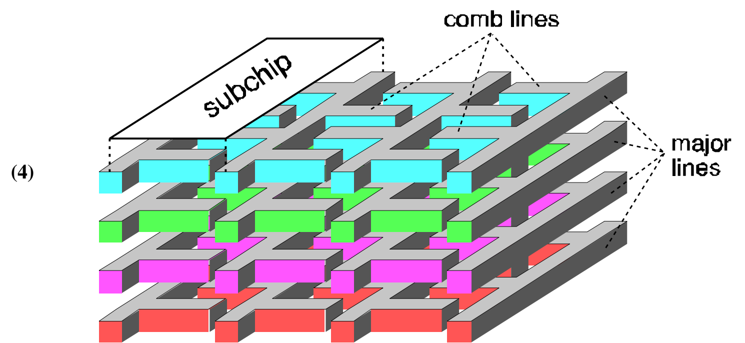


Fig. 8: 3D-view of the Multilayer Checkerboard Test Structure (MCTS).

So, a MCTS consists of m·(m-1) subchips. The following figure shows a MCTS design for n=56 MCCs distributed among L=4 layers, each containing a subset of m=14 MCCs. The course of two specific MCCs in layer l=2 is marked with bold lines. They only are adjacent in two neighbored subchips with the row index i=12 or i=13 and the column index j=5.

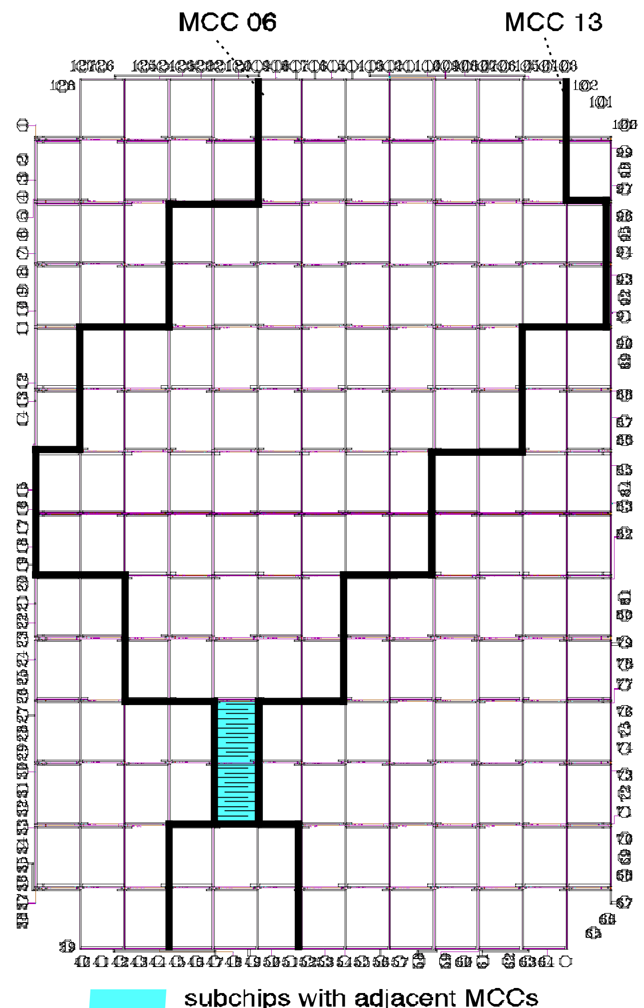


Fig. 9: Main frame of a Multilayer Checkerboard Test Structure (MCTS) without detailed comb lines inside the subchips.

If short circuits occur, at least two MCCs are connected. Since we know in which subchips these specific MCCs are neighbors we can conclude to the subchip that contains the defect.

The permutation of MCCs inside the FPM and RPM requires routing channels between the subchip rows. In the course of this, the elements of one matrix type are directly connected while the elements of the other matrix type have to be permuted and vice versa. Only two horizontal lines in two layers are necessary to permute the MCCs of 4 layers. Figure 10 shows the basic routing elements.

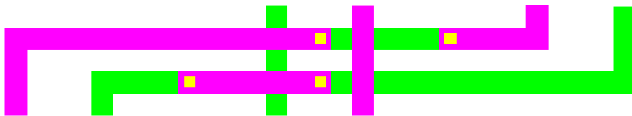


Fig. 10: Basic elements of routing channel.

Figure 11 shows the two different types of routing channels, where only these basic elements are used. The numbered arrows mark the connections to the four different layers. The design of the both routing channels have a duplicative "repeat unit" over two subchip columns. Therefore, the routing channels are designed in the same way for all possible checkerboard frame sizes containing any even number *m* of subchip rows and *m-1* subchip columns. The systematic construction of these routing channels enables a machine assisted test structure generation.

The connection of the MCCs to given boundary pads will be done, using the vector matrix, where each MCC is placed at least three times at a boundary row or column, respectively. So, more than 90% of the area inside the boundary pads will be completely filled with defect sensitive structures.

4 Defect Parameter Extraction

Generally, short circuits are detectable, testing the resistance between different pads or MCCs, respectively. To measure the resistance of the test structures, a digital tester will be used, because the electrical test must only decide whether there is a defect or not [HeWe95c]. The measured values are assigned to possible defects according to the following table.

measured value		expected value in reference data	detected type of defect
voltage	binary		
$V_{measured} < V_{threshold}$	0	0	defectless
$V_{measured} < V_{threshold}$	1	0	short circuit

Tab. 3: Data conversion.

To detect the defects inside a test chip a "walking-one" over all pads is sufficient while measuring the voltage responses at all other pads. The following table contains a defectless reference response data set, where the row index *p* represents the test vector number and the column index *q* represents the sequence of pads brought into line with the increasing MCC-index per layer and the increasing layer index itself.

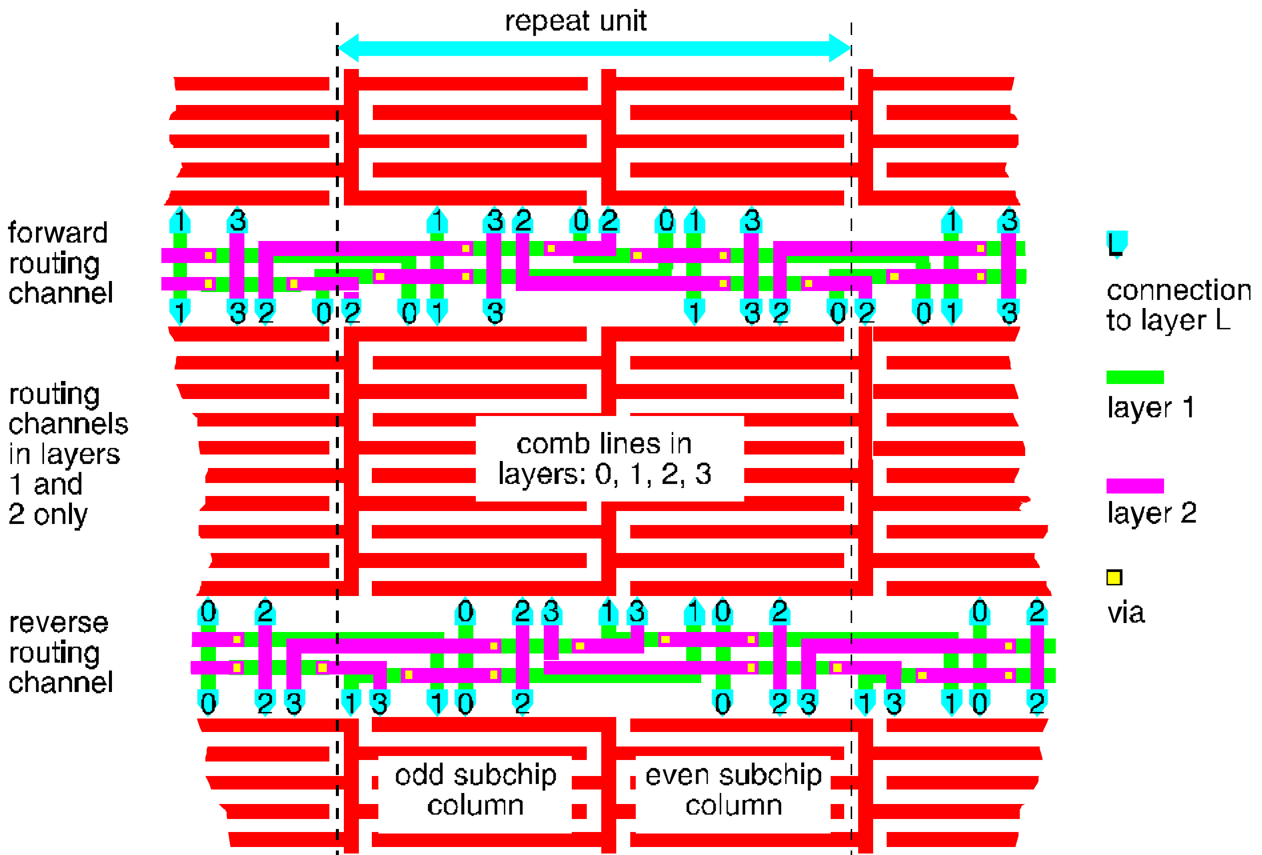


Fig. 11: Routing channels of MCTS.

```
     q=000000000111111111
       123456789012345678
  p=01 .00000000000000000 * MCC 01, layer 0 (bottom layer)
    02 0.0000000000000000 * MCC 02, layer 0
    03 00.000000000000000 * MCC 03, layer 0
    04 000.00000000000000 * MCC 04, layer 0
    05 0000.0000000000000 * MCC 05, layer 0
    06 00000.000000000000 * MCC 06, layer 0
    07 000000.00000000000 * MCC 01, layer 1
    08 0000000.0000000000 * MCC 02, layer 1
    09 00000000.000000000 * MCC 03, layer 1
    10 000000000.00000000 * MCC 04, layer 1
    11 0000000000.0000000 * MCC 05, layer 1
    12 00000000000.000000 * MCC 06, layer 1
    13 000000000000.00000 * MCC 01, layer 2 (top layer)
    14 0000000000000.0000 * MCC 02, layer 2
    15 00000000000000.000 * MCC 03, layer 2
    16 000000000000000.00 * MCC 04, layer 2
    17 0000000000000000.0 * MCC 05, layer 2
    18 00000000000000000. * MCC 06, layer 2
```

Tab. 4: Reference Data of a defectless test chip where $n=18$ and $m=6$.

If unexpected "1" values occur in one row p of a measured response data set, the defect or defects that result in this measured short circuit will be localized using the flow chart of Figure 12. The column indices $q1,q2,...$ of all "1" values in row p and the index p itself have to be taken into account. The locations of defect containing subchips have to be separately determined for each of $½·k·(k\text{-}1)$ MCC-pairs out of a set of k connected MCCs (indices $p,q1,q2, ...$). The flow chart contains first the assignment to the layer and second the specific localization sub-routines to compute the coordinates i and j of the subchips. These sub-routines use the equations of Table 5.

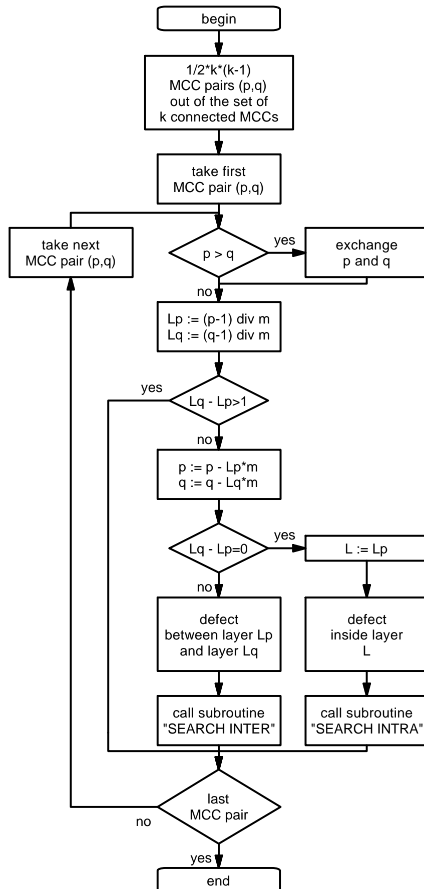


Fig. 12: Procedure to localize defects that results in electrically detectable short circuits (layer index running bottom-up, starting at "l=0" for the lowest layer).

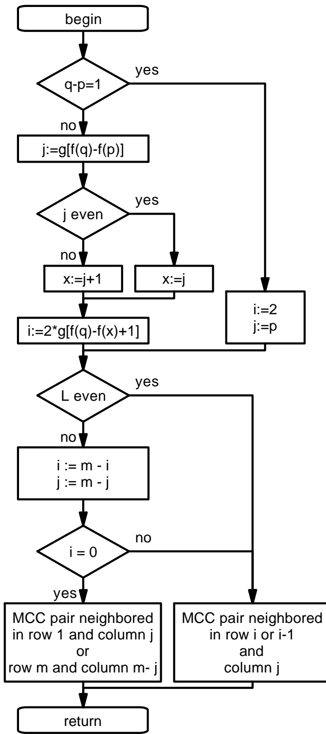


Fig. 13: Sub-routine "SEARCH INTRA".

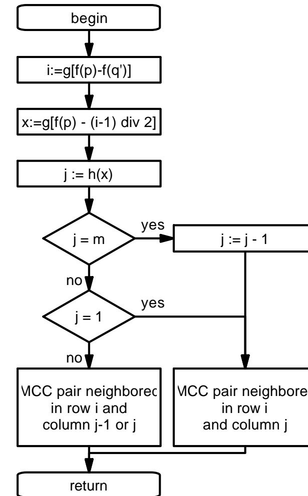


Fig. 14: Sub-routine "SEARCH INTER".

$f(x) := \begin{cases} \frac{x}{2} & \text{if } \frac{x}{2} \in \mathbb{N} \wedge 1 < x \le m \\ m - \left[\frac{x-1}{2}\right] & \text{if } \frac{x+1}{2} \in \mathbb{N} \wedge 1 \le x < m \end{cases}$	**(5)**
$h(x) = \bar{f}(x) := \begin{cases} 2 \cdot x & \text{if } 0 < x \le \frac{m}{2} \\ (m-x) \cdot 2 - 1 & \text{if } \frac{m}{2} < x \le m \end{cases}$	**(6)**
$g(x) := \begin{cases} x & \text{if } 0 < x \le m \\ x + m & \text{if } -m < x \le 0 \end{cases}$	**(7)**

Tab. 5: Functions used in the localization sub-routines.

5 Experimental Results

A multilayer checkerboard test structure was designed as an in-line process monitor to control defect appearance. The design was done in cooperation with ALCATEL SEL, Germany and manufactured at National Semiconductor, USA. The MCTS has n=56 MCCs, distributed among L=4 layers (polysilicon - metal1 - metal2 - metal3) each containing a subset of m=14 MCCs. All in all 182 distinguishable subchips contain comb lines of two different dimensions. The following figure shows a part of the MCTS. Figure 16 shows a detected defect that results in an electrically measurable short circuit.

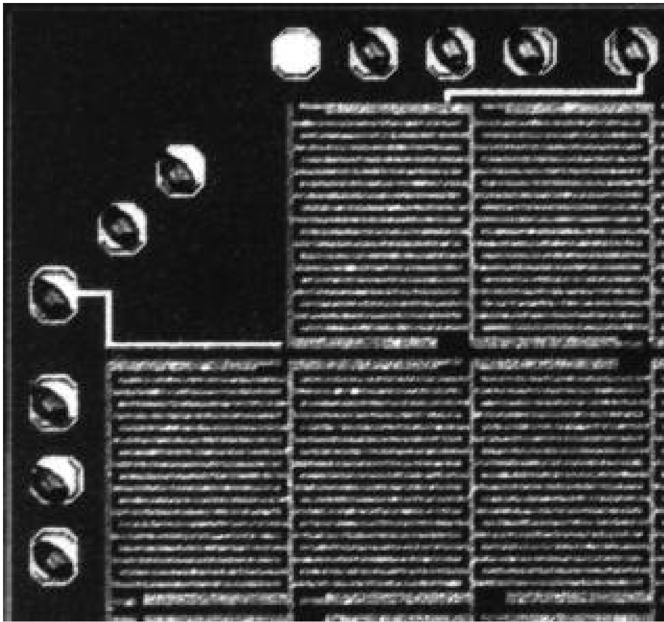


Fig. 15: Upper left corner of a MCTS.

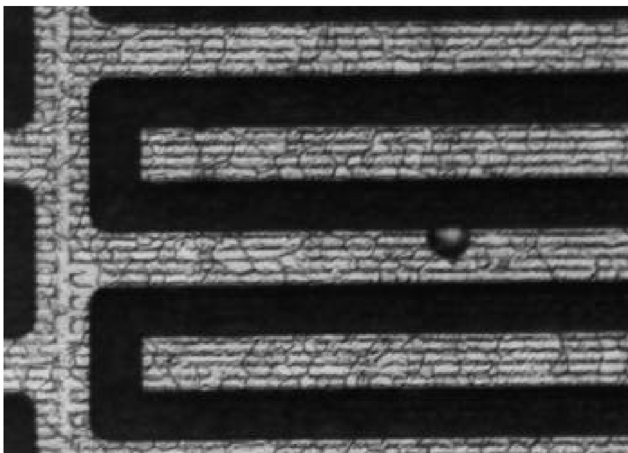


Fig. 16: Detail view of a detected hillock defect.

Finally Figure 17 gives the distribution of the digitally measured short circuits among the different layers. The number of defects increases from the bottom layer to the top layer unless larger design rules (here for metal 3) prevent this effect. 15% of the total number of short circuits are interlayer shorts while 85% are intralayer shorts.

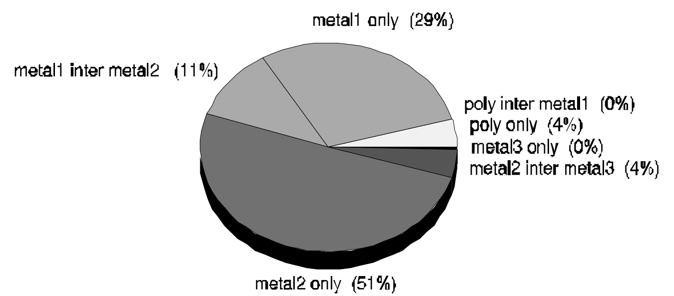


Fig. 17: Distribution of electrically detected defects inside and in-between 4 conducting layers.

6 Conclusion

The described method to place test structure layout objects inside checkered subchips, enables an efficient inspection of defects that occur anywhere in numerous conducting layers of backend process steps. The multilayer checkerboard test structure detects systematic problems as well as random defects due to its extensive defect sensitive area. However, the expanded permutation procedure guarantees a precise separation and localization of defects, to facilitate an additional versatile optical defect inspection to extract parameters like size, outline and process specific causes of defects. The systematically designed checkerboard framework enables a machine-assisted generation of test chips without any active semiconductor devices and without any limitation to the number of layers.

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