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Modeling of Test Structures for Efficient Online Defect Monitoring Using a Digital Tester

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Abstract — A novel methodology for digital measuring procedures and digital data analysis is presented in order to evaluate an online process control and defect monitoring. That can be done by manufacturing test chips side by side with standard chips and measuring them with the same measuring equipment - the digital tester. To achieve a fast and effective (efficient) measuring procedure and data analysis test structures will be modeled in geometry-graphs, neighborhood-graphs and connection-graphs.

1 Introduction

Continuous data about process specific defect parameters like the density of short circuits and open circuits are required for yield prediction, design rule development, test pattern generation and process problem debugging [Walk87], [Maly87], [Spie93], [Mitc85], [LYWM86]. To determine significant data of these parameters, test structures are used in separate lots [Spen83]. An online defect parameter monitoring requires the manufacturing of test chips side by side with standard chips so that it is reasonable to use the same measuring equipment - a digital tester with a standard probe card. Therefore, the test structures will be embedded inside a regular boundary pad frame.

The evaluation with a digital tester requires a special measuring procedure (see section 2). To achieve an effective data analysis, novel test structure models have been developed which are described in section 3. Section 4 shows the novel approach of defect diagnosis and analysis. Section 5 gives some experimental results.

2 Measuring Procedure Using a Digital Tester

In this section, two of the most common defects are discussed, namely extra material defects and missing material defects. Depending on whether the damaged material is conducting or nonconducting, the defect can cause a short circuit fault or an open circuit fault. In order to detect defects of these types, special test structures were developed. Comb structures (cf. figure 1) [Bueh83] [LYWM86] [Walk87] aim at extra material defects. These defects can cause a short between isolated lines (usually designed as combs) and thus significantly reduce the resistance measured between the pads.

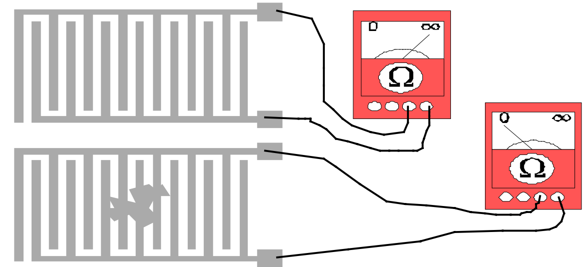

Fig. 1: Method to detect defects which result in short circuits

Meandering strings (cf. figure 2) [Bueh83] [LYWM86] [Walk87] are applied to detect missing material defects. If these defects are large enough, they interrupt the connection between the pads and increase the measured resistance very much.

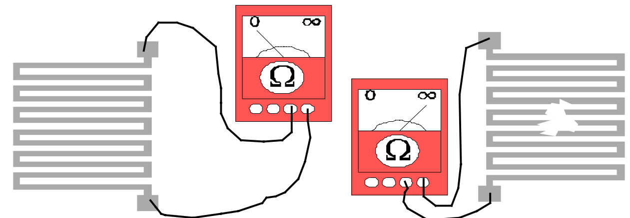

Fig. 2: Method to detect defects which result in open circuits

To measure the resistance of a test structure, commonly analog testers with a measurement frequency below 1 Hz are applied [BCKJ91] [MiFH92] [RoBF92]. In the context of this paper, an electrical test must only decide whether there is a defect or not. So in general a digital tester should be sufficient.

A digital tester has important advantages. First, the measurement frequency of a digital tester is normally many times higher than the frequency that is possible with analog 2- or 4-point measurements. So the evaluation of test structures can be much faster. Secondly, every measured value needs only one bit. This reduces the storage requirements. Thirdly, a data reduction is possible already during the electrical measurements since the measured binary data can easily be compared to reference values. Finally, using a digital tester simplifies online process control because test chips and standard chips can be measured in the same way and with the same measuring equipment.

The results of experiments have shown that applying a digital tester is feasible. The resistance values of about 100 equally designed meandrous structures have been measured. In the

histogram of figure 3 two clusters can be distinguished clearly. One of these clusters contains the resistance values of the fault free meandrous structures. The other cluster is due to the meandrous structures with defects causing open circuit faults. In [MiFH92] a similar distribution was obtained.

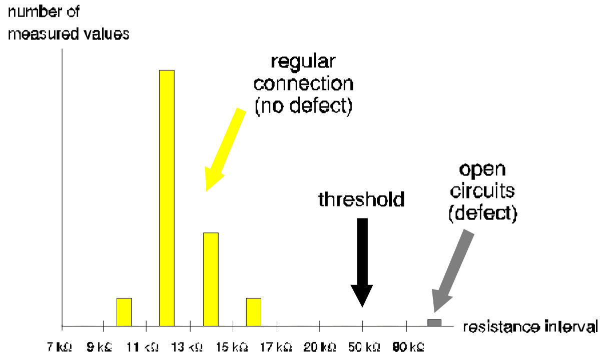

Fig. 3: Histogram of analogly measured line resistances

Using Ohm's law the resistance measurement can be reduced to a voltage measurement. The threshold voltage of the digital tester is set to a value in the middle between the two clusters of figure 3. The two distinguishable intervals will be assigned to the information "defect detected" or "no defect detected".

measured voltage	binary value	short circuit detected	open circuit detected
$V_{measured} \geq V_{threshold}$	1	yes	no
$V_{measured} < V_{threshold}$	0	no	yes

Tab. 1: Data conversion

To achieve a complete adaption of a digital tester to the test structure conditions, the stimulus Voltage V_S and the measuring frequency f_m have to be adjusted too. [HeWe92] validates this procedure for a checkerboard test structure.

3 Modeling Of Test Structures

To enable an efficient analysis of digitally measured data, a formal model of a test structure is introduced first. [CaDJ89] describes a defect-graph modeling for analogly measured test structures data, but this model only deals with short circuit defects. An effective application to digitally measured data of open and short circuit defects requires a novel comprehensive methodology which will be described here.

3.1 Geometry-Graph of Test Structures

To realize an efficient digital data analysis, it is necessary to model the geometry of layout objects inside a test chip with a *geometry-graph*. The nodes stand for the measuring points and the edges represent all conductive layout objects (conductive component (cc)) like a comb or a meandrous line between two measuring points. Conductive components, which are only connected to one measuring point will be modeled as loops. Figure 4 shows on the left side typical test structures [Bueh83], [LYWM86], [Walk87] and on the right side their geometry-graphs.

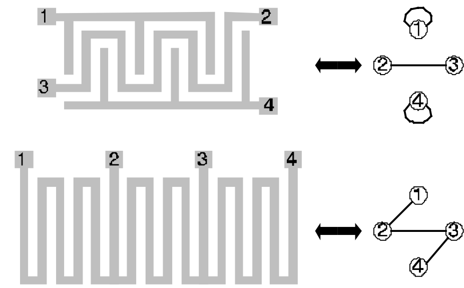

Fig. 4: Typical test structures (left) and their geometry-graphs (right)

Measuring points which are accessible for the measuring equipment are equal to the pads of a test chip (and therefore also called pads). All not accessible measuring points are called internal nodes. To implement internal nodes in a test structure design is up to the designer, but it shouldn't be forgotten that internal nodes can cause irreversible defect and fault coverage problems [Bueh83] [HeWe93] [Guga93].

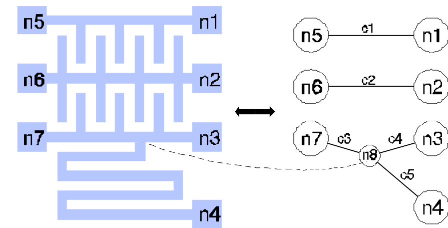

Fig. 5: Test structure and geometry-graph with internal nodes

3.2 Neighborhood-Graph of Test Structures

The identification and localization of short circuit defects require also information about the neighborhood relationship between differently connected layout objects [HeSt93] [HeWe94a]. Generally a test structure contains a set of conductive components (conductive layout objects) which are possibly arranged in different layers. A maximal set of conductive components and measuring points that are connected to each other is called a maximal conductive component (mcc). Each mcc should contain at least one pad.

The neighborhood relationship of mcc's inside the whole test structure is modeled by the *neighborhood-graph* (mccn-graph). The nodes represent the maximal conductive components of the fault-free test structure. So every node of the neighborhood-graph corresponds to a subset of pads (=nodes of the geometry-graph) **and** conductive components (=edges of the geometry-graph) which belongs to one single mcc. Two nodes mcc_1, mcc_2 are connected by an edge if and only if in some region of the test structure a layout object of mcc_1 and a layout object of mcc_2 lie side by side or one on top of the other with only nonconducting material between them. Thus the edges correspond to shorts that can be caused by defects (undesigned shorts). Figure 6 shows typical test structures and their neighborhood-graphs. To refer to the geometry-graph the mcc index of one node in the neighbor-hood-graph contains the indices of all pads (=nodes inside the geometry-graph) which belongs to this specific mcc.

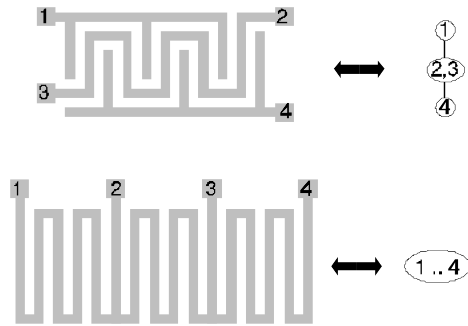

Fig. 6: Test structures (left) and their neighborhood-graphs (right)

In [CaDJ89] the defect-graph has been defined for a similar purpose. Its nodes have the same meaning as in the neighborhood-graph, but its edges describe only the undesigned shorts that are considered in the measurement analysis. So the defect-graph mixes information about the design of the test structure (nodes) and information about the evaluation (edges). In contrast, the structure of the neighborhood-graph introduced above is determined solely by the geometric features of the test structure. It is independent of the applied analysis procedure.

3.3 Connection-Graph of Test Structures

An efficient measurement data management requires information about the connections between the measuring points (pads) of a test chip [HeWe92]. During the electrical measurement a voltage can be measured between two pads of a test chip. For that every test chip will be modeled with a *connection-graph*. Here, the nodes stand for the accessible measuring points (pads) and the edges represent the conductive connections (measurable current flow) between accessible measuring points. The connection-graph of a fault-free test structure is called *golden device*. Figure 7 shows on the left side two test structures and on the right side their connection-graphs.

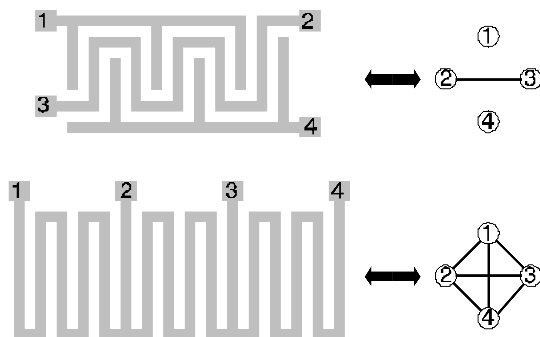

Fig. 7: Test structures (left) and their connection-graphs (right)

4 Data Analysis

The measurement results of test structures are representable by matrices, which can be converted into the graphs described above. The detection of the defects will be achieved by comparing the different graphs or their matrices, respectively. This section therefore presents novel algorithms which enable machine-assisted defect diagnostics.

The data of a digital tester are normally arranged in two matrices. The *test matrix* (stimulus matrix) contains the test vectors, where each row represents a test vector and the columns represent the different stimulus points (pads). The *response matrix* contains the measured vectors where each row represents the measured response to a test vector and the columns represent the different measuring points or pads respectively. Normally bidirectional tester channels are used, so that a test structure without any active elements (transistors, diodes, ...) will be completely tested by using a "walking one" as test vector set ("1" = channel in stimulus mode; "0" = channel in response mode) over all pads. Figure 8 shows an example of the described procedure for a test structure with 7 pads, where bidirectional tester channels are used with a walking one in the stimulus matrix.

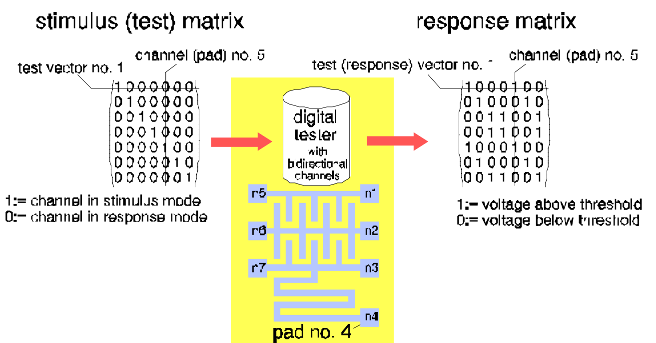

Fig. 8: Example of data analysis

Each test vector and its measured response can be converted into a connection-graph [HeWe93] [Guga93]. In case of using a "walking-one" the conversion into the connection-graph is simplified, because the rows and columns of the quadratic response matrix directly represent the accessible measuring points (pads). A "1" in row i and column j stands for a measured conductive connection between the node i and the node j. A "0" in row i and column j stands for a measured nonconductive connection between the node i and the node j. The following figure shows the conversion algorithm.

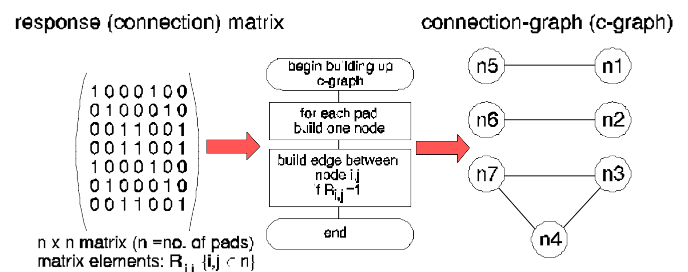

Fig. 9: Converting the response matrix into the c-graph

A missing or extra connection can be concluded from the comparison of the different graphs, which also leads to the localization of resulted defect. Subsection 4.1 deals with the detection of open circuits and subsection 4.2 describes the method to detect short circuits. Both methods are explained by an example. For that the following figure contains the fault free test structure of figure 5 and all necessary graphs.

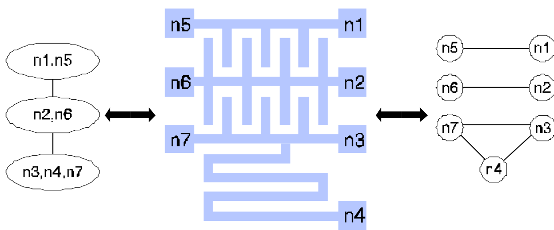

Fig. 10: Neighborhood-graph (left) and connection-graph (golden device) (right) of a sample test structures

For this example we assume that the structure has two different defects as can be seen in the following figure.

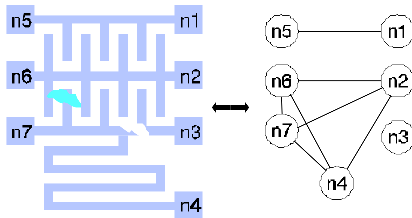

Fig. 11: Measured connection-graph of a test structure with open and short circuits

4.1 Open Circuits

The detection of open circuits requires a comparison of the measured connection-graph to the geometry-graph of the test structure. Due to the existence of internal nodes, the measured connection-graph has to be transformed into a graph, which is directly comparable to the geometry-graph. In the first step all effects caused by short circuits have to be faded out. For that the measured connection-graph will be compared with the golden device. The AND operation (cf. table 2) of the edges of these two graphs lead to the novel c-graph.

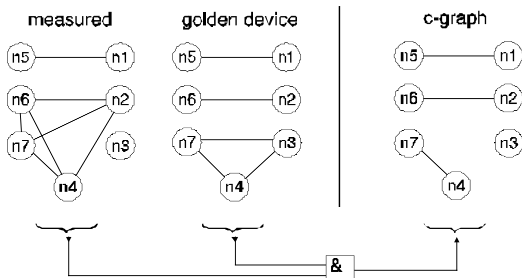

Fig. 12: Fade out all edges which are caused by short circuits

edge in graph 1	edge in graph 2	edge in novel graph
not existing	not existing	not existing
not existing	existing	not existing
existing	not existing	not existing
existing	existing	existing

Tab. 2: AND operation (&) of the edges of two graphs into a novel third graph, where all nodes are equal

In the second step the c-graph has to be transformed into an extended c-graph (ec-graph), which also includes internal nodes. For that each edge in the c-graph is replaced by the equivalent path (including internal nodes) of the geometry-graph. Also, all edges get an index with reference to the geometry-graph.

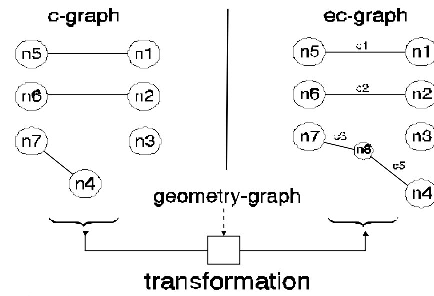

Fig. 13: Transforming c-graph into extended c-graph

Finally the ec-graph will be compared to the geometry-graph to identify open circuits. For that a NOT operation (cf. table 3) will be applied to the edges of the ec-graph. Afterwards an AND operation (cf. table 2) of the edges of these two graphs lead to the result-graph. Each edge in this result-graph represents an open circuit in the implemented conductive component. In this example an open circuit in the conductive component "c4" was detected.

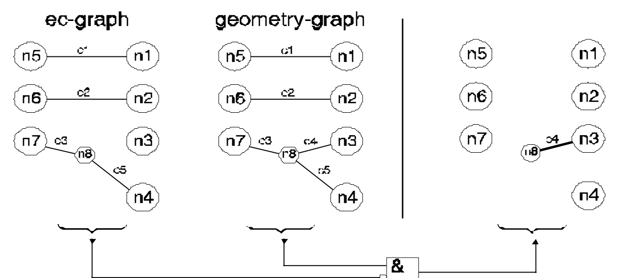

Fig. 14: Diagnosis of open circuits

edge in input graph	edge in novel graph
not existing	existing
existing	not existing

Tab. 3: NOT operation of the edges of an input graph into a novel graph, where all nodes are equal

The following figure shows the general methodology to detect open circuits.

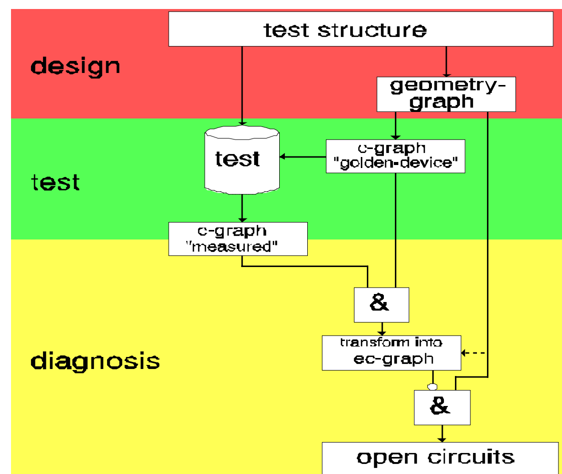

Fig. 15: Procedure to diagnose open circuits

4.2 Short Circuits

The detection of short circuits requires a comparison of the measured connection-graph to the neighborhood-graph of the test structure. Due to the existence of multiple pads at one single mcc, the measured connection-graph has to be transformed into a graph which is directly comparable to the neighborhood-graph. In the first step all designed connections have to be faded out. For that a NOT operation (cf. table 3) will be applied to the edges of the golden device. Afterwards an AND operation (cf. table 2) of the edges of these two graphs lead to the novel c-graph.

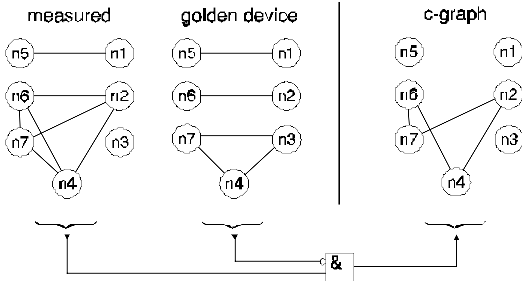

Fig. 16: Fade out all designed connections (edges)

In the second step the c-graph has to be transformed into a mcc-graph, which only includes all maximal conductive components as nodes (of the mccn-graph). For that every subset of pads (=nodes of the c-graph) and conductive components (=edges of the c-graph), which belongs to one single mcc will be summarized to one node in the mcc-graph. Multiple edges between two nodes of the novel mcc-graph will be replaced by one single edge.

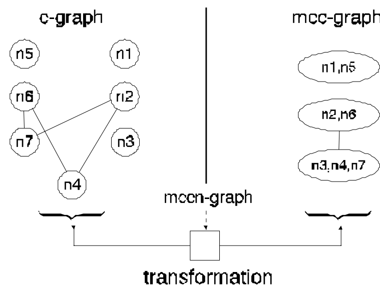

Fig. 17: Transforming c-graph into mcc-graph

Finally the mcc-graph will be compared to the mccn-graph to identify short circuits. The AND operation (cf. table 2) of the edges of these two graphs lead to the result-graph. Each edge in this result-graph represents a short circuit between different mcc's. In this example a short circuit between $mcc_{(n2,n6)}$ and $mcc_{(n3,n4,n7)}$ was determined.

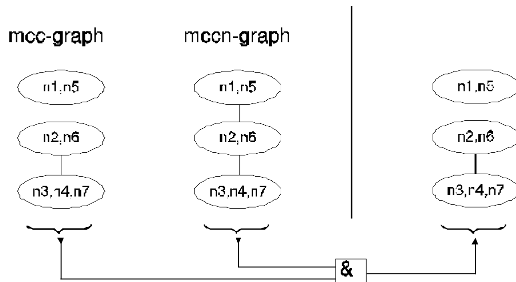

Fig. 18: Diagnosis of short circuits

The following figure shows the general methodology to detect short circuits.

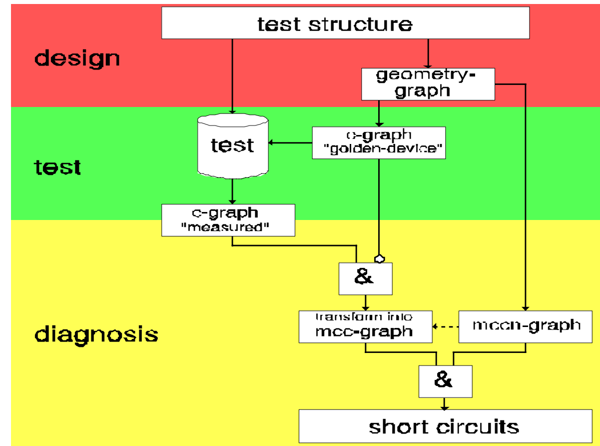

Fig. 19: Procedure to diagnose short circuits

4.3 Machine Assisted Data Analysis

Both methods to detect defects are independently applicable. For that the comparison and transformation of the graphs are transferable into computer algorithms [HeWe93] [Guga93]. This methodology of data handling is included in a program called VIADUCT (**V**ersatile Automatic **I**dentification **A**nalysis of **D**efects from **U**ndesigned Open and Short **C**ircuits in **T**est Structures).

5 Experimental Results

Nearly 1000 test chips with different test structure designs were manufactured at the *Institut für Mikroelektronik Stuttgart* (**IMS**) to validate this procedure of data measurement and analysis. To detect open circuit defects, 20 meandrous lines were designed in a single metal layer inside a boundary pad frame of 40 pads.

To detect short circuits, 20 comb lines were also designed in a single metal layer inside the same boundary pad frame. All in all 9 modules per test chips with different line width and space were implemented. These chips were measured first with a digital tester and later on with an analog tester. Both test methods yield the same number of detected defects. The figures 20 and 21 contain the comparison between digitally and analogly detected defects.

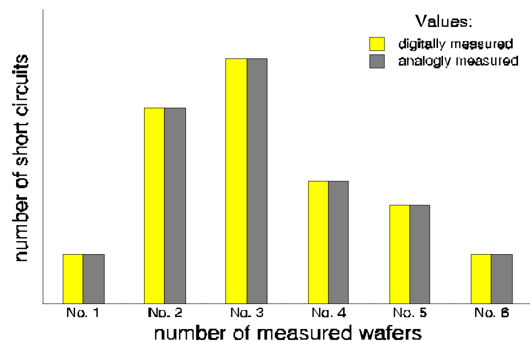

Fig. 20: Comparison of the number of analogly measured and digitally measured short circuit defects

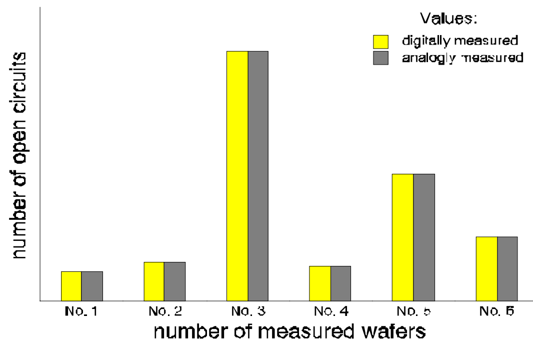

Fig. 21: Comparison of the number of analogly measured and digitally measured open circuit defects

The difference of measuring time was $2 \cdot 10^{-3}$ seconds per test chip for the digital test and 20 seconds per test chip for the analog test. Furthermore all analogly measured data have to be stored and analyzed, because a data comparison with reference data during the electrical measurement is impossible.

Due to the easy data comparison between digitally measured data and their reference data an effective data reduction is already achieved during the electrical measurement. Only the data which differ from the reference data have to be stored and analyzed. So the analysis of the digital test chip data takes less time than the analysis of the analogly measured data.

Using the program VIADUCT on a Sun4 workstation, the data analysis time was less than 1 sec per module.

Figure 22 shows some results of the additional optical defect inspection.

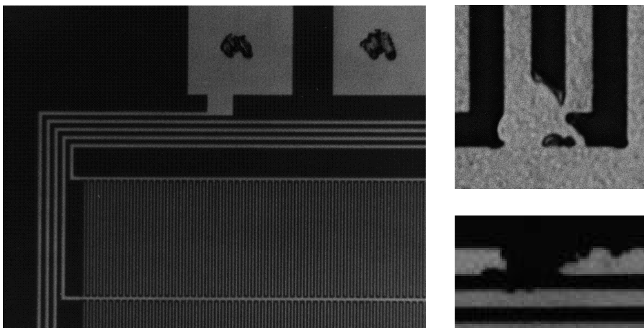

Fig. 22: Optical Inspection of electrically detected defects

6 Conclusion

The accuracy of defect detection using a digital tester is the same as the accuracy of most common analog measuring procedures, but the measuring time is at least 10000 times faster. This is important if checkerboard test structures [HeWe92] [Hess93] [HeSt93] are used because the number of 2 point measurements is too high for an efficient analog measurement. The comparability of digitally measured data and the usage of the described test structure graph models leads to a faster data analysis. Finally, the usage of a digital tester simplifies an online process control, because test chips and standard chips can be measured in the same way with the same measuring equipment.

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