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Drop in Process Control Checkerboard Test Structure for Efficient Online Process Characterization and Defect Problem Debugging

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Abstract — A novel diode-checkerboard test structure (DCTS) is presented to determine open circuit defects and short circuit defects as well as to investigate the 3D-influence of underlying topography. The arrangement of the DCTS in a standard boundary pad frame and the digitally measuring procedure evaluate a fast and effective (efficient) online process characterization. The precise defect detection and localization facilitate an additional optical defect problem debugging.

1 Introduction

Today's semiconductor manufacturing technologies cannot guarantee that all produced chips completely satisfy the specification. Even if the design is error-free, defects can occur during manufacturing and make a chip faulty. Global defects, which damage large portion of the wafer, can be detected easily. But small defects like little spots of extra material or missing material are often hard to detect as they damage only single transistors or lines. This paper deals with small defects that have dimensions comparable to the size of transistors.

Information about type, size, and shape of defects and statistical data (e. g. defect density) are important for many tasks. Data on defects are the starting point for inductive fault analysis [FeSh88] and realistic fault modeling [Maly87]. Defect statistics and systematic parameters like line width and space are used to characterize the process resolution [Mitc85] and to optimize the manufacturing process [LYWM86]. Moreover, these parameters play an important role in the development of design rules and for yield estimation [Stap86] [Ferr85] [Walk87]. Knowledge about fault probabilities is also useful for test pattern generation and the optimization of test pattern sets [SpSt93].

To determine significant data of these parameters test structures are used in separate lots [Spen83]. An online defect parameter monitoring requires the manufacturing of test chips side by side with standard chips. To enable a fast and effective (efficient) process control and characterization online test chips should fulfill the following conditions:

1. The test chips must have an extensive defect sensitive area for test structures.
2. The test chips must be tested by the same measuring equipment as the standard chips - a digital tester with a standard probe card.
3. The test chips and the standard chips must use the same standard boundary pad frame.
4. The position of the defects within a test chip must be localized for an additional optical test.

Section 2 describes methods to localize defects inside a large defect sensitive area. Section 3 deals with the diode checkerboard test structure design that fulfils the conditions above. Section 4 gives some experimental results.

2 Defect Localization

Generally a test structure contains a set of conductive layout objects (conductive components (cc)) which are possibly arranged in different layers. Comb structures (cf. figure 1 left) [Bueh83] [LYWM86] [Walk87] aim at extra material defects. These defects can cause a short between isolated lines (usually designed as combs) and thus significantly reduce the resistance measured between the pads. Meandering strings (cf. figure 1 right) [Bueh83] [LYWM86] [Walk87] are applied to detect missing material defects. If these defects are large enough, they interrupt the connection between the pads and increase the measured resistance very much.

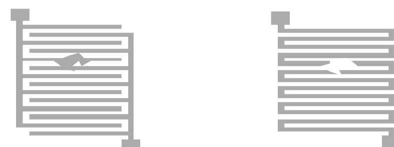


Fig. 1: Basic test structures to detect short circuit (left) and open circuit defects (right)

In [LYWM86] and [BCKJ91] a combined comb-string-comb structure has been proposed where a meandering string lies between two combs. The known test structures together with electrical measurements are appropriate to detect defects, but

they cannot give us details like the exact size and shape of a defect. Also they cannot tell us which process step is responsible for the defect. So in many cases an optical inspection is necessary. A picture of the defect can also help to answer the questions how the defect was produced during manufacturing (defect mechanism) and how the defect could cause faulty behavior (fault mechanism).

If we do not know the position of the defect, an optical inspection is very time consuming since the whole chip area must be scanned. So we need means to localize the defect first. The test structures of figure 1 and the comb-string-comb structure are not sufficient to solve the localization problem since the obtained data do not allow to conclude to the position of the defect.

An obvious approach to localization is to partition the chip area into a large number of small regions that can be analyzed separately. Combs, meandering strings, or other structures are designed so that they fit into these small regions. In order to deal with these subchips separately, each of them must be accessible to electrical measurements. If the subchips are arranged inside a 2 by N probe-pad array [Bueh79], the defect sensitive area is relatively small. To avoid this disadvantage we choose a boundary pad frame of standard chips. Then the number of pads is smaller, and if we connected each subchip to its own private pads in a straightforward way, only a small number of subchips could be implemented. So another approach is required.

In the following two methods are described that optimize the number of subchips and the connections to the pads. For a given number of pads we maximize the information available for localization procedures and hence the accuracy of localization. Without increasing the number of pads the number of detectable defects will be increased.

2.1 Open Circuits

Every test structure is connected to n pads inside a test chip. To assess the ability to detect a various number of different open circuit defects the whole test structure is modeled by the *geometry-graph* [HeWe94]. The nodes stand for the accessible measuring points (pads) and the edges represent all conductive layout objects (conductive component (cc)) like a comb or a meandrous line. Figure 2 shows a typical test structure to detect open circuit defects [LYWM86].

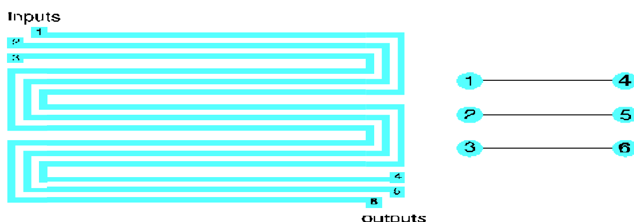


Fig. 2: Meandrous test structure (left) and its geometry graph (right)

In order to achieve a precise localization of open circuit defects, the chip should contain as many distinguishable meandrous lines as possible. Two lines are distinguishable, if a defect located in one line can be distinguished from a defect in the other line using only electrical measurements at the pads. Lines are distinguishable if they are connected to different pairs of pads where each pad belongs to a different set of pads. Each of these pad pairs corresponds to a directed edge of a bipartite geometry-graph (geometry-digraph), where all nodes are splitted into two different sets of pads (input nodes E_j and output nodes A_i) and all edges are directed from the inputs to the outputs. Hence this geometry-digraph should have as many edges as possible. For n pads the digraph having $(\frac{n}{2})^2$ directed edges is the best solution. The realization of this digraph leads to the well-known array of diodes [LiBL85] [WWRH90] [WWGH92].

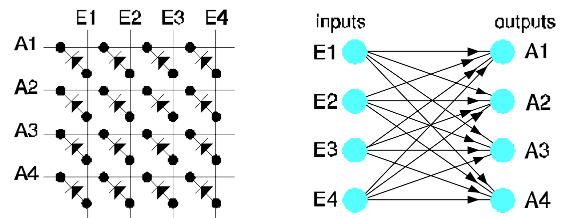


Fig. 3: Array of diodes (left) and its geometry digraph (right)

2.2 Short Circuits

A maximal set of conductive components (layout objects) and measuring points that are connected to each other is called a maximal conductive component (mcc). Each mcc should contain at least one pad. To assess the ability to detect a various number of different defects, the whole test structure is modeled by the *neighborhood-graph* [HeWe94]. Each node represents one mcc of the fault-free test structure. Two nodes mcc_1 and mcc_2 are connected by an edge if and only if in some region of the test structure a layout object of mcc_1 and a layout object of mcc_2 lie side by side or one on top of the other with only nonconducting material between them. Thus the edges correspond to shorts that can be caused by defects (undesigned shorts).

Figure 4 shows a test structure with 5 subchips that each corresponds to the comb structure of figure 1. Every node of the neighborhood-graph represents one single-sided or doublesided comb and the pad connected to it. For n=6 mcc's only n-1=5 edges are implemented.

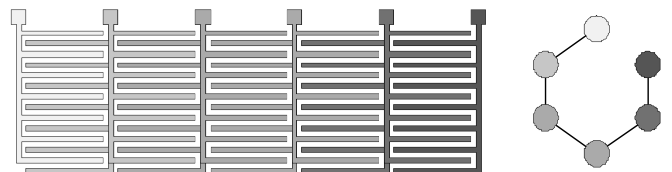


Fig. 4: Comb structure (left) and its neighborhood graph (right)

In order to achieve a precise localization of defects, the chip should be partitioned into as many distinguishable subchips as possible. Two subchips are distinguishable if a defect located in one subchip can be distinguished from a defect in the other subchip using only electrical measurements at the pads. Clearly,

subchips are distinguishable if they contain different pairs of mcc's. Each of these mcc pairs corresponds to an edge of the neighborhood-graph. Hence the neighborhood-graph should have as many edges as possible. For n mcc's, the complete graph having ½·n·(n-1) edges is the best solution.

For that the following **2D-permutation procedure** arranges the subchips in regular rows and columns. Figure 5 shows the situation in a row of subchips. The mcc's are numbered from 1 to n, in this example we have n=8. As every subchip contains a pair of neighboring mcc's, we get n-1 subchips in a row.

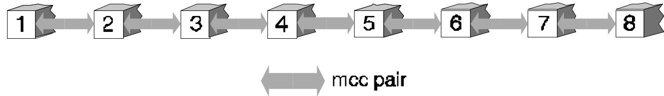


Fig. 5: Mcc's in a row of subchips

In every row all the mcc's are present, but the mcc's are permuted such that all pairs of neighboring mcc's occur. The neighborhood relationships can be represented by a $n \times \frac{n}{2}$-matrix, called 2D-matrix. Each row of the matrix corresponds to a row of subchips and shows the order of the mcc's in this row. The 2D-matrix is constructed using the following equations:

$$
h(i,j) := \begin{cases}
j+2\cdot i-2 & \text{if } \frac{j}{2}\in\mathbb{N} \wedge i \le \frac{m-j+2}{2} \quad \textbf{(1a)} \\
2\cdot m-j-2\cdot i-3 & \text{if } \frac{j}{2}\in\mathbb{N} \wedge i > \frac{m-j+2}{2} \quad \textbf{(1b)} \\
2\cdot i-j-1 & \text{if } \frac{j+1}{2}\in\mathbb{N} \wedge i > \frac{j+1}{2} \quad \textbf{(1c)} \\
j-2\cdot i+2 & \text{if } \frac{j+1}{2}\in\mathbb{N} \wedge i \le \frac{j+1}{2} \quad \textbf{(1d)}
\end{cases}
$$

i,j : row index, column index of 2D-matrix

Figure 6 shows a 2D-matrix for n=8 mcc's where in the rows each of the 7·4=28 different mcc pairs occurs once. The gray shaded numbers show all possible neighborhood relationships for the mcc_1 which are also marked with bold edges in the neighborhood-graph.

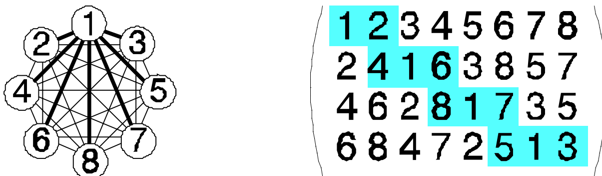


Fig. 6: Neighborhood graph (left) and 2D-matrix (right) for n=8 different numbers (mcc's)

The 2D-permutation procedure is applicable for all positive integer values n that are even.

3 Diode-Checkerboard Test Structure (DCTS)

In this section, the localization procedures described above will be combined to design a novel test structure, where open and short circuit defects are detectable and locatable inside an extensive defect sensitive area.

3.1 Design Principles

All available pads are numbered from 1 to n and splitted into different subsets. At least 2 different subsets with $m=\frac{n}{2}$ pads are required for the inputs E_j and outputs A_i. The procedure to localize open circuit defects (cf. subsection 2.1) will be applied to the elements of the subsets A and E. The procedure to localize short circuit defects (cf. subsection 2.2) will be applied to the elements of the subset E. If also topological effects shall be determined, a third subset of pads is required. This set represents the mcc's of underlying structures in buried layers.

elements of set	index	placement
$E_j \in E$	$j = 1, 2, .. m$	2D-permutation procedure
$A_i \in A$	$i = m+1, m+2, .. 2\cdot m$	top $(i=m+1)$ → down $(i=2\cdot m)$
$U_i \in U$	$i = 2\cdot m+1, 2\cdot m+2, .. 5\cdot \frac{m}{2}$	top $(i=2\cdot m+1)$ → down $(i=5\cdot \frac{m}{2})$

Tab 1: Distribution of all available pads (numbered: 1, 2, .. n) to different mcc's and localization procedures

To realize the m² lines (edges of the geometry-digraph) a diode array will be used between the E_j and A_i pads. The detection of all ½·m·(m-1) possible short circuit defects (edges of the neighborhood-graph) will be achieved by using a 2D-matrix for all mcc's which are connected to the E_j pads. Both principles will be mixed in a way shown in figure 7. Starting point is the diode-array of figure 3 in section 2.1. Every second line of diodes will be mirrored and moved which results in the construction in the middle of figure 7. Finally the E_j mcc's have to be permutated corresponding to the 2D-permutation procedure (cf. figure 7 right).

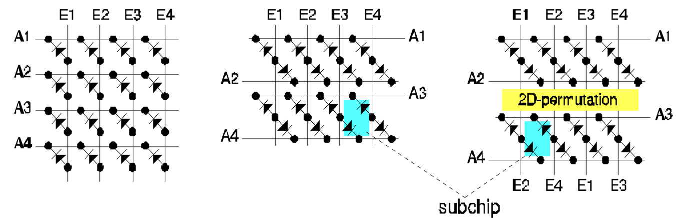


Fig. 7: Test structure design principle

Each of the $\frac{m}{2}\cdot(m-1)$ subchips resulted from this mixture will be filled with 2 meandrous lines as can be seen in figure 8.

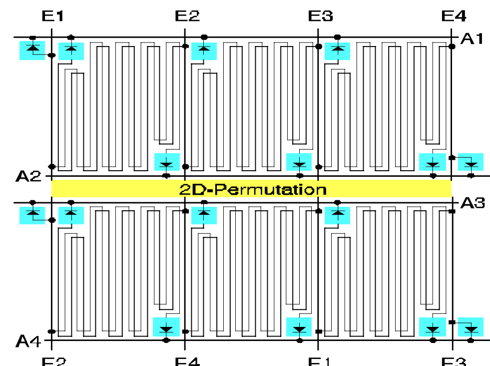


Fig. 8: Diode checkerboard test structure design (m=4)

All subchips contain m²-m distinguishable lines. At the left and right border of the DCTS, m reference diodes are placed which enable the determination of parasitic influences like diode open and short circuits. The meandrous lines can be designed solid (cf. fig. 8) or as via strings (cf. fig. 9) whose dimensiones can vary in each subchip. It shouldn't be forgotten that the lines have to be connected like "E_j → meandrous line or via string → diode → A_i".

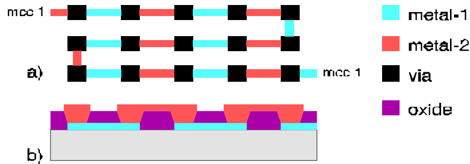


Fig. 9: mcc formed to a via-string
a, top view b, cross section

Underlying topography can have a very detrimental influence on conducting layers' integrity. To investigate this 3D-influence test chips should contain underlying structures, which are placed and connected as can be seen in figure 10.

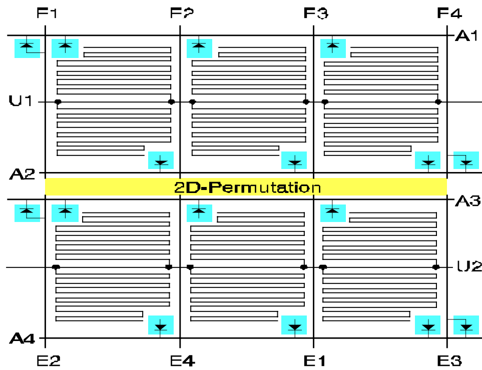


Fig. 10: DCTS underground structures (m=4)

Finally the subchips will be arranged in a standard boundary pad frame. Each mcc (A_i, E_j, U_i) is placed at the boundary at least two times, and 3 or 4 different mcc's lie next to each pad (cf. figure 11). So the connection of the mcc's to the pads is very simple and does not require any additional layout area.

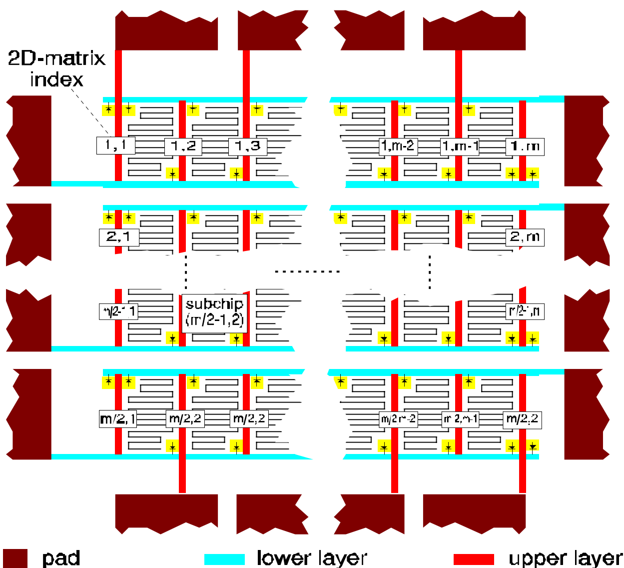
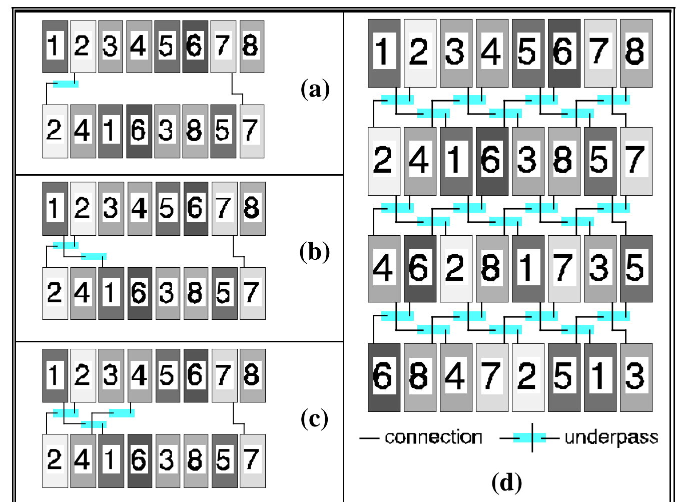


Fig. 11: Test chip design

3.2 2D-Permutation Routing Channel

The 2D-permutation requires a routing channel between the rows of subchips. Parts of the same mcc are represented by matrix elements that have the same value. All these parts must be connected. The permutations used in the 2D-matrix allow a very efficient routing with regular patterns. The channel can be composed of three basic wiring elements. Table 2 illustrates this for the example m=8. First the parts of mcc 2 and the parts of mcc 7 are connected using two basic elements (table 2 (a)). Then the parts of mcc 1 are connected by the third basic element (table 2 (b)). If mirrored horizontally, this element can also connect the parts of mcc 4 (table 2 (c)). These last two elements are then copied again and again until all parts are connected (table 2 (d), first row). In this way we only need space for two parallel horizontal lines in the routing channel. The channels between all subchip rows are equal (table 2 (d)).



Tab. 2: Design of the routing channels

3.3 Diodes

The implementation of the directed edges in the geometry-digraph requires diodes. Instead of normally implemented diode cells also CMOS transistors are usable. In this case the two different CMOS manufacturing process principles have to be distinguished because only the transistors in isolated wells are usable. Figure 12 shows the usable diodes in a n-well process and a p-well process including the connections of the E_j and A_i lines. According to figure 8 the connections to the anode and cathode of the diodes have to be exchanged, if a p-well process is used. The sequence "E_j → meandrous line or via string → diode → A_i" exists unchanged.

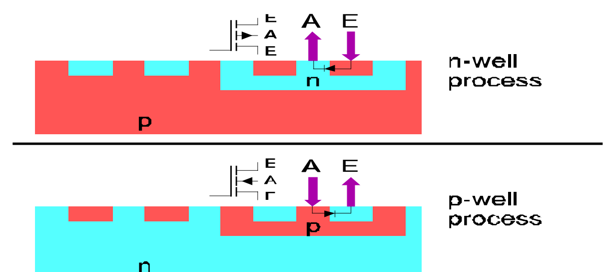


Fig. 12: DCTS test set

3.4 Measuring Procedure Using a Digital Tester

To measure the resistance of a test structure, commonly analog testers with a measurement frequency below 1 Hz are applied [BCKJ91] [MiFH92] [RoBF92]. In the context of this paper, an electrical test must only decide whether there is a defect or not. So in general a digital tester should be sufficient.

The results of experiments have shown that applying a digital tester is feasible [HeWe92] [HeWe94]. Using Ohm's law resistance measurements can be reduced to voltage measurements. A measured voltage above the threshold voltage indicates low resistance, while a measured voltage below the threshold voltage indicates high resistance. These measured values are assigned to possible defects according to the following table.

measured voltage	binary value	short circuit detected	open circuit detected
$V_{measured} \geq V_{threshold}$	1	yes	no
$V_{measured} < V_{threshold}$	0	no	yes

Tab. 3: Data conversion

To detect the defects inside a DCTS a "walking-one" over all E_j lines is sufficient while all other channels are measuring the voltage responses.

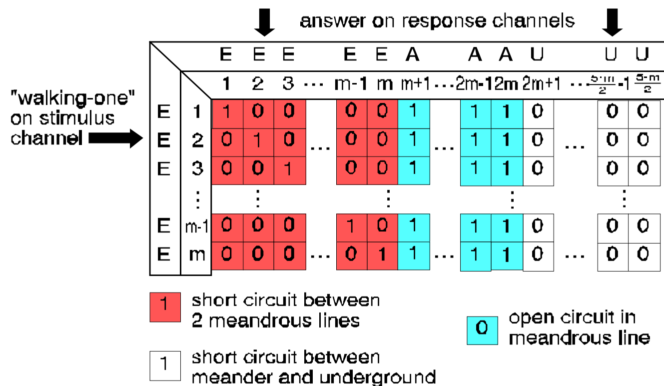


Fig. 13: DCTS test set

If a p-well process (with exchanged diode connections) is used the following alternative test set have to be used. In this case a "walking-one" over all E_j and all A_i lines is required.

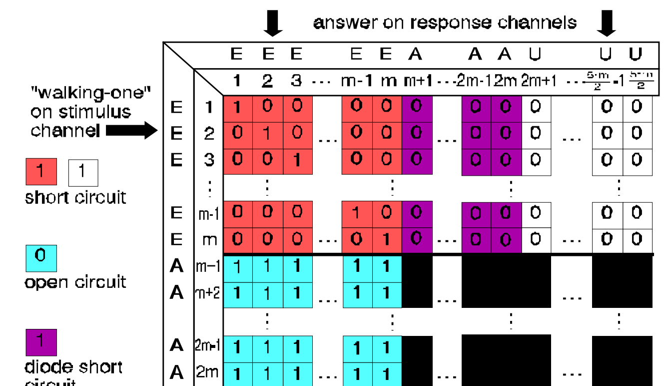


Fig. 14: DCTS alternative test set

3.5 Localization Procedures

If a defect occurs, two or more mcc's are connected or the implemented connection of two pads is interrupted, respectively. Since we know in which subchips specific mcc's are neighbors - or meandrous lines are placed - we can conclude to the subchip that contains the defect. The numbers of a list of k connected mcc's or of a pair (p,q) of separated pads, respectively, are the input to the localization procedure of table 4. This table contains the assignment to the defect types and the specific localization flow charts to compute the coordinates i and j of the subchips. The flow charts also use the equations of table 5. The described localization procedure can also handle multiple defects.

mcc 1	mcc 2	type of defect	see
∈ E (1,2, .. ,m)	∈ E (1,2, .. ,m)	short circuit between meandrous lines	flow chart of figure 16
∈ E (1,2, .. ,m)	∈ A (m+1, .. ,2·m)	open circuit of meandrous line	flow chart of figure 17
∈ E (1,2, .. ,m)	∈ U (2·m+1, .. , 5· $\frac{m}{2}$)	short circuit between meander and underground	flow chart of figure 15

Tab. 4: Assignment to defect types and localization procedures

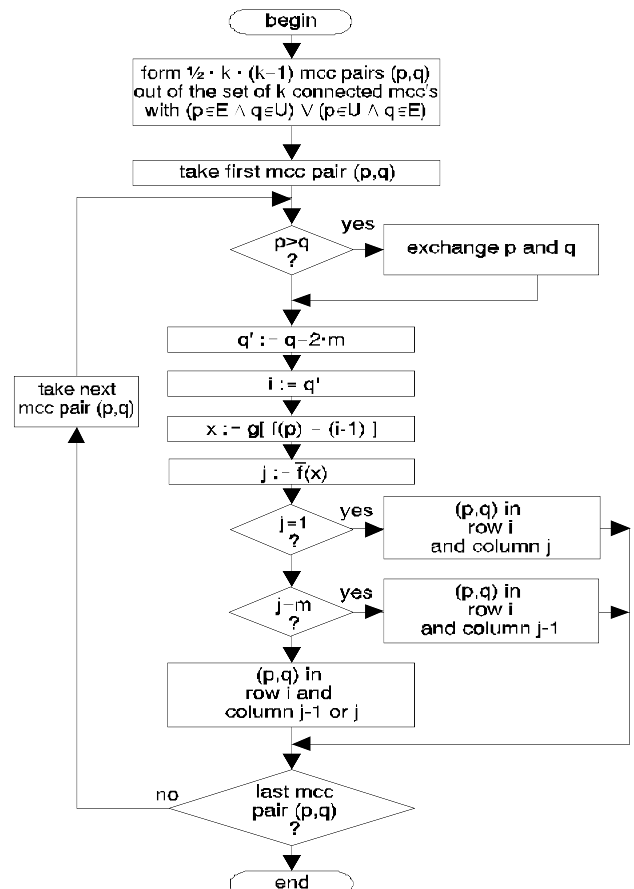


Fig. 15: Subprocedure *SEARCH "E"-"U"*

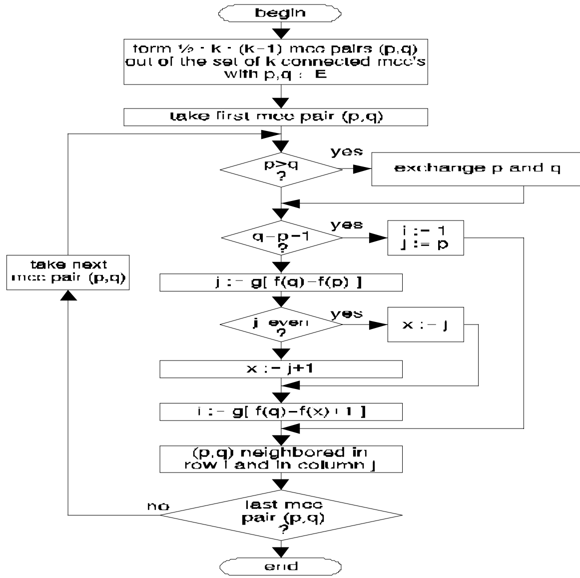


Fig. 16: Subprocedure *SEARCH "E"-"E"*

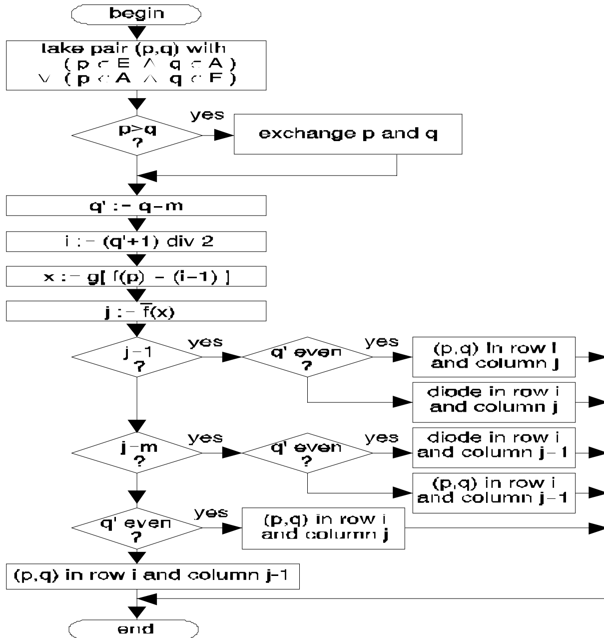


Fig. 17: Subprocedure *SEARCH OPEN CIRCUIT "E"-"A"*

$$f(x) := \begin{cases} \frac{x}{2} & \text{if } \frac{x}{2} \in \mathbb{N} \;\wedge\; 1 < x \leq m \\ m - \left\lceil \frac{x-1}{2} \right\rceil & \text{if } \frac{x+1}{2} \in \mathbb{N} \;\wedge\; 1 \leq x < m \end{cases} \quad \textbf{(2)}$$

$$\bar{f}(x) := \begin{cases} 2 \cdot x & \text{if } 0 < x \leq \frac{m}{2} \\ (m-x) \cdot 2 \quad 1 & \text{if } \frac{m}{2} < x \leq m \end{cases} \quad \textbf{(3)}$$

$$g(x) := \begin{cases} x & \text{if } 0 < x \leq m \\ x + m & \text{if } -m < x \leq 0 \end{cases} \quad \textbf{(4)}$$

Tab. 5: Functions used in the localization procedure

4 Experimental Results

To investigate the influence of underlying structures test chips containing a DCTS were manufactured side by side with standard chips on a number of wafers at the *Institut für Mikroelektronik Stuttgart* (**IMS**).

4.1 Test Structure Design

The test structure design bases on a crosswise arrangement of lines in two metal layers as can be seen in figure 18.

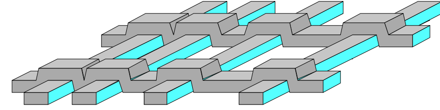


Fig. 18: DCTS subchip design

The topography of the underlying layers is represented by parallel lines with different spaces, which varies logarithmically. These lines are arranged in a comb structure, where each comb is connected with one pad ($U_i \in U$), so that intermetal shorts can be detected. In the upper layer meandrous lines are designed between the pads $A_i \in A$ and $E_j \in E$. The line width and space also vary logarithmically. Figure 19 shows some test structure details, where also implemented via strings are visible.

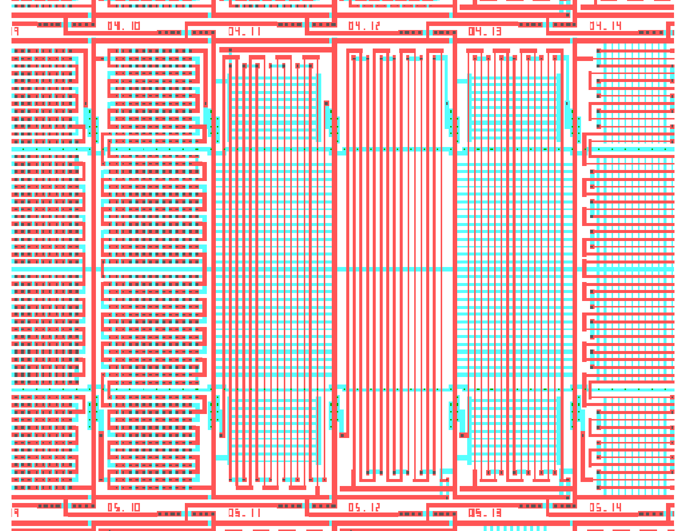


Fig. 19: Detail view of 5 subchips inside the DCTS

This figure shows clearly that this arrangement not only enables a precise defect localization but also guarantees an extensive defect sensitive area. More than 90% of the area inside the boundary pads is completely filled with defect sensitive structures. In comparison, a chip with the 2 by N probe-pads often utilizes less than 50% of the chip area for defect sensitive structures [Bueh83].

part of defect sensitive structures (subchips)	> 90 %
part of the routing channels	< 9 %
part of the pad connection lines	< 1 %

Tab. 6: Distribution of the area of the DCTS inside the boundary pad frame of a test chip

4.2 Measurement Results

Among other things the analysis of the digitally measured DCTS test chip data yields the defect distributions figured in the following table.

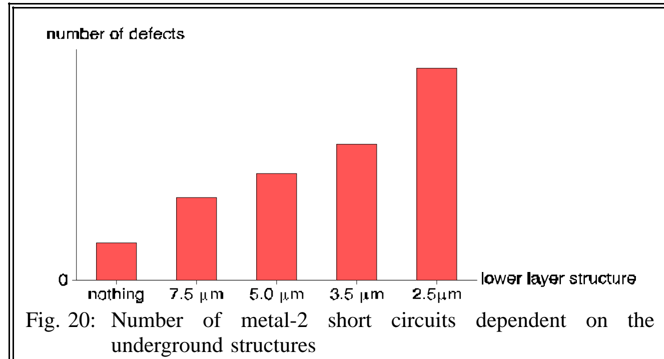


Fig. 20: Number of metal-2 short circuits dependent on the underground structures

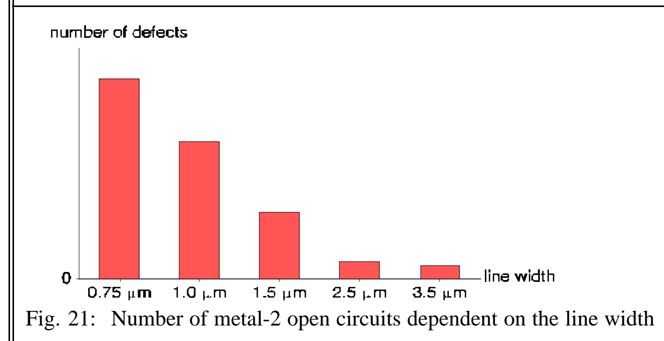
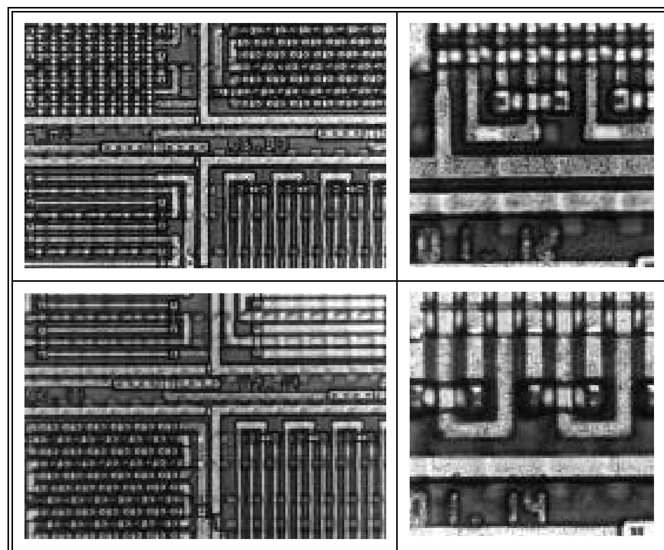


Fig. 21: Number of metal-2 open circuits dependent on the line width

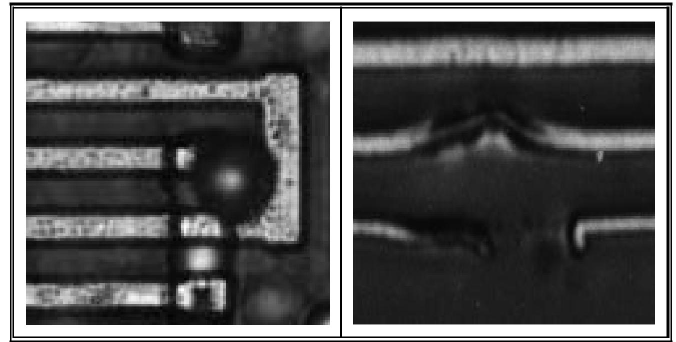
Tab. 7: Analysis of electrically measured DCTS test chips

Figure 20 shows the distribution of the metal-2 short circuits, where the number of defects is proportional to the line width. The overall distribution of the metal-2 open circuits can be seen in figure 21, where the number of defects is proportional to the line width. Table 8 gives some DCTS details, where the different contents of the subchips can be seen.



Tab. 8: DCTS details

Finally the following table shows some results of the additional optical defect inspection.



Tab. 9: Detected and photographed defects

5 Conclusion

A test structure is described, which cannot only be used alongside with standard chips as a process control monitor but also as a test chip to characterize wafer fabrication process resolution. The use of a digital tester guaranties a measuring procedure without any additional measuring effort (equipment and time). The digitally measured test structure data yield a precise defect detection and localization, which facilitates additional optical defect inspection. The test chip has an extensive defect sensitive area and can be easily designed. It is transferable to all other material layer configurations like CONDUCTING - ISOLATING - CONDUCTING - ... - ISOLATING - CONDUCTING.

Acknowledgment

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