Copy of: Proc. IEEE 1993 Int. Conference on Microelectronic Test Structures, Vol.6, March 1993

MODELING OF REAL DEFECT OUTLINES FOR DEFECT SIZE DISTRIBUTION AND YIELD PREDICTION

Christopher Hess, Albrecht Ströle

Institute of Computer Design and Fault Tolerance (Prof. Dr. D. Schmid)
University of Karlsruhe, P. O. Box 6980
W-7500 Karlsruhe 1, Germany

Abstract:

For efficient yield prediction defects are usually modeled by circular discs or squares. This paper presents a more accurate model that considers the real outline of physical defects. To utilize this model only the maximum and the minimum extension of detected defects have to be determined. That can be done easily using a checkerboard test structure including a defect localization procedure.

1 Introduction

The frequency of defects and the defect size distribution are important data for inductive fault analysis and yield prediction. In order to avoid the time-consuming computations required by complex defect shapes, defects are usually modeled as circular discs [Stap83], [Stap84], [Ferr85], [Walk87], [Maly90], [MVM90] or squares [GyDi92]. However, real defects show a great variety of different shapes. In literature there is no precise answer to the question of how to determine the diameter of the circular disc model for real defect data.

In yield prediction the defect size distribution affects the probability, that a defect causes a fault in the implemented electrical network. If the diameter of the circular disc model is determined as the maximum extension of the real defect (see fig. 1 [Spie91]), the probability of causing a fault is estimated too high.

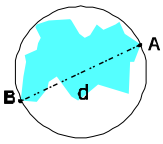


Fig. 1: Circular disc model

This paper presents an improved model for the outlines of defects and gives a procedure to extract the required parameter values from real defect data. Section 2 describes the checkerboard test structure that facilitates the defect localization and the observation of the defect shapes. Section 3 shows the novel approach of defect modeling. Section 4 gives some experimental results.

2 Checkerboard Test Structure (CTS)

For detecting a significant number of random defects which can cause short circuits in a 2 metal layer process, a test structure with large defect sensitive area is required. Furthermore defect localization is necessary to determine the size and outline of defects precisely using optical measurement equipment. The **checkerboard test structure (CTS)** fulfils these demands and in addition allows to use a standard boundary pad frame for the electrical measurement procedure [HeWe92]. Section 2.1 describes the test structure design, section 2.2 deals with the defect localization procedure, and section 2.3 shows some CTS data.

2.1 Checkerboard Test Structure Design

Normally a voltage can be measured between two pads of a test chip, so that every test chip can be modeled with a graph. The nodes stand for the pads and the edges represent the possible connections between the pads, therefore called potential pairs. Figure 2 shows on the left side a well known comb test structure [Bueh83], [LYWM86], [Walk87] and its graph. By using the n boundary pads of a standard chip, usually only n-1 edges are implemented which represent the undesigned short circuits.

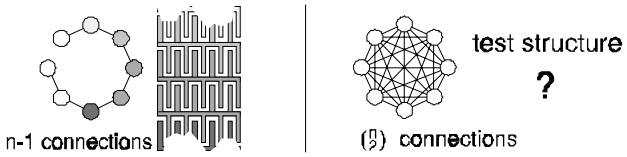


Fig. 2: Graphs and test structures

The **3D-permutation procedure** enables a test structure design, where all possible $\binom{n}{2}$ edges are implemented (fig. 2 right) in a material layer configuration like CONDUCTING, ISOLATING, CONDUCTING (fig. 3).

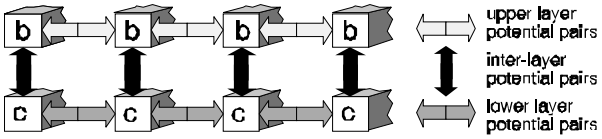


Fig. 3: Potential pairs

For a test chip with n=2·m pads the elements $b_{i,j}$ and $c_{i,j}$ of the 3D-permutation procedure are arranged in a **3D-matrix** with m rows and m columns, where $b_{i,j}$ represents a potential number of the upper layer ($1 \le b_{i,j} \le m$) and $c_{i,j}$ represents a potential number of the lower layer ($m < c_{i,j} \le n$). Figure 4(a) shows a general 3D-matrix and figure 4(b) shows the 3D-matrix for n=8, m=4.

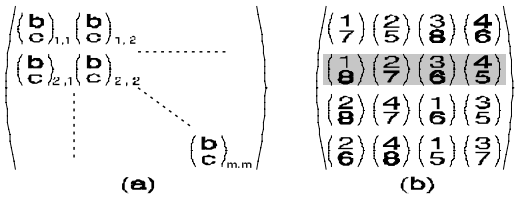


Fig. 4: General 3D-matrix (a)
and 3D-matrix for n=8 potentials (b)

The flow table of the 3D-permutation procedure for calculating the potential numbers $b_{i,j}$ and $c_{i,j}$ is shown in figure 5. It uses the equation (1) with an integer value $m=\frac{n}{2}$.

$$h(i,j):=\begin{cases} j \quad 2\cdot i-2 & \text{where } \frac{j}{2}\in\mathbb{N} \ \wedge \ i\le \frac{m-j-2}{2} & \textbf{(1a)} \\ 2\cdot m-j-2\cdot i-3 & \text{where } \frac{j}{2}\in\mathbb{N} \ \wedge \ i> \frac{m-j+2}{2} & \textbf{(1b)} \\ 2\cdot i-j-1 & \text{where } \frac{j-1}{2}\in\mathbb{N} \ \wedge \ i> \frac{j+1}{2} & \textbf{(1c)} \\ j-2\cdot i \quad 2 & \text{where } \frac{j \quad 1}{2}\in\mathbb{N} \ \wedge \ i\le \frac{j \quad 1}{2} & \textbf{(1d)} \end{cases}$$

i,j : row index, column index of 3D-matrix

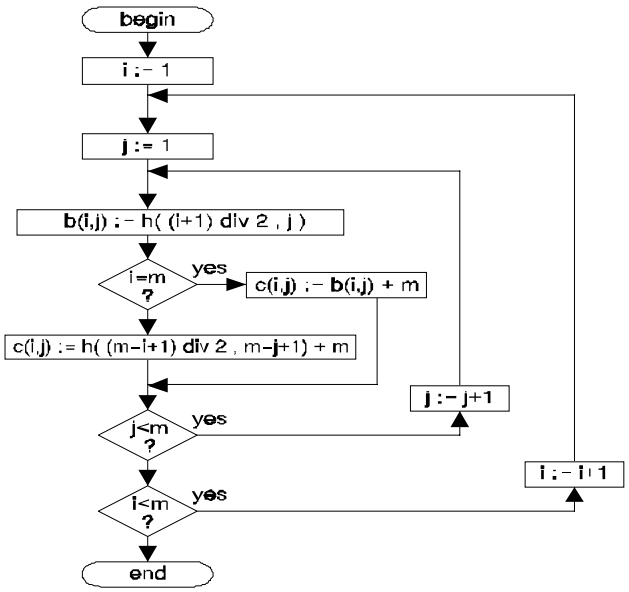


Fig. 5: 3D-permutation procedure where $\frac{m}{2}\in\mathbb{N}$

Each row of the 3D-matrix will be transferred into a test structure layout as can be seen in figure 6 for the light gray shaded row 2 of figure 4(b). The potential pairs are also shown with different shaded arrows. Theoretically in each of the $\frac{n}{2}\cdot(\frac{n}{2}-1)$ subchips a different test structure can be placed. In this paper, superimposed combs are used in both metal layers as defect monitors in a subchip. The combs are sized in relationship to the expected defects.

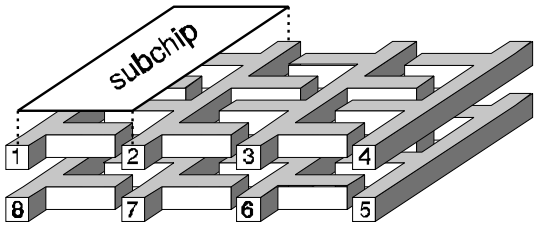
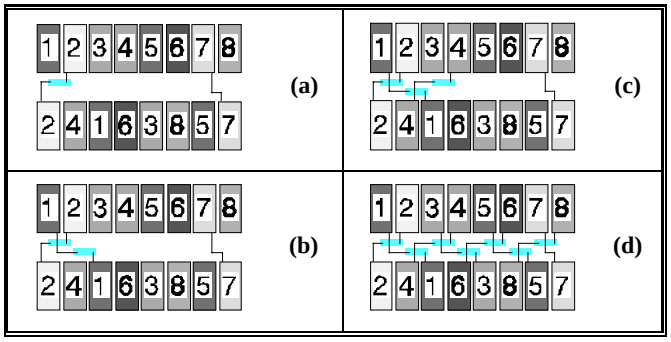


Fig. 6: Subchip layout with the specification of the potential pairs

Only 2 horizontal parallel wires are required in a routing channel between the subchip rows or the 3D-matrix rows, respectively. The channel is composed of only 3 basic routing elements as can be seen in table 1, where the example m=8 and the permutation of the upper layer was chosen. First the lines "2" and "7" are connected with two basic elements (tab. 1 (a)). Then the lines "1" are connected with the third basic element (tab. 1 (b)). This element also connects the lines "4" after copying and horizontal mirroring (Tab. 1 (c)). These two elements ("1" + "4") are now copied again and again until all lines are connected (Tab. 1 (d)).



Tab. 1: Routing channel composition

So, only a minimum of additional layout effort and additional layout area is necessary, because this routing channel is the same between all subchip rows (cf. fig 7) if the following rules are applied:

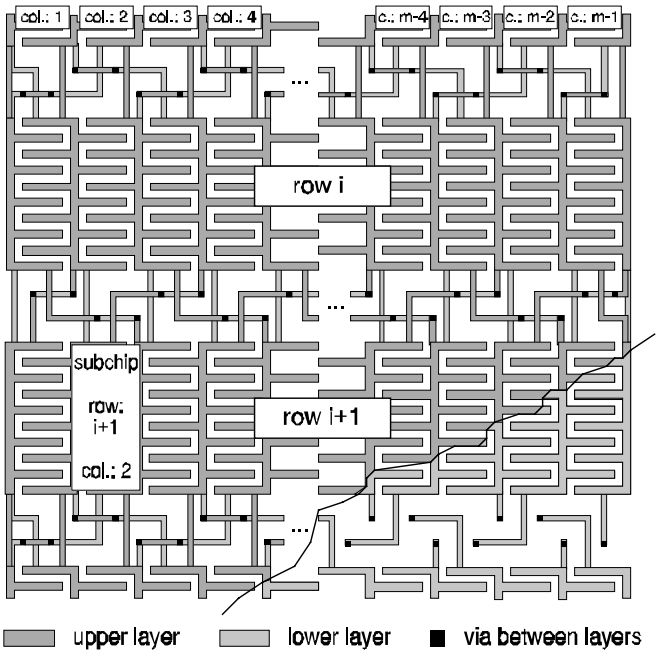


Fig. 7: Wiring between the subchip rows where i is even

- In a routing channel between an odd subchip row i-1 and an even subchip row i the lower layer is permutated while the upper layer is connected directly.
- In a routing channel between an even subchip row i and an odd subchip row i+1 the upper layer is permutated while the lower layer is connected directly.

Each potential number is placed at least three times at the boundary of the 3D-matrix. 3 or 4 different potential numbers lay beside every pad. So the connection of the potential numbers to the pads is trivial and will be achieved without any additional layout effort and layout area as can be seen in figure 8. More than 90% of the area inside the boundary pads of a standard chip is completely filled with defect sensitive test structures. (A test chip with the 2-by-N pads often uses less than 50% of the chip area [Bueh83].)

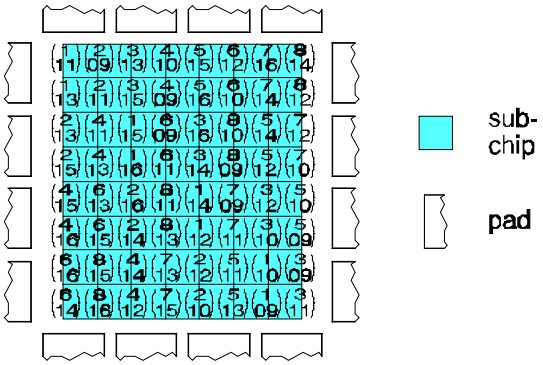


Fig. 8: Connection of the potentials to the n=2·m boundary pads

2.2 Defect Localization Procedure

In case of a short circuit two (or more) potential numbers are connected inside a CTS. The localization of the defect is possible due to the analysis of the connected potential numbers. To ascertain the subchip row i and column j (cf. fig. 7) it is necessary to use the procedure which is described in the flow table of figure 9. The subprocedures "SEARCH UPPER", "SEARCH LOWER" and "SEARCH INTER" are illustrated in the flow tables of the figures 10-12, where the equations of table 2 are required.

$$f(x):=\begin{cases}\dfrac{x}{2} & \text{where } \dfrac{x}{2}\in\mathbb{N} \ \wedge\ 1<x\le m \quad \textbf{(2a)}\\[2ex] m-\left[\dfrac{x-1}{2}\right] & \text{where } \dfrac{x+1}{2}\in\mathbb{N} \ \wedge\ 1\le x<m \quad \textbf{(2b)}\end{cases}$$

$$\bar{f}(x):=\begin{cases}2\cdot x & \text{where } x\in\mathbb{N} \ \wedge\ 0<x\le \dfrac{m}{2} \quad \textbf{(3a)}\\[2ex] (m-x)\cdot 2-1 & \text{where } x\in\mathbb{N} \ \wedge\ \dfrac{m}{2}<x\le m \quad \textbf{(3b)}\end{cases}$$

$$g(x):=\begin{cases}x & \text{where } x\in\mathbb{N} \ \wedge\ 0<x\le m \quad \textbf{(4a)}\\ x\ \ m & \text{where } x\in\boldsymbol{Z} \ \wedge\ -m<x\le 0 \quad \textbf{(4b)}\end{cases}$$

Tab. 2: Search functions

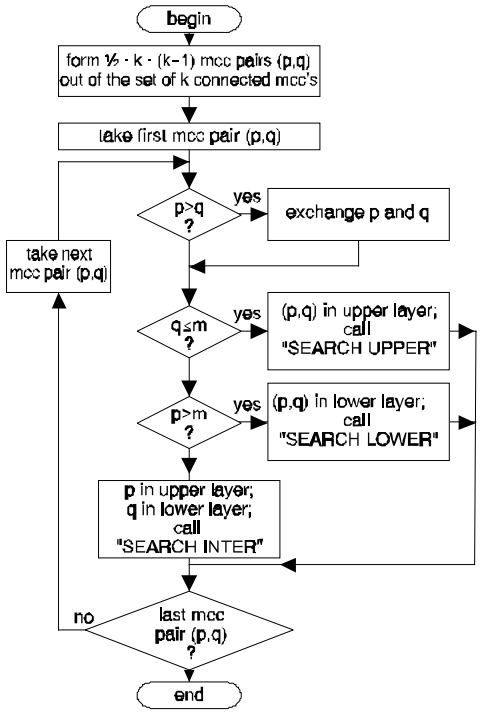


Fig. 9: Defect localization procedure where k≥2 is the number of connected potentials

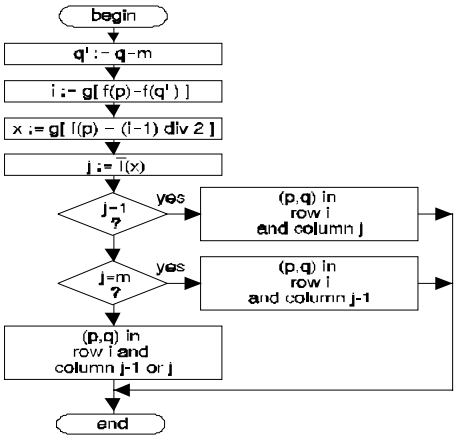


Fig. 10: Subprocedure "SEARCH INTER"

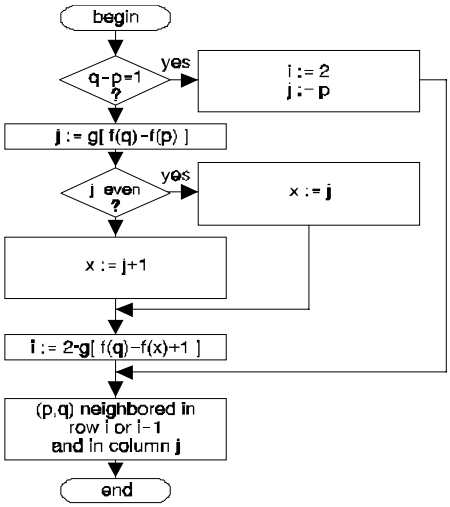


Fig. 11: Subprocedure "SEARCH UPPER"

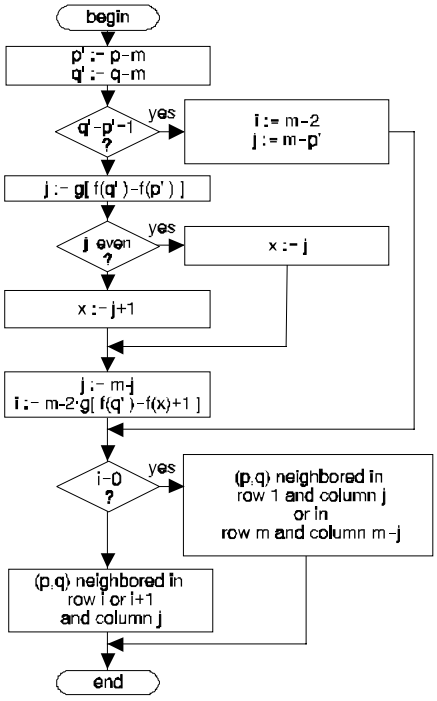


Fig. 12: Subprocedure "SEARCH LOWER"

2.3 Measured CTS Data

Different test chips were manufactured at the *Institut für Mikroelektronik Stuttgart* (**IMS**). The test chips contain 870 subchips with a test structure design far below the valid IMS design rules. All process steps were performed according to the IMS 2 µm CMOS backend process. All lithography steps were performed via electron beam direct write. Due to the small test structure design, the density of virtual vias (intermetal shorts) and metal-2 shorts could be above the average, especially on topography. This gives a better opportunity to verify the defect localization procedure.

The analysis of the electrically measured data allows the detection and localization of defects inside the subchips of the CTS, which facilitates an additional optical measurement for determining the sizes and outlines of the defects.

Figure 13 shows typical defect shapes. The ratio between the maximum extension and the minimum extension ranges between 1 and more than 3. The ratio data of more than 200 defects are summarized in figure 14. The shown relative frequency is practically independent of the defect size.

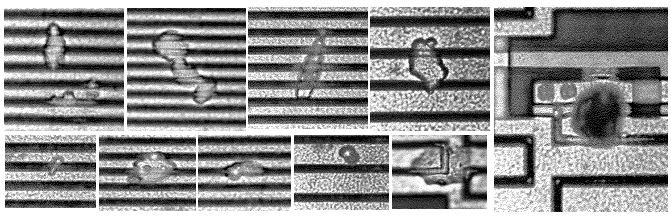


Fig. 13: Typical defect shapes

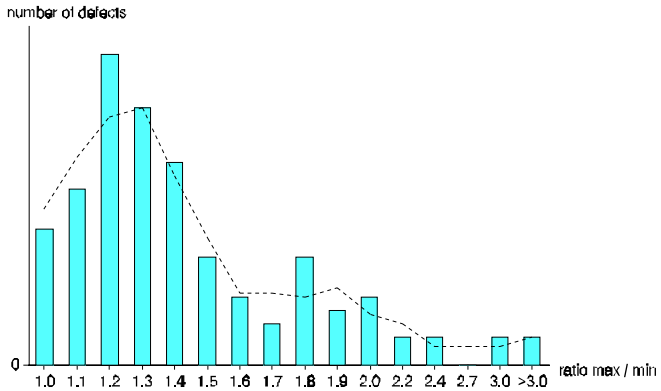


Fig. 14: Ratio between the maximum (max) and minimum (min) extension of a defect

These results make clear, that a circle with a diameter equal to the maximum extension of the defect cannot be an accurate model of real defect outlines.

3 Defect outline modeling

To make the application of the model easy, the defect outline should be transformed into a circle. The diameter of this circle has to be determined such that the probability that the circular defect causes a fault is the same as the probability that the real defect causes a fault. Since in general the grids used for layouts are orthogonal and the subchips of the CTS have parallel comb lines, it is appropriate to measure the extension of a real defect between two parallel staight lines, which touch the defect as can be seen in figure 15. The defect extension (dependent on the angle φ) corresponds to the distance d' or d", respectively, between the two straight lines. The angle φ' or φ", respectively, is measured between the comb lines and the straight lines.

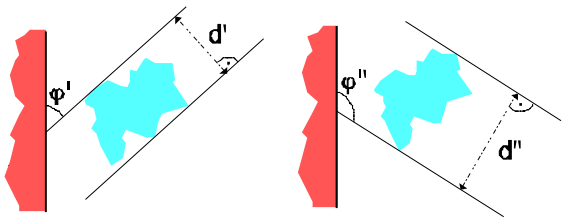


Fig. 15: Measurement of the real defect extension

The orientation of the defect is defined as the angle φ_0 where d(φ) reaches its minimum. The analysis of the detected defects has shown, that the distribution of the orientation is almost uniform for φ=0° .. 180°. Then the average extension of a defect with respect to an arbitrary but fixed direction ψ is

$$\bar{d} := \frac{1}{180°} \cdot \int_{\varphi=\psi}^{\varphi=\psi+180°} d(\varphi)\, d\varphi \qquad (5)$$

In order to reduce the high cost of measuring a large number of d(φ) values, the defect outline can be modeled by an ellipse that is determined by the maximum extension and the minimum extension of the real defect (see fig. 16).

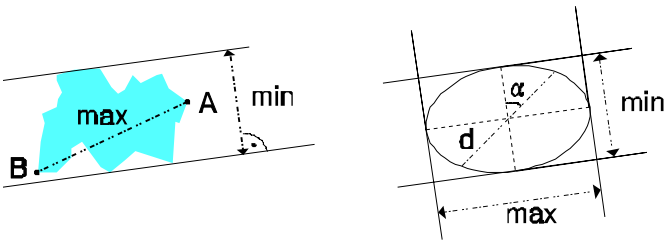


Fig. 16: Maximum (max) and minimum (min) extension of a defect and the elliptical model

Using the elliptical model we have

$$d(\alpha) = \frac{\min}{\sqrt{1-\left(1-\left(\frac{\min}{\max}\right)^2\right)\cdot\sin^2\alpha}} \qquad (6)$$

and choosing an appropriate value ψ the average extension is

$$\bar{d} = \frac{\min}{180°}\cdot\int_{\alpha=0}^{\alpha=180}\frac{d\alpha}{\sqrt{1-k^2\cdot\sin^2\alpha}} \qquad (7)$$

$$\text{where} \quad k = \sqrt{1-\left(\frac{\min}{\max}\right)^2}$$

An analytical solution of this first order elliptical integral is not known [RHJ71], but it can be computed numerically. Alternatively the approximation

$$\bar{d} \approx \tfrac{1}{2}\cdot\sqrt{\min\cdot\max}\quad\frac{\min\cdot\max}{\min-\max} \qquad (8)$$

can be applied. For $\frac{max}{min} \le 4$ the approximation error is less than 1%. So for almost all cases (cf. fig. 14) the value of $\bar{d}$ is estimated very precisely (fig. 17).

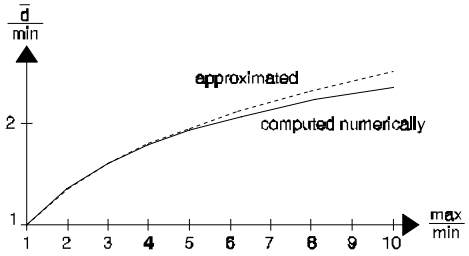


Fig. 17: Values of the normalized average extension $\bar{d}$/min for different ratios $\frac{max}{min}$

Figure 18 summarizes the approach, where the real defect is first modeled by an ellipse and then this ellipse is transformed into a circle with the same probability of causing an open line or a short circuit between parallel lines, respectively.

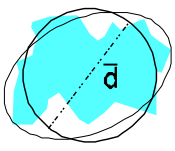


Fig. 18: Defect modeling

4 Experimental Results

Two CTSs, CTS A and CTS B, with comb lines of different width (see fig. 19) were manufactured side by side on a number of wafers for eliminating possible wafer cluster effects. As both have the same defect sensitive area, yield prediction is simplified. Only defects of type "extra material" are considered.

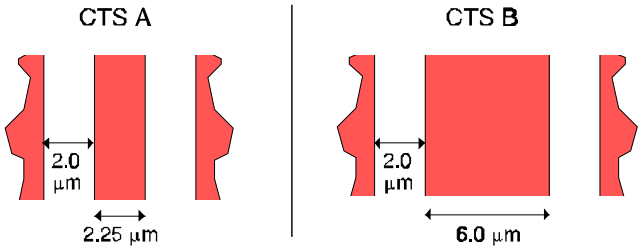


Fig. 19: Manufactured test structures

The analysis of the CTS A with the finer combs (using the localization and optical measurement procedure of section 2.3) yields the defect size distribution of figure 20. The left bar of each size interval shows the size distribution using the max circle model of figure 1. The bars in the center represent the size distribution using the elliptical model which was described in section 3. The right bars show the size distribution using the min circle model, where the diameter is chosen equal to the minimum extension of the defect.

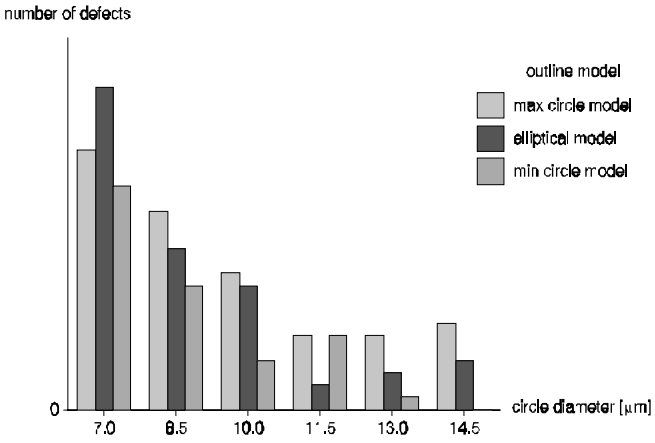


Fig. 20: Measured defect size distribution of CTS A

For each model figure 21 shows the sum of all the defects larger than 6,25 µm. All defects larger than 6,25 µm cause a short circuit with probability 1 and thus are detected with certainty.

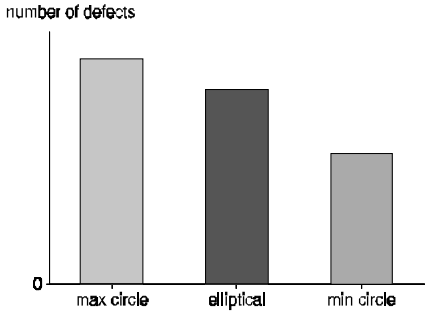


Fig. 21: Accumulated number of defects of CTS A

The same procedure was applied to CTS B with the coarser combs (fig. 22).

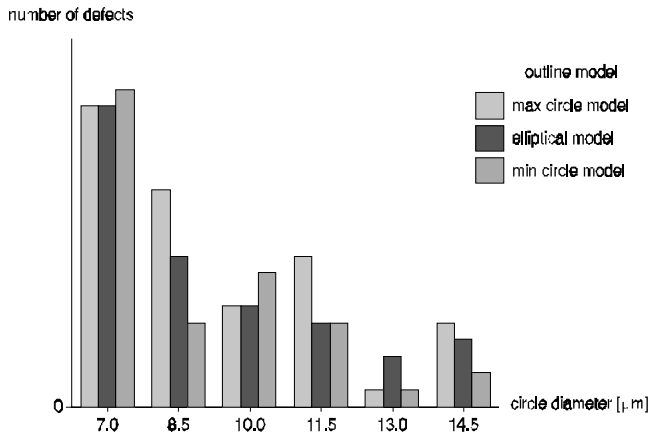


Fig. 22: Measured defect size distribution of CTS B

On the other hand the expected number of defects in CTS B can be predicted using the data of CTS A and the fault probability kernel described in [Stap84] and [Ferr85]. The fault probability kernel depends on the specific layout, but it is independent of the outline of defects. The probability kernels of CTS A and CTS B are shown in figure 23.

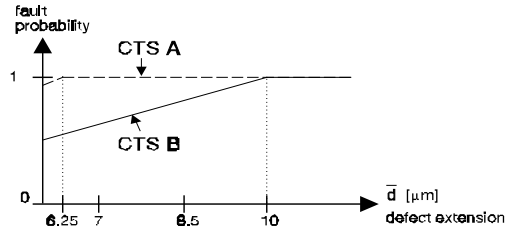


Fig. 23: Fault probability kernels

For each defect outline model the sum of all the measured defects larger than 6,25 µm is shown in figure 24 and compared with the expected value. The relative error between the predicted and the measured defect frequency is +7.5% for the max circle model, -17% for the min circle model, and -2% for the elliptical model. The differences among the measured frequencies are caused by the different methods of determining the diameters of the approximating circles.

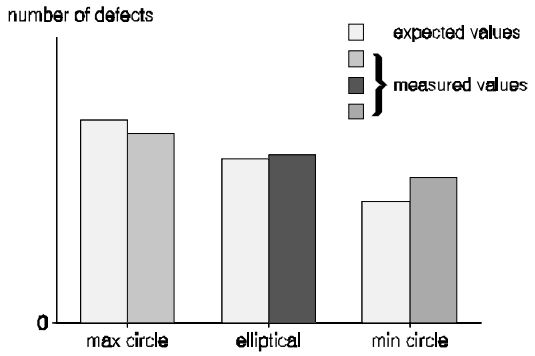


Fig. 24: Comparison between the expected and the measured defect frequency of CTS B

5 Conclusion

The accuracy of the predicted number of defects can be substantially enhanced by modeling real defect outlines with the elliptical model. Only the minimum and maximum extension of defects have to be measured. If the elliptical model of the defect outlines is applied, the defect size distribution implicitly contains the information about the physical defect outlines. Hence for yield prediction the inspection of defect outlines can be omitted.

If one uses the max circle model or the min circle model, which both neglect the defect outlines, the real defect outlines should be taken into account in a modified layout specific fault probability kernel. But that fails due to the high additional expense.

Acknowledgment

The authors thank L. Weiland (Institut für Rechnerentwurf und Fehlertoleranz, Universität Karlsruhe), Dr. H. Richter and B. Laquai (Institut für Mikroelektronik Stuttgart) for advice and assistance with testing procedures.

References

[Bueh83] Buehler, M. G.:
Microelectronic Test Chips for VLSI Electronics
Academic Press, New York, 1983

[Ferr85] Ferris Prabhu, A. V.
Modeling the Critical Area in Yield Forecasts
IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 4, Aug. 1985

[GyDi92] de Gyvez, J. P., Chennian, D.
IC Defect Sensitivity for Footprint-Type Spot Defects
IEEE Transactions on CAD, Vol. 11, No. 5, May 1992

[HeWe92] Hess, C., Weiland, L. H.
Test Structure for the Detection, Localization, and Identification of Short Circuits with a High Speed Digital Tester
ICMTS 92, San Diego, March 1992

[LYWM86] Lukaszek, W., Yarbrough, W., Walker, T. , Meindl, J.:
CMOS Test Chip Design for Process Problem Debugging and Yield Prediction Experiments
Solid State Technology, March 1986

[Maly90] Maly, W.
Computer-Aided Design for VLSI Circuit Manufacturability
Proceedings of the IEEE, Vol 78, No. 2, Feb. 1990

[MVM90] Michalka, T. L., Varshney, R. C., Meindl, J. D.
A Discussion of Yield Modeling with Defect Clustering, Circuit Repair, and Circuit Redundancy
IEEE Transactions on Semiconductor Manufacturing, Vol. 3, No. 3, August 1990

[RHJ71] Reutter, F., Haupt, D., Jordan, G.
Elliptic Functions of a complex variable nomograms and formulas
G. Braun, Karlsruhe, 1971

[Spie91] Spiegel, G.
Defektanalyse für die Repräsentation realistischer Fehlfunktionen in hochintegrierten Schaltungen
Inst. für Rechnerentwurf und Fehlertoleranz, Uni. Karlsruhe, 1991

[Stap83] Stapper, C. H.
Modeling of Integrated Circuit Defect Sensitivities
IBM J. Res. Develop., Vol. 27, No. 6, November 1983

[Stap84] Stapper, C. H.
Modeling of Defects in Integrated Circuits Photolithographic Patterns
IBM J. Res. Develop., Vol. 28, No. 4, July 1984

[Walk87] Walker, H.:
Yield Simulation for Integrated Circuits
Kluwer Academic Publisher, Boston, Dordrecht, Lancaster, 1987