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Issues on the Size and Outline of Killer Defects and their Influence on Yield Modeling

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Abstract **— Yield prediction models and critical area calculations base on defects modeled as circular disks. But, the observation of real defects provides mostly irregular defect outlines. For this reason, we investigate the influence of real defect outlines on determining defect size distributions for yield prediction. To collect data on defects, checkerboard test structures were manufactured that enable a precise localization of defects inside large chip areas. Furthermore, we introduce a methodology to calculate a general defect size distribution that includes variety of real defect outlines. So, this realistic size distribution will be compared to defect size distributions based on known yield models to describe defect outlines.**

1 Introduction

Dependent on the layout, defects (e. g. particles) can become the cause of electrically measurable faults (killer defects), which are responsible for manufacturing related malfunctions of chips. Decreasing time to market and faster scaling down of design rules demand precise yield prediction and failure analysis. A major factor in manufacturing smaller features is data on defect density and defect size distribution. Since the 70's, yield prediction models include defect size distributions based on a circular disk model to describe the outline of defects [StRo95], [Ferr85c], [Maly90], [Stap83], [Walk87]. But, what is today's outline of real process defects?

So, we decided to measure the outlines of some hundred defects and investigate their influence on determining defect size distributions for yield modeling. The following Section will describe the design principle of the checkerboard test structures that were manufactured to collect the required defect data. Section 3 gives the procedure to measure the size and outline of defects and we introduce our outline specific classification of defects. In Section 4, we present a methodology to provide a defect size distribution that reflects real outlines of defects. Then, in Section 5 we discuss the influence of defect outlines on yield modeling. Finally we conclude our approach.

2 Checkerboard Test Structure

A special test structure is required to enable an efficient optical inspection of random particle defects that results in electrically measurable faults. It should provide a *large defect sensitive area* to detect defects even if the average defect density is low. A *layer sensitive defect separation* is required to assign electrically detected defects to a specific layer. Only a *precise defect localization* inside the chip area will enable a precise optical measurement of the size and outline of the defects.

Two major methods to organize test chips are known, the "2 by N" probe-pad array [Bueh79] and standard boundary pads. The defect sensitive area inside a "2 by N" array is relatively small so that the large sensitive area inside the boundary pads seems to be more suitable. But here the number of pads is relatively small so that methods are required to separate defects. The checkerboard test structure based on the 2D-permutation procedure described in [HeSt94] enables the separation and localization of defects that results in electrically measurable faults inside a large chip area, even if the number of boundary pads is limited [Hess94], [HeWe95b], [HWLS96].

For that, checkerboard test structures partition the total chip area into a large number **n** of electrically distinguishable subchips to separate and localize defects.

$$n := \frac{p}{2 \cdot k} \cdot \left(\frac{p}{k} - 1 \right) \quad \textbf{(1)}$$

n : number of subchips
p : number of pads
k : number of conducting layers

The boundary of each subchip is marked by a unique set of test structure lines that are all connected to different pads. The following Figure 1 shows the frame of a designed checkerboard

test structure. Here, for example, all test structure lines connected to two pads are highlighted. Both lines are neighbored in one subchip only (row four and column ten).

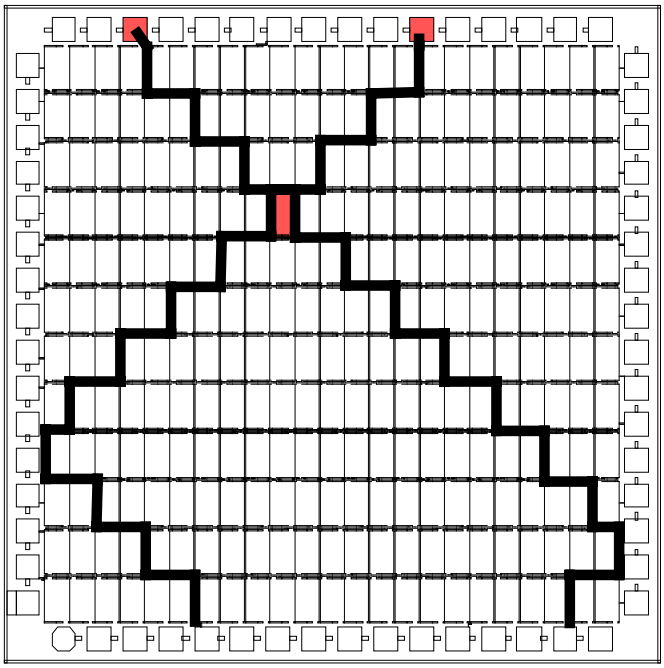

Fig. 1: Frame of a checkerboard test structure with 276 separable subchips.

Faults and defects will be detected inside the subchips. So, comb lines, meandrous lines or via strings will be designed inside the subchips to detect different types of faults which are the result of process specific defects (ref. Figure 2). They will be connected to the test structure lines that mark the boundary of each subchip.

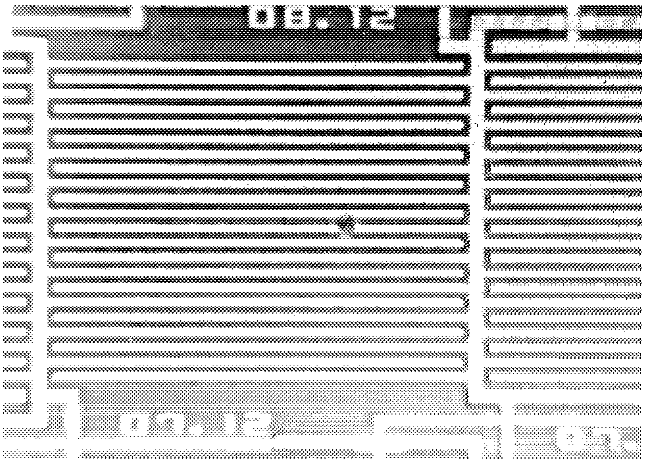

Fig. 2: Detail view of one subchip containing parallel comb lines.

If for example a short circuit occurs, two or more test structure lines are connected. Since we know in which subchips these specific lines are neighbored we can conclude to the subchip that contains the defect. Precise localization procedures are described in [HeSt94], [HWLS96] that also handle multiple faults.

Checkerboard test structures cannot only be used as defect monitors but also to characterize wafer fabrication process resolution. Furthermore, they will be manufactured alongside with standard chips as a process control monitor. More than 90% of the total chip area is completely filled with defect sensitive structures. However, the permutation procedure guarantees a precise localization of defects without the requirement of any additional active semiconductor devices. The systematically designed checkerboard framework enables a machine-assisted generation of test chips without any limitation to the number of layers.

3 Measurement and Classification of Defect Outlines

Generally, open and short circuits are detectable, testing the resistance between different pads. To measure the resistance of the test structures, a digital tester will be used, because the electrical test must only decide whether there is a defect or not [HeWe95d]. So, the measured values will directly assigned to possible defects. The use of a digital tester guaranties a measuring procedure without any additional measuring effort (equipment and time). Additional analysis procedures guarantee a layer-specific fault localization inside specific subchips that enables an efficient optical defect inspection to exactly determine the size and outline of each defect.

During the past five years, checkerboard test structures containing various subchip designs in interconnection layers were manufactured at the Institute of Microelectronics Stuttgart (IMS) in Germany, ALCATEL SEL in Germany, National Semiconductor (NSC) in Santa Clara CA, THESYS in Germany, and ELMOS in Germany. There, we measured the defect extension of hundreds of defects between parallel lines as can be seen in the following Figure (e. g. in $\Delta\varphi$=5° steps).

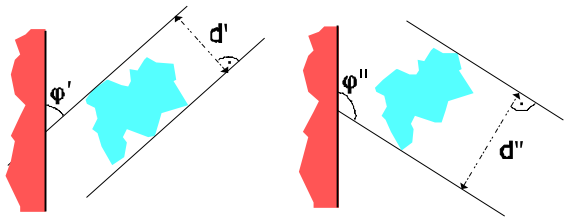

Fig. 3: Measurement of the extension of a defect in-between parallel lines.

For this reason, image-processing based tools were developed to provide curves to describe the defect extension (y-axis) dependent on the measurement angle (x-axis: 0°-180°) [Guga95]. The inspection of defects collected from several fabs always yield three basic types of curves:

Type-0: The defect extension varies within 25%, so that there are no clear relative maxima and minima (ref. Figure 4 and left defect in Figure 7).

Type-1: The defect extension varies more than 25% and the defect extension has exactly one clear maximum value within Δφ=±5° or exactly one clear minimum value within Δφ=±5° (ref. Figure 5 and middle defect in Figure 7).

Type-2: The defect extension varies more than 25% and the defect extension has two relative maxima within Δφ=±5° or two relative minima within Δφ=±5° (ref. Figure 6 and right defect in Figure 7).

The following three figures give some defect extension curves where f(0°) = f(180°) is valid. Figure 7 shows a typical defect of each outline type.

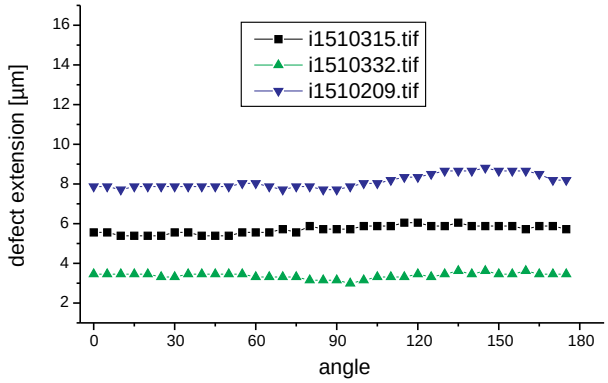

Fig. 4: Typical outline of type-0 defects.

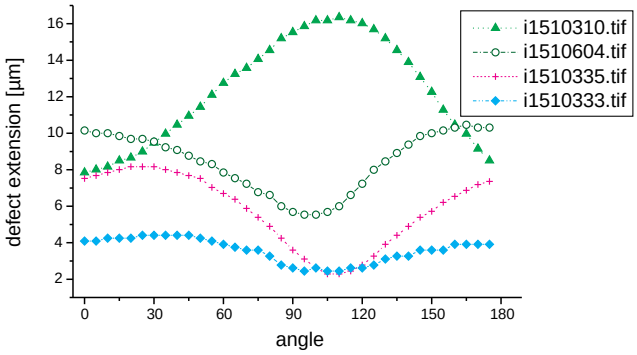

Fig. 5: Typical outline of type-1 defects.

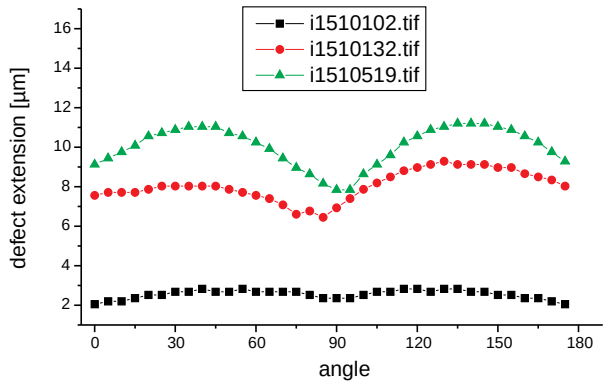

Fig. 6: Typical outline of type-2 defects.

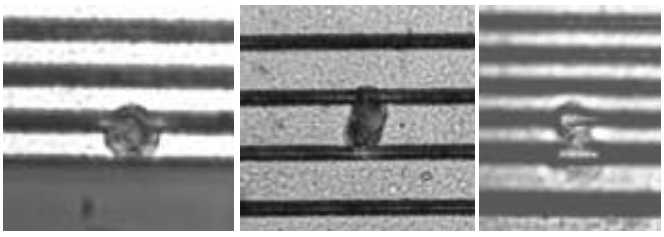

Fig. 7: Detected defects: Type-0 (left), type-1 (middle), type-2 (right).

We investigated the extensions of hundreds of defects without observing preferred defect orientations, which means that there is no preferred angle for maximum or minimum extensions. The classification of all inspected defects yields that 23% of them are type-0 defects. Just 10% of all defects are type-2 defects. So far we don't observe defects that have more than two clear maximum or minimum values if their extension varies more than 25%. Most defects (67%) are type-1 defects as can be seen in the following Figure 8.

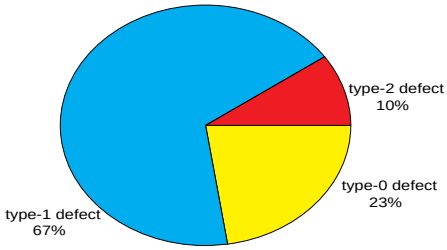

Fig. 8: Distribution of types of defect outlines.

4 Determination of Defect Size Distribution

Generally, just one extension value will be measured for each observed defect. Based on these values, a defect size distribution will be determined. The following Figure 9 gives the ratio between the maximum and minimum extension of all defects. Only the type-0 defects having a ratio of less than 1.25 fit to the generally used measurement procedure based on just one extension value per defect. But, what influence has the outline of all other defect types on determining defect size distributions? For that, we have to find a measurement procedure to provide a defect size distribution based on real outlines of defects.

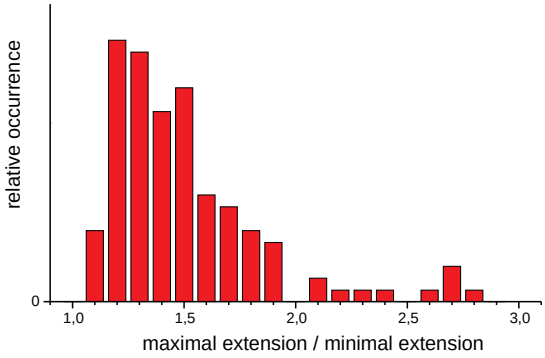

Fig. 9: Ratio between the maximum and minimum extension of defects.

Our intention is to model each defect as a so called *Micro Size Distribution*. Then, these distributions will be summarized in a general defect size distribution. For this reason, we measure the defect extension between parallel lines as described in Figure 3. We select equivalent measurement steps $\Delta\varphi$, so that we get

$$w = \frac{180°}{\Delta\varphi} \qquad \textbf{(2)}$$

measurement values. Now, we replace each original defect by **w** imaginary defects each with its individual extension (e. g. $\Delta\varphi$=5° results in **w**=36 imaginary defects). Each imaginary defect has to be weighted with **1/w** because all **w** imaginary defects represent just one original defect. So, the absolute occurrence of detected defects remains unchanged, if and only if for each defect

$$\sum_{i=1}^{s} \frac{1}{w} D_i = 1 \qquad \textbf{(3)}$$

where **s** is the total number of size intervals and **Di** stands for the number of imaginary defects per size interval. For example, the defect "i1510604.tif" of Figure 5 results in a *Micro Size Distribution* as can be seen in the following Figure.

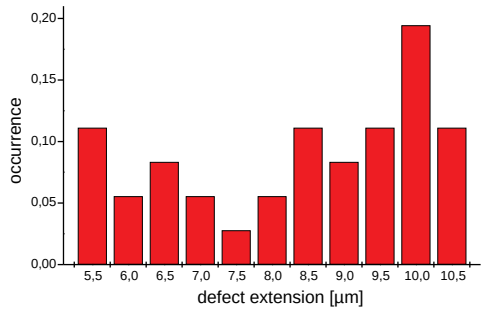

Fig. 10: *Micro Size Distribution* of imaginary defects based on one original defect.

Then, we determine a general size distribution based on all *Micro Size Distributions* of the imaginary defects, where the total number of all original defects is identical to the sum of all imaginary defects.

Using the fault probability kernels introduced by Stapper [Stap84] and Ferris Prabhu [Ferr85b], it is possible to calculate the probability that a defect causes a fault between parallel lines. So, defect densities and defect size distributions will be comparable and independent of the dimensions of the test structures used to detect the defects. For this reason, each imaginary defect gets its individual fault probability. The following Figure 11 shows two general size distributions extracted from two test structure designs adjacently placed on some wafers, but containing comb lines with different line pitch. Nevertheless both structures yield similar size distributions so that we select them as reference size distributions to compare some yield models to describe defect outlines.

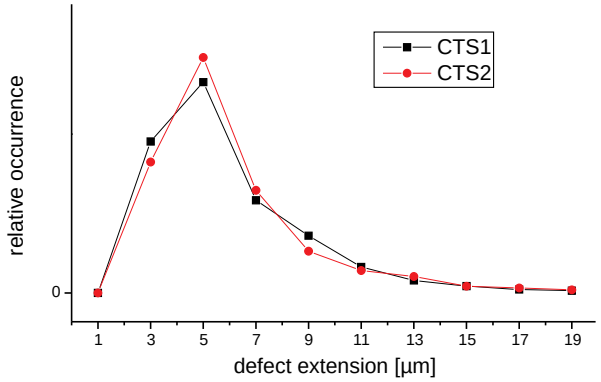

Fig. 11: Defect size distributions collected from different test structure designs.

5 Influence on Yield Modeling

Today's methodologies to include defect sizes for yield prediction base on defects whose outline is modeled as a circular disk [StRo95]. So, we will compare the reference distribution introduced above to size distributions measured and calculated based on known models to describe the outline of defects.

5.1 Outline Models

Modeling defect outline should provide the correct diameter of a circular defect model, so that its probability to cause a fault (= fault probability) fits to the probability that the real defect causes a fault. The following models will be used in semiconductor yield prediction.

5.1.1 Circle Based on Maximum or Minimum Defect Extension

Generally, the diameter of the circle to describe a defect will be calculated based on the maximal defect extension. Also, the minimal defect extension will be used to get the diameter of the circle.

5.1.2 Circle Based on Mean Defect Extension

Here, the defect will be modeled in a circle, where both should have the same area. So the mean value of individually measured defect extension **di** will be calculated as

$$\bar{d} := \frac{1}{v} \cdot \sum_{i-1}^{v} d_i \qquad \textbf{(4)}$$

where **v** is the number of measured values.

5.1.3 Circle Based on Elliptical Defect Extension

To measure all extension values of a defect is costly, so that [HeSt94] introduced the elliptical model to describe real defect outlines. Therefore, the approximation

$$\bar{d} \approx \tfrac{1}{2} \cdot \sqrt{\min \cdot \max} + \frac{\min \cdot \max}{\min + \max} \qquad \textbf{(5)}$$

calculates the mean extension of an ellipse, just based on the maximum extension **max** and the minimum extension **min** of the real defect. For $\frac{max}{min} \leq 4$ the approximation error is less than 1%. So for almost all cases (ref. Figure 9) the value of $\bar{d}$ is estimated very precisely.

5.2 Comparison of Outline Models

First, the following Figure 12 gives the extension of one defect dependent on the measurement angle. Also, the values of the four differently modeled circles can be seen. In most cases, the circle based on the ellipse is smaller than the mean circle. Nevertheless, none of these models represent the outline of type-1 and type-2 defects.

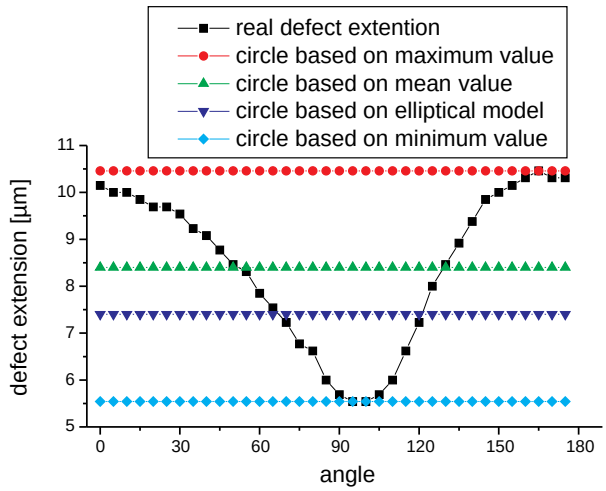

Fig. 12: Outline of circles calculated from an original defect.

We choose data samples collected from different test structures to point out the influence of these models on determining defect size distributions. The following Figure 13 gives the size distributions based on all four models and also includes the reference size distribution of the real defect outlines.

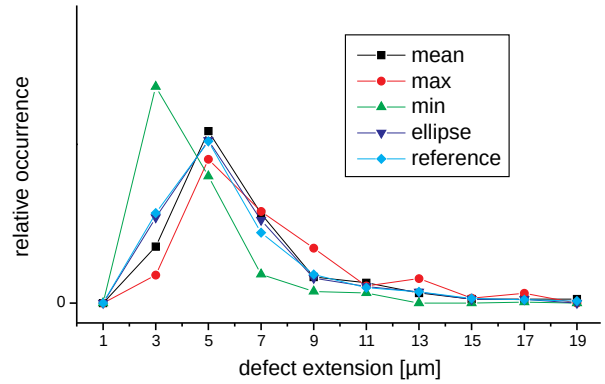

Fig. 13: Defect size distributions collected from data of test structure A that base on different modeling procedures.

Figure 14 gives the relative errors of the models, compared to the reference size distribution. The mean circle model and the elliptical model have the smallest error. Especially the sum of all errors per size is very small for these two models. Defect size distributions based on maximum or minimum circles should not be used for accurate yield prediction.

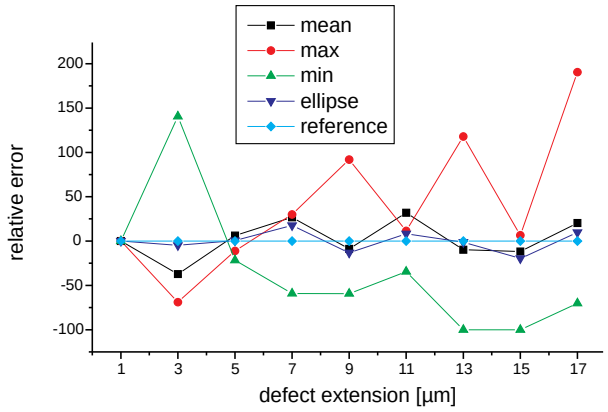

Fig. 14: Relative percentage error of defect outline models based on data of test structure A.

The following two figures 15 and 16 present the results based on another test structure which yield similar results.

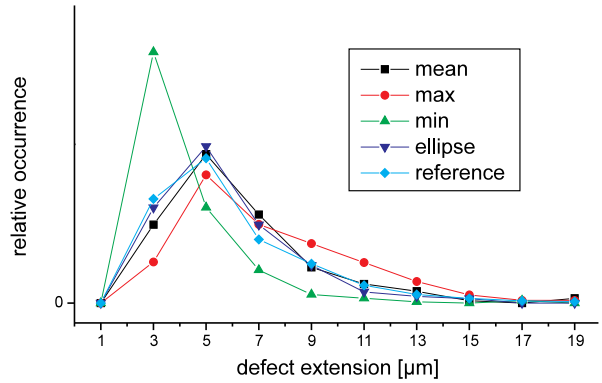

Fig. 15: Defect size distributions collected from data of test structure B that base on different modeling procedures.

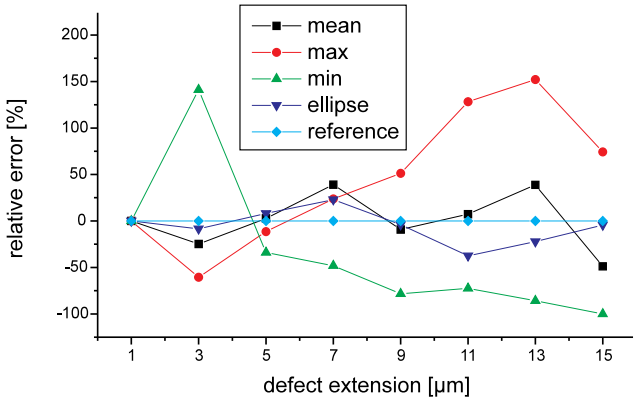

Fig. 16: Relative percentage error of defect outline models based on data of test structure B.

6 Conclusion

Generally, errors in yield prediction were assigned to wrong critical area calculations and faulty selections of the models to describe defect densities. Yield prediction models and critical area calculations base on defects modeled as circles. But, the measurement of the extension of real defect outlines yields a classification of defects, where just about a quarter of all defects may be modeled as circles (type-0 defects). The major occurrence of type-1 and type-2 defects having irregular outlines are the reason, why defect size distributions based on circular defect models are insufficient, which may also be one reason for trouble in yield prediction.

So far, a general defect size distribution bases on just one extension value per detected defect. Our approach in determining a more realistic defect size distribution bases on the inclusion of *Micro Size Distributions* that reflect the outline of each detected defect. To enable an efficient collection of necessary data on defect outlines, we presented the checkerboard test structure design to precisely localize defects inside large chip areas.

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