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Strategy to Optimize the Development, Use, and Dimension of Test Structures to Control Defect Appearance in Backend Process Steps

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Abstract **— To inspect and classify defects occurring during backend process steps, this paper describes a comprehensive methodology how to develop, use, and dimension test structures and how to optimize their organization inside given test chip boundaries. Starting point is the description of process steps and known types of defects. According to existing design rules different test structures will be designed and arranged as (in-line) process monitors inside a checkerboard framework using standard boundary pads.**

1 INTRODUCTION

TODAY'S complexity of integrated circuits requires more and more backend layers to connect all circuit cells and devices (at the moment 5 metal layers in ASICs). For that typical backend defects like intermetal shorts and virtual vias as well as the 3D-influence of underlying layers gain more importance in defect statistics. So especially designed test chips to control the backend process steps for polysilicon and metal layers are in demand. In order to obtain test chips with test structures optimized to control defect appearance in backend process steps, the following methodical procedure is suggested.

After pointing out the relationship between general types of defects and their causes from specific process steps, possible test structures will be selected according to their defect detecting characteristics (section 2). Then these test structures have to be arranged inside a given test chip area (section 3). Section 4 deals with the dimension of the test structure layout objects. Also, the distribution of different sized structures inside a test chip will be discussed. Section 5 describes methods to analyze the measured data and to extract defect parameters. Section 6 gives some experimental results. Finally section 7 concludes the paper.

2 SELECTION OF TEST STRUCTURES

Dependant on the application of process relevant data, different types of test structures are used (ref. table 1). The goal of the selection process is to use structures that provide a versatile defect parameter extraction for many applications.

TEST STRUCTURES	Optical test structures (marks to adjust masks, optical etch windows, ...) [GoTH93]						
	Basic geometrical layout objects (serpentine & comb lines, contact & via strings) [IpSa77], [Bueh83], [LYWM86], [Walk87]						
	Electrical sheet resistance, line width, and contact resistance & size structures (cross and bridge resistor, split cross bridge, ...) [BuTh78], [BuHe86], [FrLu88], [LiSa92]						
	DRAM, SRAM, transistor-arrays [BuLi81], [GeWR92], [KMGS94]						
	Small specific (test) circuits (oscillators, standard cells, ...) [Bueh83], [Bren92]						
	Discrete semiconductor devices (transistors, diodes, resistors, capacitances) [Bueh83]						
APPLICATIONS	Design rule development & checking						
	Process development						
	(In-line) process control	?					
	Defect monitoring (random and systematic)						
	Yield monitoring and prediction						
	Transistor measurement & circuit parameter extraction						

Tab. 1: Application of different test structures

Undesigned layout objects (=*defects*) can occur during the manufacturing process. A *defect mechanism* describes how a defect is produced by a specific sequence of process steps. Dependant on the layout, defects can become the cause of electrically measurable *faults* which are responsible for manufacturing related malfunctions of chips. A *fault mechanism* describes how a fault results from a defect according to the specific chip layout.

Figure 1 gives an example of the relationship between defects, their possible process specific causes, and the layout specific resulting faults for the typical material configuration in backend processes (*LOWER CONDUCTING LAYER - ISOLATING LAYER - UPPER CONDUCTING LAYER*). This figure

shows that the defects occurring in backend process steps can be generally divided in only two basic types of defects: Extra material defects (EMDs) and missing material defects (MMDs).

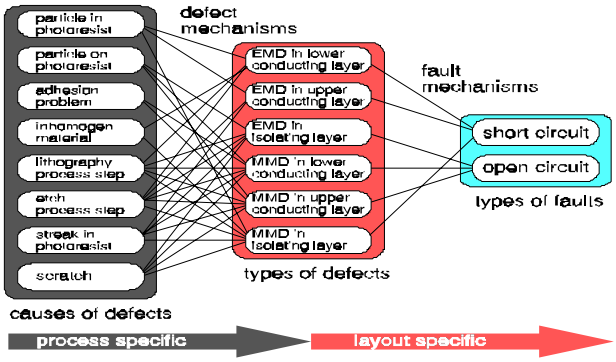


Fig. 1: Defect mechanisms and fault mechanisms

Due to the small number of basic types of defects it should be possible to use only a few basic test structures to investigate the appearance of defects. To decide whether test structures are suitable to control backend process steps or not, their characteristics summarized in table 2 have to be compared with the following demands:

- Systematic problems have to be pointed out as well as random defects should be detectable even if the probability of occurrence is low.
- Test structures exclusively manufactured in backend process steps cannot use any active areas (except ASICs based on gate arrays).

TEST STR.	Optical test structures							
	Basic geometrical layout objects							
	Electrical sheet resistance, line width, and contact resistance & size structures							
	DRAM, SRAM, transistor-arrays							
	Small specific (test) circuits							
	Discrete semicond. devices							
CHARACTERISTICS	Test chip organization & placement on wafer	2 by N pad array	2 by N pad array	bound-ary pads	2 by N pad array	2 by N pad array	bound-ary pads	scribe line
	Aims at systematic effects	yes	yes	no	yes	yes	yes	yes
	Aims at random effects	no	no	yes	no	no	yes	no
	Electrical measurement	yes	yes	yes	yes	yes	yes	no
	Optical measurement	yes	?	yes	yes	?	no	yes
	Localization of problems	yes	?	yes	yes	?	no	yes
	Uses active areas for semiconductor devices	yes	yes	yes	no	no	no	no

Tab. 2: Characteristics of different types of test structures

Table 2 shows that only basic geometrical layout objects fulfill all demands if they are distributed throughout the complete chip area to provide a large defect sensitive area. Normally straight lines and comb lines are used to detect defects that result in electrically measurable short circuits, while via strings, contact strings and lines formed as serpentines aim at defects, that results in electrically measurable open circuits [IpSa77], [Bueh83], [LYWM86].

3 Organization of Test Chips

Different test structures have to be arranged inside a given chip area. Methods to organize test chips are preferred combining the following three partly contrasting conditions:

- Test chips should provide a *large defect sensitive area* to detect defects even if the average defect density is low.
- A *layer sensitive defect separation* is required to assign electrically detected defects to a specific layer
- A *precise defect localization* enables an analysis of defect cluster effects inside the test chip area. The localization also simplifies the optical determination of defect parameters like size and outline as well as the mechanisms how a defect results from specific process steps.

Two major methods to organize test chips are known, the "2 by N" probe-pad array [Bueh79] and standard boundary pads. The defect sensitive area inside a "2 by N" array is relatively small so that the large sensitive area inside the boundary pads seems to be more suitable (ref. table 2). But here the number of pads is relatively small so that methods are required to separate defects. After the principal description of those separation methods, two test chip arrangements will be presented especially designed for an efficient application in backend process steps.

3.1 Methods to Separate Defects

The following neighborhood graph is introduced, to describe the principle to separate and localize different defects that result in *short circuits* without using any active semiconductor devices.

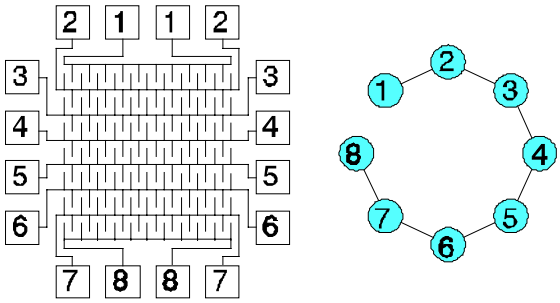


Fig. 2: Neighborhood graph of a test chip [HeWe94], [HeSt94]

One node stands for all designed conductive layout objects that are connected to each other inside a test chip and so called a **maximal conductive component (MCC)**. An undesigned short circuit defect is only detectable between two different MCCs; therefore called **MCC-pair**. Thus an edge between two nodes (MCCs) of the neighborhood graph indicates that the layout objects of this MCC-pair are adjacent to each other in one region of the test chip with only nonconducting material between them.

The number of different MCCs is limited to the number of pads. To increase the number of MCC-pairs or separable short circuits, respectively, all MCCs have to be arranged inside a test chip in a way that each MCC is once adjacent to every other MCC. For n different MCCs the permutation procedures introduced by [HeWe92], [Hess93], and [HeSt94] organizes all ½·n·(n-1) MCC-pairs in the rows of matrices so that each MCC-pair exists once or twice. The following figure shows the basic 2D-matrix for n=8 MCCs.

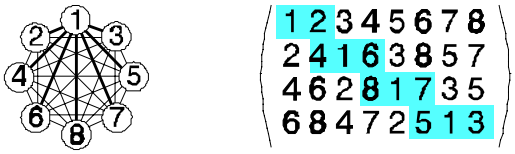


Fig. 3: Neighborhood graph and the matrix with the MCC-pairs

The distribution of the n elements $x_{i,j}$ inside the 2D-matrix will be done, using the following equations:

$$x(i,j) := \begin{cases} j+2\cdot i-2 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i \le \frac{n-j+2}{2} \quad \textbf{(1a)} \\ 2\cdot n-j-2\cdot i-3 & \text{where } \frac{j}{2}\in\mathbb{N} \wedge i > \frac{n-j+2}{2} \quad \textbf{(1b)} \\ 2\cdot i-j-1 & \text{where } \frac{j+1}{2}\in\mathbb{N} \wedge i > \frac{j+1}{2} \quad \textbf{(1c)} \\ j-2\cdot i \;\; 2 & \text{where } \frac{j\,1\,1}{2}\in\mathbb{N} \wedge i \le \frac{j\,1\,1}{2} \quad \textbf{(1d)} \end{cases}$$

i,j : row index, column index of the 2D-matrix

In contrast to the short circuit defects, there is no possibility to increase the number of distinguishable defects that results in *open circuits* without either increasing the number of pads or using primitive semiconductor devices (refer geometry digraph in [HeWe94a]). If diodes are available in addition to the backend polysilicon and metal layers, a diode array increases the number of distinguishable connections for a given number of pads. In this case each diode stands for a distinguishable serpentine line or a via (or contact) string, respectively.

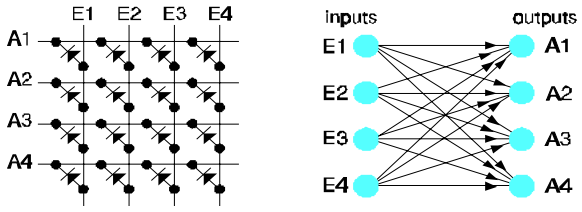


Fig. 4: Diode array for n pads with $(n/2)^2$ diodes (left)
Geometry digraph where nodes represent pads and edges stand for serpentines [HeWe94a]

3.2 Checkerboard Test Chips

A given set of MCCs will be divided in disjunct subsets (ref. figure 5). Each subset includes the MCCs of one layer so that the number of subsets is equal to the number of layers. So each MCC will be implemented in a specific layer. After this all MCCs will be replaced by major lines as it can be seen on the right side of figure 5.

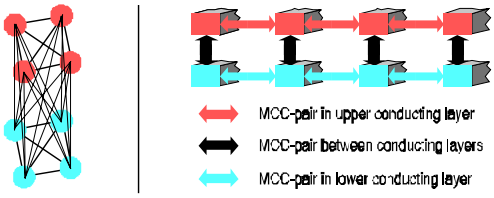


Fig. 5: Arrangement of MCC-pairs in a test chip

The major lines will be arranged inside given boundary pads generating rectangular subchips, where the really defect sensitive test structures will be placed consisting of basic layout objects like comb lines. The checkered arrangement of subchips is responsible for the naming of the **Checkerboard Test Chip (CTC)**. The routing channels to enable the permutation of the MCCs between the checkerboard lines are described in detail in [Hess93] and [HeSt94].

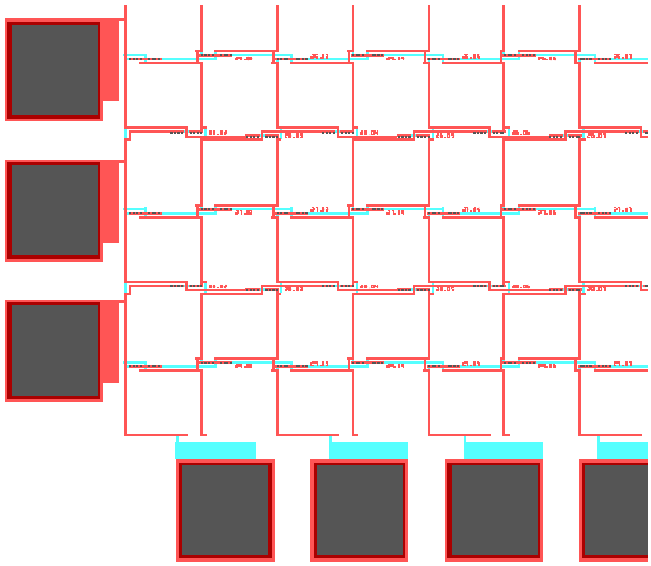


Fig. 6: Detail view of the checkerboard framework

In addition to that, [HeWe94a] describes a **Diode Checkerboard Test Chip (DCTC)** to detect open circuit defects as well as short circuit defects. In this case, all available pads are numbered from 1 to n and splited into different subsets, the inputs E_j and outputs A_i. The procedure to localize open circuit defects will be applied to the elements of the subsets A and E. The assignment to the layers and the procedure to localize short circuit defects and will be applied to the elements of the subset E. Both principles will be mixed in a way shown in figure 7. Starting point is the diode-array of figure 4. Every second line of diodes will be mirrored and moved which results in the construction in the middle of figure 7. Then the E_j MCCs have to be permutated corresponding to the permutation procedure (ref. figure 7 right).

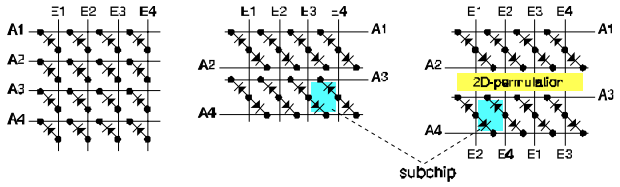


Fig. 7: Procedure to design a diode checkerboard test chip

Finally the subchips will be arranged inside boundary pads which also results in a checkerboard test chip design seen in the following figure. Serpentine lines, via strings, and contact strings can be implemented inside these subchips.

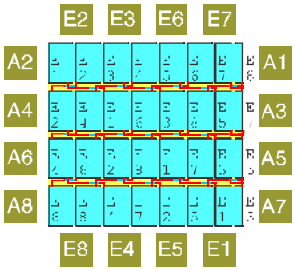


Fig. 8: Detail view of the framework of a diode checkerboard test chip (DCTC)

3.3 Harp Test Chips

If a defect size distribution is sufficient at a rough estimation, another test chip arrangement will be proposed. Here all MCCs will be replaced by lines also according to the rows of the 2D-matrix. But now, all rows will be placed in one continuous string, where an additional MCC marks the border of the matrix rows (black line in figure 9). Thus, the size of an occurring short circuit defect will be estimated dependant on the number of connected MCC-lines.

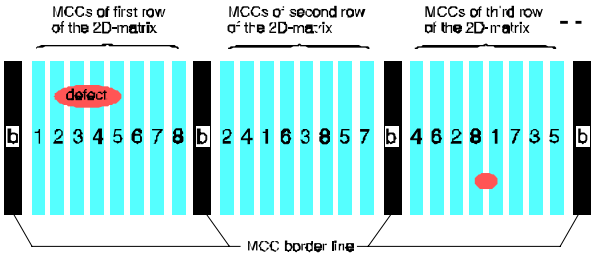


Fig. 9: Arrangement of parallel distinguishable MCC-lines

All parallel lines will also be arranged inside boundary pads, where the length of the lines corresponds to the chip size. The routing channels to permute the MCC-lines will be placed above or beyond the lines (ref. left side of figure 10). Thus the arrangement of lines looks similar to the strings of a harp therefore called **Harp Test Chip (HTC)**. The detection of open circuit defects as well as short circuit defects again requires diodes to separate implemented serpentine lines, via strings or contact strings, respectively. The right side of figure 10 shows the principle to design a **Diode Harp Test Chip (DHTC)**.

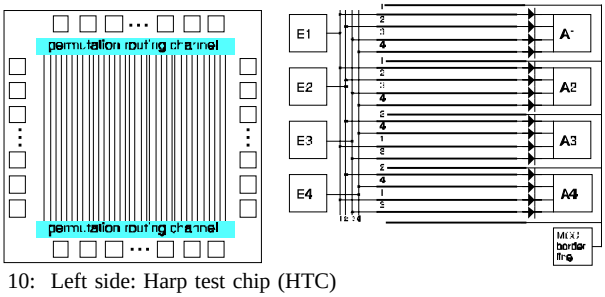


Fig. 10: Left side: Harp test chip (HTC)
Right side: Diode harp test chip (DHTC)

3.4 Selection of CTC, DCTC, HTC, or DHTC

The following table shows different parameters of defects which are interesting within the bounds of backend process steps and the test chip organization that facilitates an efficient data recording.

parameter of defects	electrically measurable		optically measurable
	shorts	opens	
type (EMD, MMD)	CTC / DCTC HTC / DHTC	DCTC / DHTC	
layer	CTC / DCTC HTC / DHTC	DCTC / DHTC	
position inside chip area (localization)	CTC / DCTC	DCTC	
size	rough estimation using HTC	DCTC / DHTC with different dimension	CTC / DCTC
outline (circular, elliptical, rectangular)			CTC / DCTC
3D-influence of underlying topography	CTC / DCTC	DCTC	
systematic problems or random defects?	CTC / DCTC (HTC / DHTC) analysis of frequency	DCTC (DHTC) analysis of frequency	CTC / DCTC
process specific causes			CTC / DCTC
process specific defect mechanisms (*Answer to the question*: Which process step is responsible for the observed defect?)			CTC / DCTC
layout specific fault mechanisms (*Answer to the question*: Is it necessary to modify existing design rules?)	CTC / DCTC (HTC / DHTC)	DCTC (DHTC)	CTC / DCTC

Tab. 3: Extraction of defect parameters using specific test chips

4 Dimension of Test Structures

After giving some indications how to dimension test structure layout objects, different sized structures have to be distributed among the subchips of the CTC/DCTC or the lines of the HTC/DHTC, respectively.

4.1 Dimension of Layout Objects

The sequence of manufacturing process steps and different types of defect mechanisms are responsible for two major principles to dimension basic layout objects as test structures. For example missing adhesion of lines is dependent on the line width, so that only different sized lines can investigate this problem. On the other hand, one size of comb lines is sufficient to investigate different sized particle defects resulting in electrically measurable short circuits.

Normally different sized - 5 up to 10 dimensions - structures are used to detect defects that results in open circuits. So each size covers only a relatively small area inside a test chip which might be decrease the statistical significance of measured data. But systematic problems only have an influence on parts of the designed structures and already the electrical measurement yields a size distribution of defects.

In contrast to that, only a few - 1 up to 3 - dimensions of structures are used to detect defects that results in electrically measurable short circuits. So the sensitive area is equally distributed inside the test chip to increase the statistical significance. But the occurrence of systematic problems can disturb the data recording and the electrical measurement cannot give any information about the defect size except a HTC or DHTC is used.

As a result of this, the dimensions of the test structure layout objects have to be determined very carefully. It is always to find a golden mean between an accurate resolution to detect very small defects and the exclusion of massive systematic problems. The following figure shows on the left side the probability that a defect causes an electrically measurable fault corresponding to its extension (ref. [Ferr85]). Dependant on existing regular design rules it would be necessary to decrease these rules as illustrated on the right side of the figure to really detect all defects that might be responsible for a fault. To prevent systematic problems, even test structures should not use dimensions so far below existing design rules. So it is more effective to design test structure layout objects near to existing design rules and fit measured data according to the fault probability distribution.

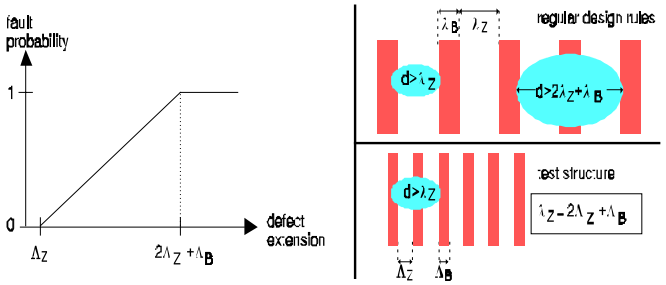


Fig. 11: Regular design rules compared to test structure dimensions

In order to obtain the step size λ_i, to implement layout objects using several dimensions, a start value α and a stop value β have to be determined. According to the number k of steps each step interval will be determined using the following equation, which follows the generally nonlinear size distributions.

$$\lambda_i = \alpha \cdot \sqrt[k-1]{\frac{\beta}{\alpha}}^{\,i} \qquad \text{if} \quad i \in \mathbb{N} \quad \wedge \quad 0 \le i < k \qquad \textbf{(2)}$$

So different sized comb lines, serpentine lines, via strings, and contact strings will be placed inside the checkerboard framework as can be seen in the following figure. In order to obtain the localization of intermediate shorts the designer should avoid crosswise overlapping of comb lines.

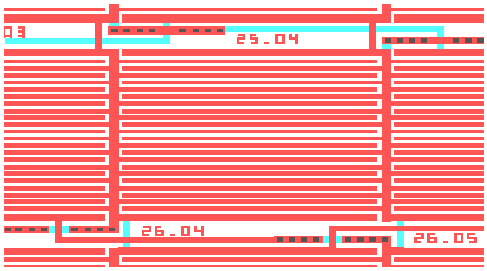


Fig. 12: Comb lines inside a subchip of a CTC

4.2 Distribution in CTC, DCTC, HTC, and DHTC

In order to avoid that systematic process problems affect the complete test chip, different sized test structure layout objects have to be especially distributed among the subchips. A given subset of MCCs per layer (ref. subsection 3.2) has to be divided in subsets again. The number k of distinguishable dimensions is dependent on the number m of (sub-)subsets.

$$k = \frac{1}{2} \cdot m \cdot (m + 1) \qquad \textbf{(3)}$$

Each MCC-pair will be assigned to a dimension according to its accompanying sub-subset. Smaller dimensions should be assigned to MCC-pairs of equal sub-subsets. The following table shows an example where 3 dimensions are distributed among 4 layers, each containing 12 MCCs in 66 subchips.

66 subchips in layer	dimension A (in 15 subchips)		dimension B (in 15 subchips)		dimension C (in 36 subchips)	
	1st MCC ∈	2nd MCC ∈	1st MCC ∈	2nd MCC ∈	1st MCC ∈	2nd MCC ∈
metal 3	{37-42}	{37-42}	{43-48}	{43-48}	{37-42}	{43-48}
metal 2	{25-30}	{25-30}	{31-36}	{31-36}	{25-30}	{31-36}
metal 1	{13-18}	{13-18}	{19-24}	{19-24}	{13-18}	{19-24}
polysilicon	{1-6}	{1-6}	{7-12}	{7-12}	{1-6}	{7-12}

Tab. 4: Disjunct distribution of 48 MCCs (or pads respectively) among 4 conducting layers dependent on 3 different dimensions of comb lines

In case of DCTC and DHTC this procedure will be applied to the E elements. So systematic problems only affect a small number of MCCs and therefore also a small number of subchips while the major rest of subchips enable a data recording of random defects.

5 Defect Parameter Extraction

To measure the resistance of the test structures, a digital tester will be used, because the electrical test must only decide whether there is a defect or not. The measured values are assigned to possible defects according to the following table.

measured voltage	binary value	short circuit detected	open circuit detected
$V_{measured} \ge V_{threshold}$	1	yes	no
$V_{measured} < V_{threshold}$	0	no	yes

Tab. 5: Data conversion

To detect the defects inside the test chips a "walking-one" over all pads is sufficient while all other channels are measuring the voltage responses. If a defect occurs, two or more MCCs are connected or the implemented connection of two pads is interrupted, respectively. The numbers of a list of k connected MCCs or of a pair (p,q) of separated pads, respectively, are the starting point to the localization procedures. For that it is necessary to extract all possible MCC-pairs from the connected MCC-k-tuple.

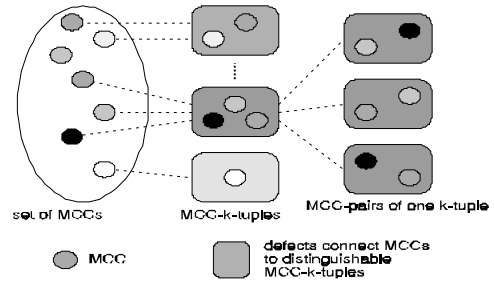


Fig. 13: Principle to localize defects

After that, it is possible to conclude the subchip that contains a defect, because each MCC-pair can be clearly assigned to a specific subchip and its containing test structure layout objects (ref. algorithms in [HeWe94a], [HeSt94]).

6 Experimental results

This section describes some manufactured test chips and also gives some figures that results from a defect parameter extraction. The first figure shows a checkerboard test chips (CTC), where a standard boundary pad frame is completely filled with defect sensitive structures. Some details of implemented test structures inside the subchips of a diode test chip can be seen in figure 15, where different sized structures (serpentine lines and via strings) are visible.

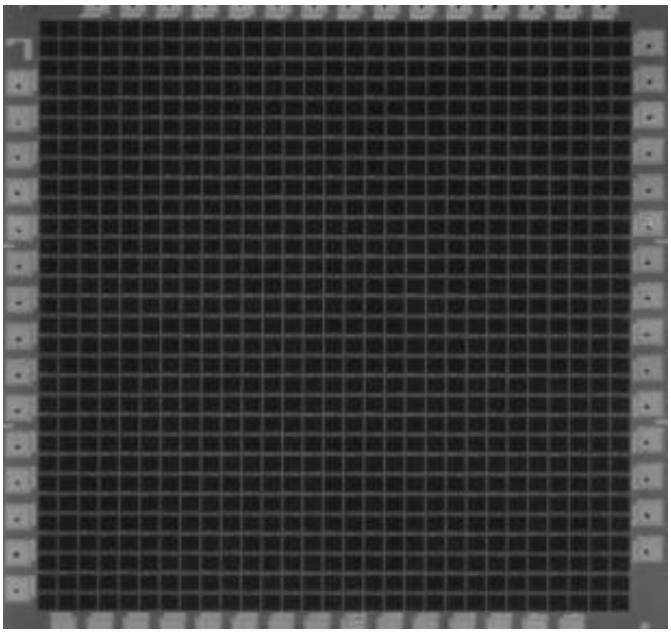


Fig.14: Checkerboard Test Chip (CTC) with two metal layers, n=60 MCCs or pads, respectively, and 870 distinguishable subchips

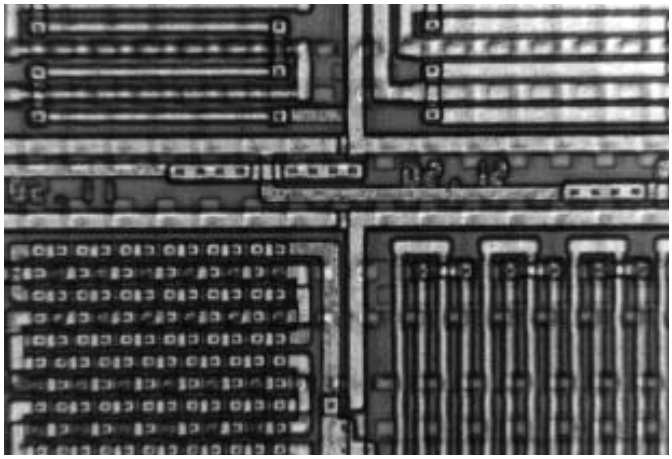


Fig. 15: Details of the subchips inside a diode checkerboard test chip where serpentines and via strings with different dimensions are visible

Figure 16 shows a defect size distribution of more than 200 detected defects. The distribution of the resulting faults among the manufactured layers can be seen in figure 17.

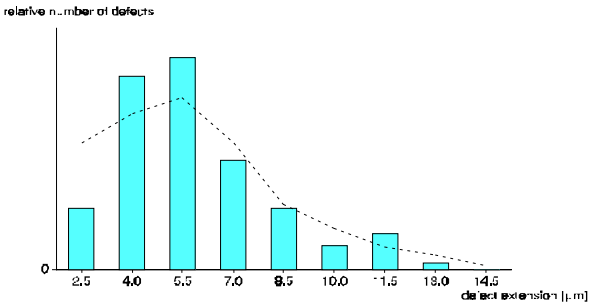


Fig. 16: Defect size distribution using the elliptical model of [HeSt94] to describe the defect outline

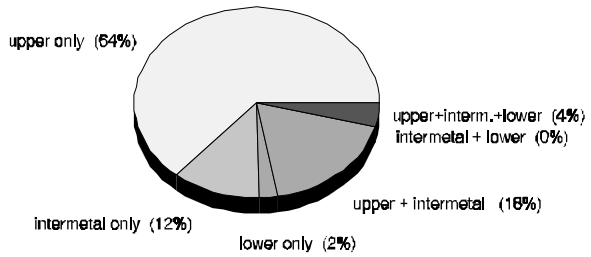
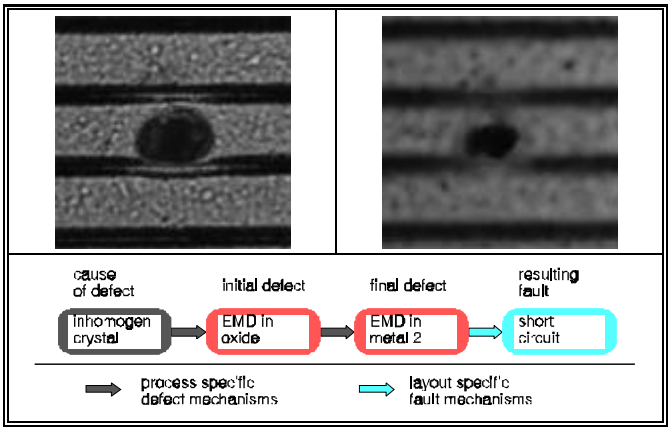
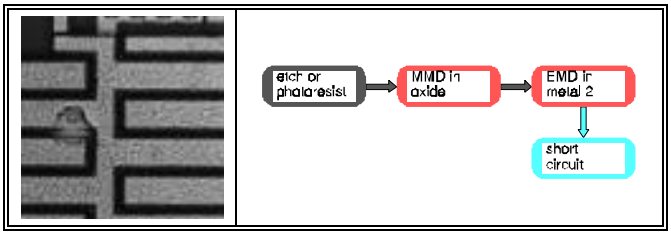


Fig. 17: Distribution of shorts among manufactured metal layers

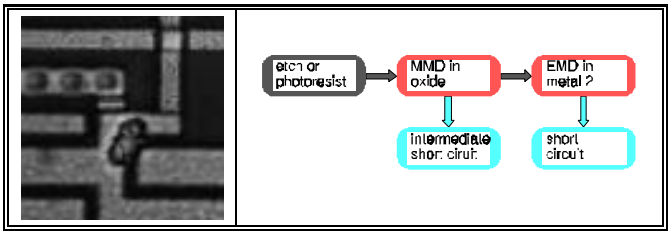
The following tables show some typical defects. For example, table 6 shows an extra oxide defect that is due to a crystal error. The upper right picture shows the same defect with another focus. As a result of this, an extra metal-2 defect is also produced. Only this metal-2 defect results in an electrically detectable metal-2 short circuit. A missing oxide defect, that is caused by a particle in lacquer during the via process step, can be seen in table 7. It leads to an extra metal-2 defect. Again only the extra metal-2 defect causes an electrically detectable metal-2 short circuit. Table 8 also shows a missing oxide defect leading to an extra metal-2 defect. But here the missing oxide defect causes an electrically detectable inter-metal short and the extra metal-2 defect results in a metal-2 short circuit.



Tab. 6: Detected EMDs in a subchip of a checkerboard test chip



Tab. 7: Detected MMD & EMD in a subchip of a CTC



Tab. 8: Detected EMD and MMD in a subchip of a CTC

Finally the following table compare the CTC & DCTC and HTC & DHTC arrangements to known methods to organize test chips.

Characteristics		Organization of test chips		
		2 by N	Boundary pads	(D)CTC & (D)HTC in boundary pads
Ratio: Pad area / chip area		> 60 %	< 15 %	< 15 %
Ratio: test structure area / inside pad area		50 - 90 %	> 80 %	> 90 %
-> relative size of defect sensitive area		20 - 36 %	> 68 %	> 76,5 %
Detect random defects		no (area to small)	yes	yes
Detect systematic problems		yes	yes	yes
Separation and localization of problems or defects, respectively	without active devices	**shorts** & **opens** due to numerous pads	impossible	**shorts** using permutation procedures
	using active devices		**shorts** & **opens** using decoder, multiplexer, transistor	**opens** using diodes

Tab. 9: Characteristics of different types to organize test chips

7 Conclusion

The described method to arrange test structure layout objects inside boundary pads enables an efficient inspection of defects that occur in backend process steps. CTC & DCTC and HTC & DHTC detect systematic problems as well as random defects due to their extensive defect sensitive areas. However, the permutation procedures guarantee a precise separation and localization of defects to facilitate an additional optical determination of size, outline and causes of defects. The systematically designed checkerboard framework enables a machine-assisted generation of test chips according to a specific sequence of process steps, existing design rules, and the extension of expected defects.

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