“Dark Silicon and Dependability”

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… with Muhammad Shafique and Hussam Amrouch

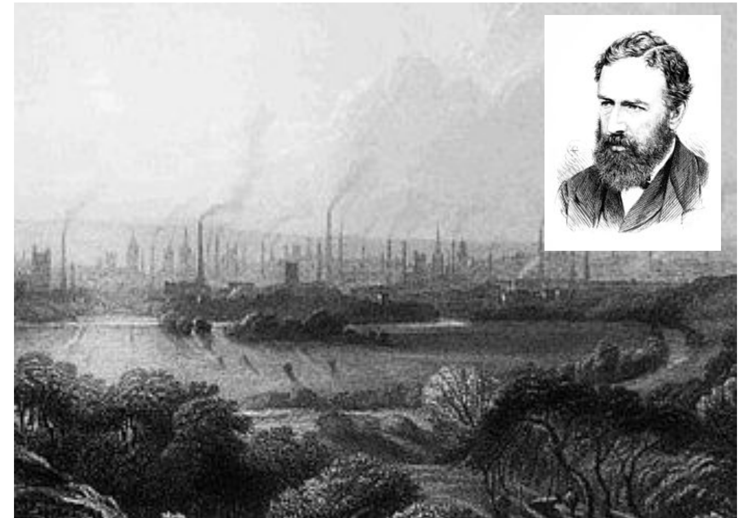
Overview

- What is Dark Silicon
- Interplay of Power Density, Temperature and Dependability
- Mitigating Dark Silicon

What is Dark Silicon?

Lets go back to 1865 …

In economics, the **Jevons paradox** (/ˈdʒɛvənz/; sometimes Jevons effect) occurs when technological progress increases the efficiency with which a resource is used (reducing the amount necessary for any one use), but the rate of consumption of that resource rises because of increasing demand.

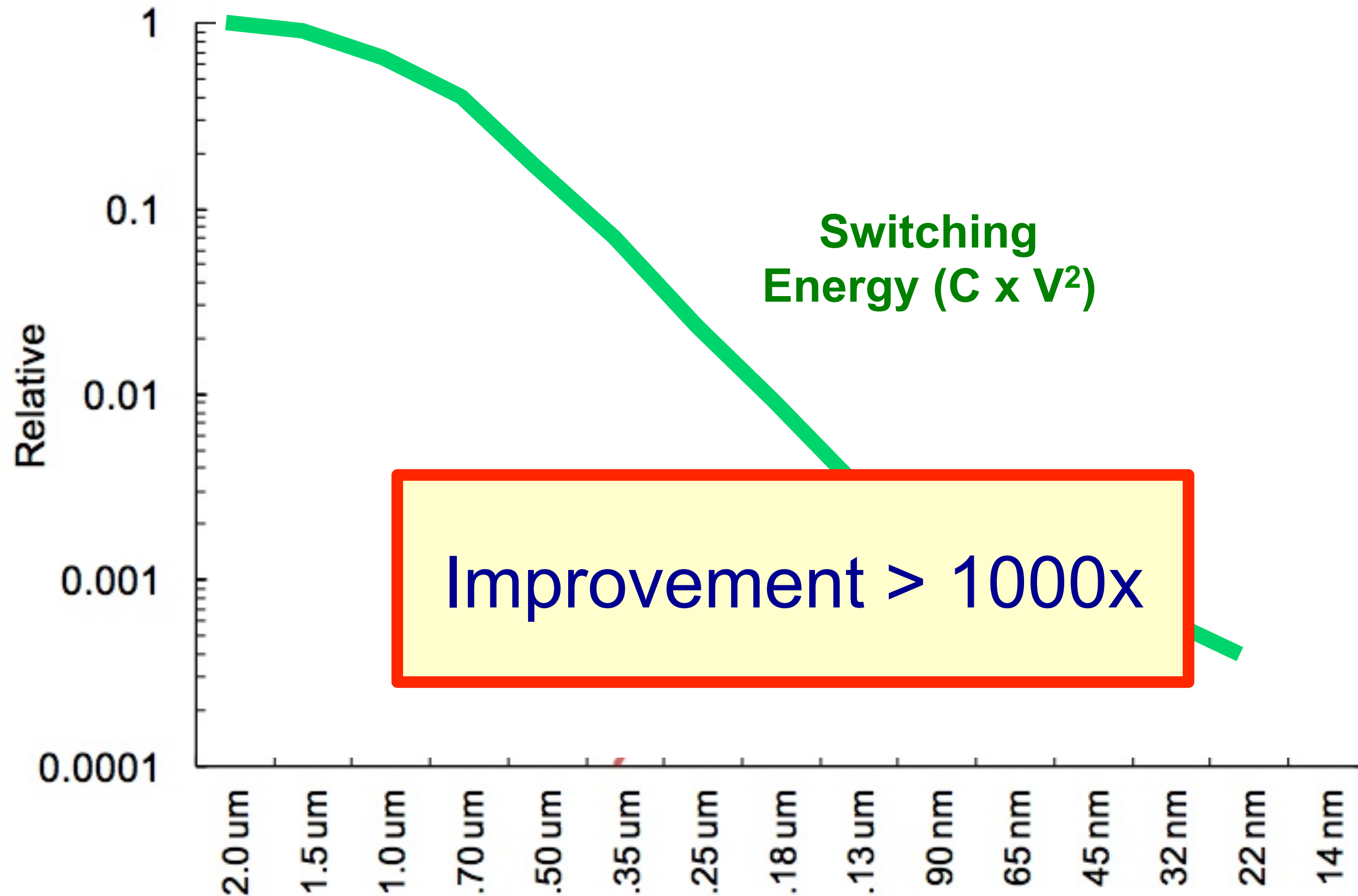


[Src: Wikipedia]

So, how is this related to Dark Silicon ?

[Photo Src: Wikipedia]

Transistor Switching Energy: 1990s - today



[Src: Intel]

Dennard Scaling … (or failure thereof)

Classic

Device count (N)	S^2
Device frequency (f)	S
Device power (cap C)	1/S
Device power (V_{dd})	$1/S^2$
Power Density	**1**

(Src: "Dennard Scaling")

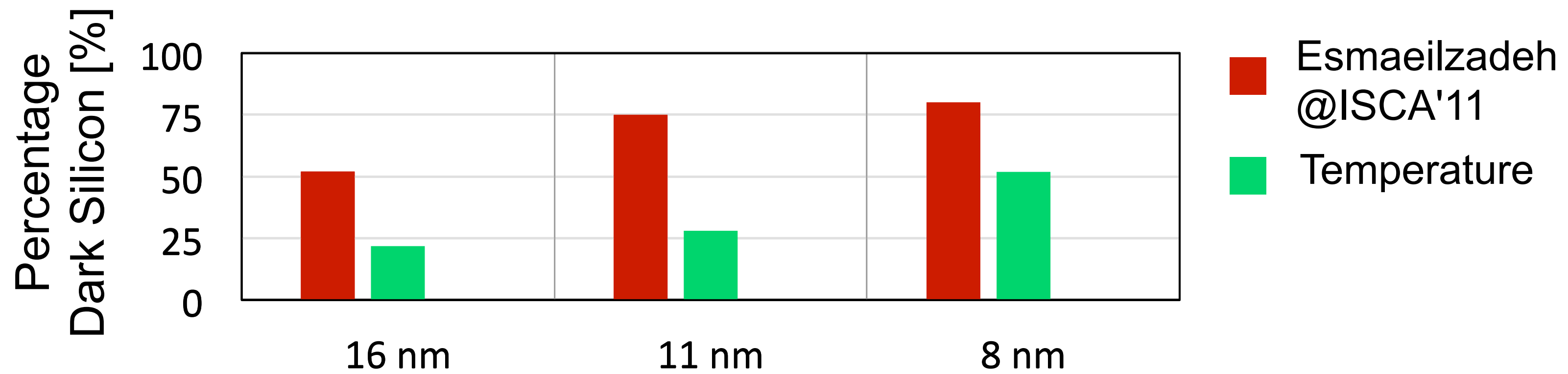
$$P = \frac{1}{2} C V^2 f N$$

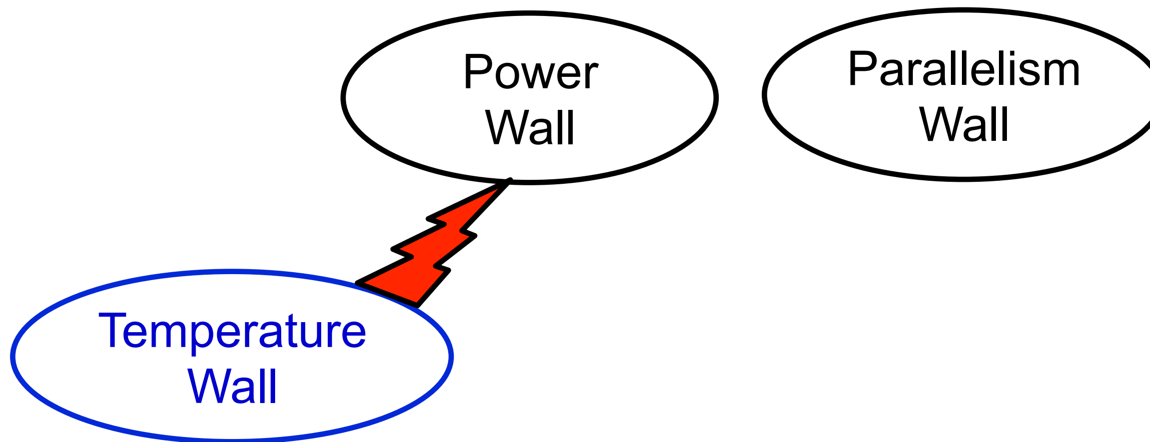
*** Failure of Dennard Scaling leads to Dark Silicon**

*** Dark Silicon is a manifestation of the Jevon paradox**

Dark Silicon: Depends on Point of View …

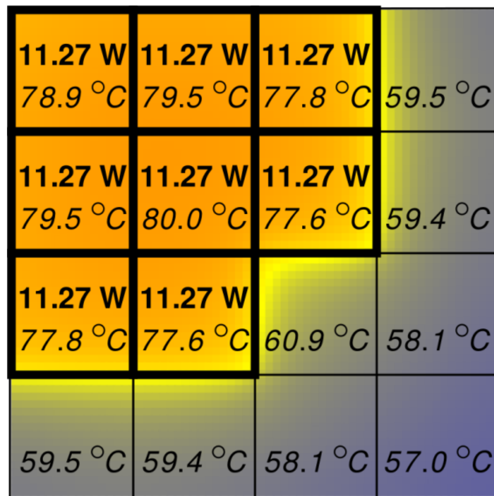
- Dark silicon as a function of power constraint …





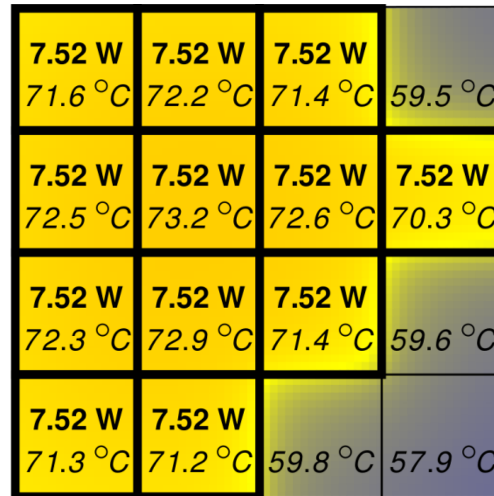
Temperature, Power and TDP

- Example:
  - 16 cores with area 5.3 mm^2
  - Threshold temperature: 80°C
  - Power budget: 90 W



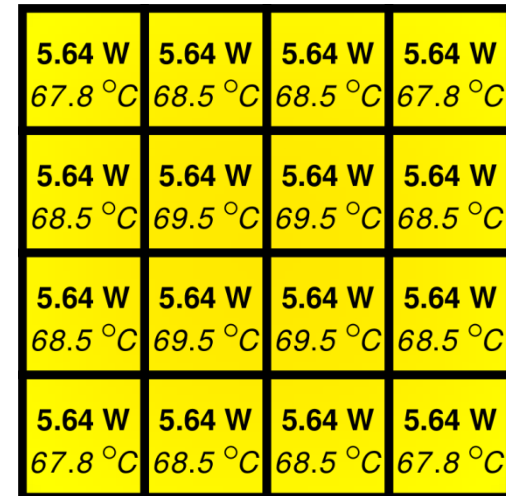
Highest Temperature: 80.0°C

8 active cores



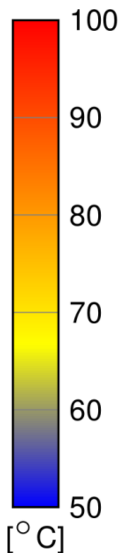
Highest Temperature: 73.2°C

12 active cores



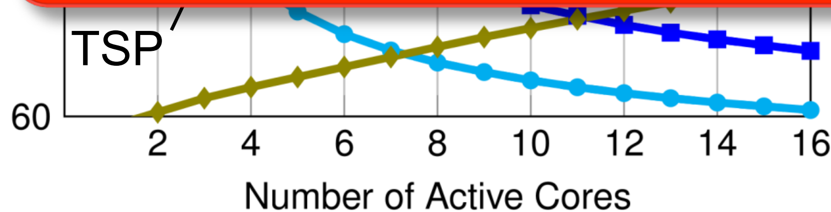
Highest Temperature: 69.5°C

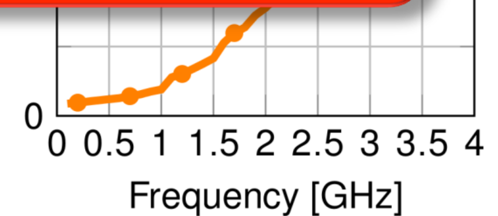
16 active cores



Temperature, Power and TDP

- 16 cores with area 5.3 mm^2
- Threshold temperature: 80°C
- Po
- Co





Example Conclusions:

Single and constant power budgets (e.g., TDP)

- **Thermal unsafe**
- **Pessimistic**

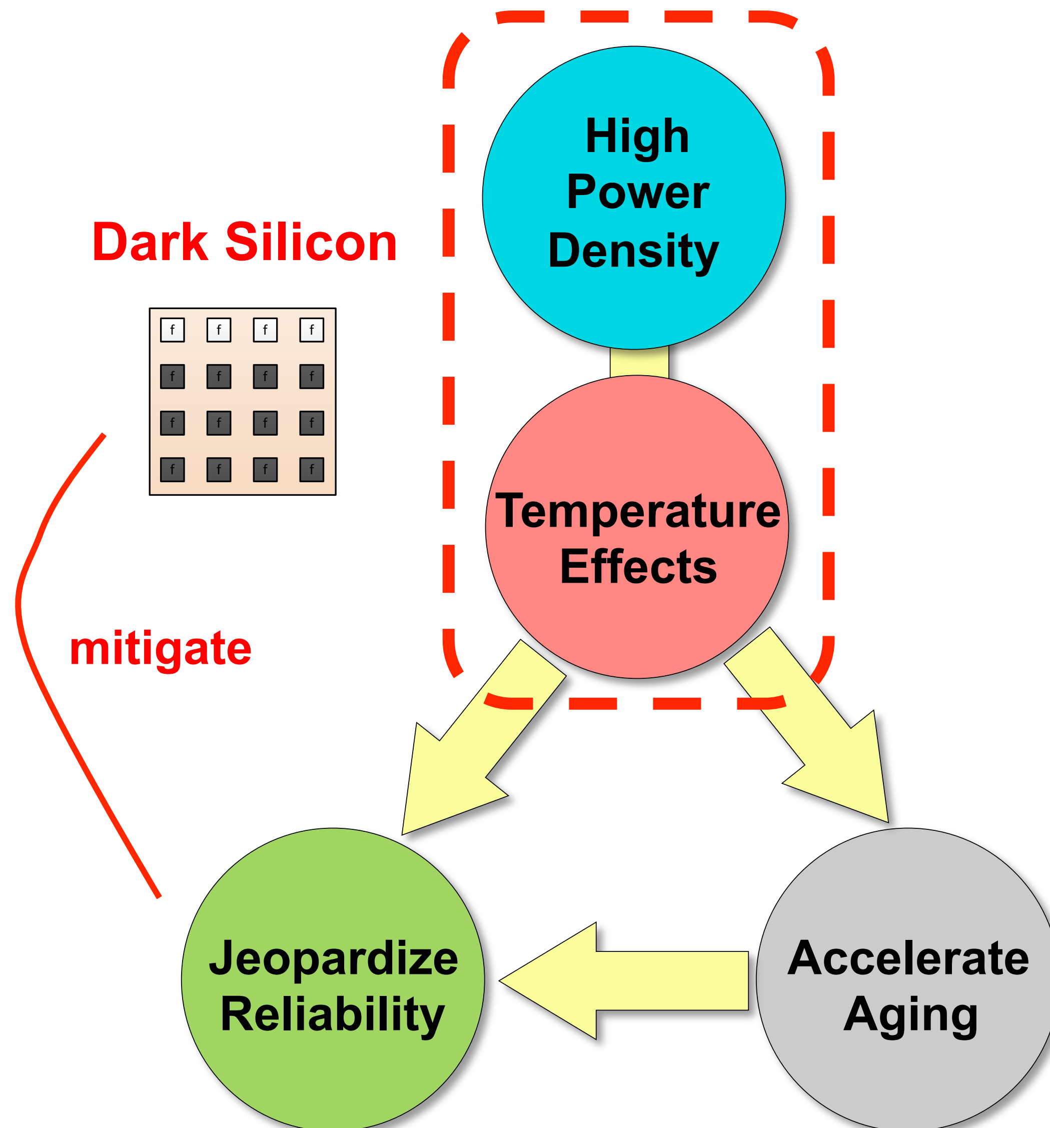
Thermal Safe Power (TSP)

- Power budget depends on the number of active cores
- ...ions

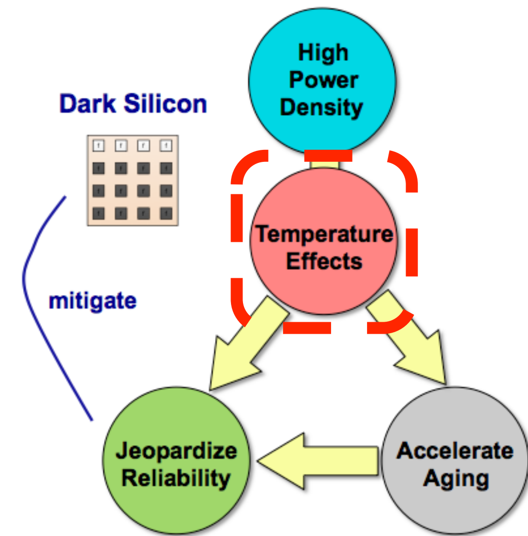
TS...

S. Pagani, H. Khdr, W. Munawar, J.-J. Chen, M. Shafique, M. Li, J. Henkel, "*TSP: Thermal Safe Power - Efficient power budgeting for Many-Core Systems in Dark Silicon*", (**CODES+ISSS**), 2014.

Outline



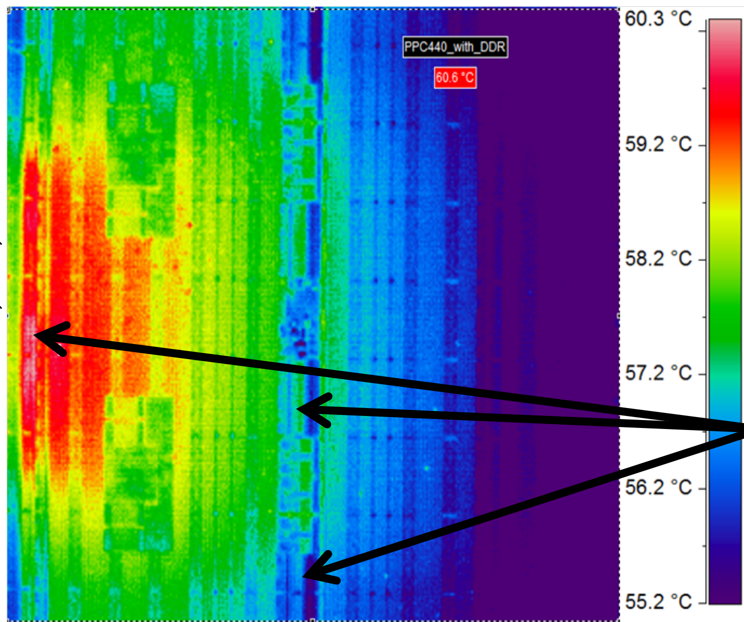
Temperature Effects



Thermal Gradients

- Due to: a) Low-frequency power change, b) Workload change, c) Power management
- Affects MTTF

Scr: Amrouch, Ebi, Henkel

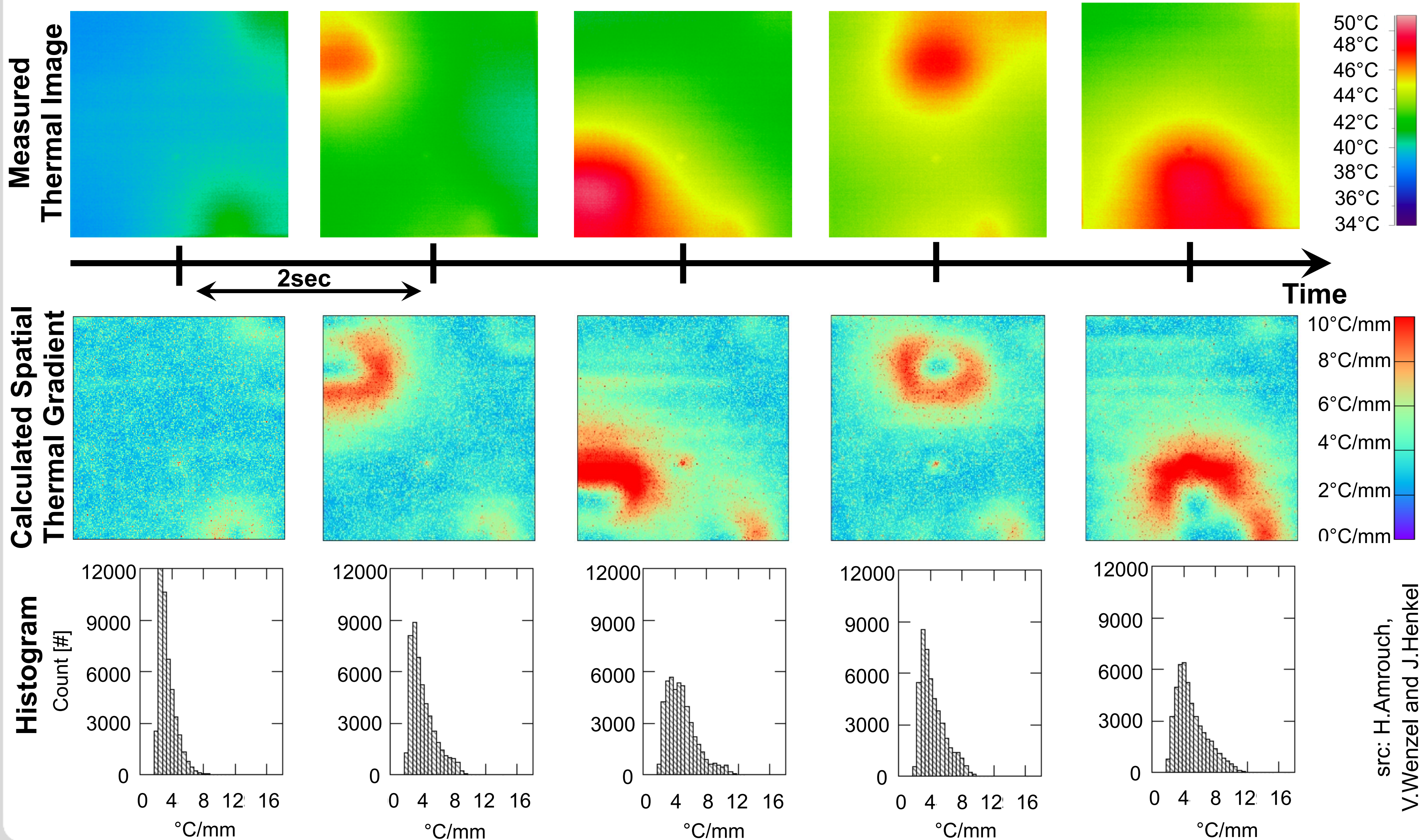


Virtex-5 with two PowerPC CPUs

Temperature analysis of Virtex-5 FPGA using infrared thermal camera showing peak spatial thermal gradients of 0.12°C/µm resulting in an increase of electromigration and accelerated aging

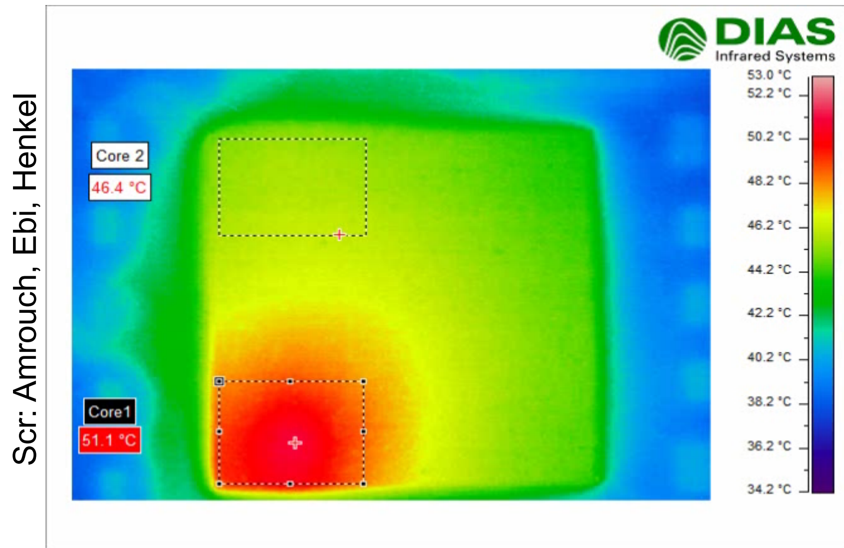
Spatial gradients

Spatial Thermal Gradient Analysis

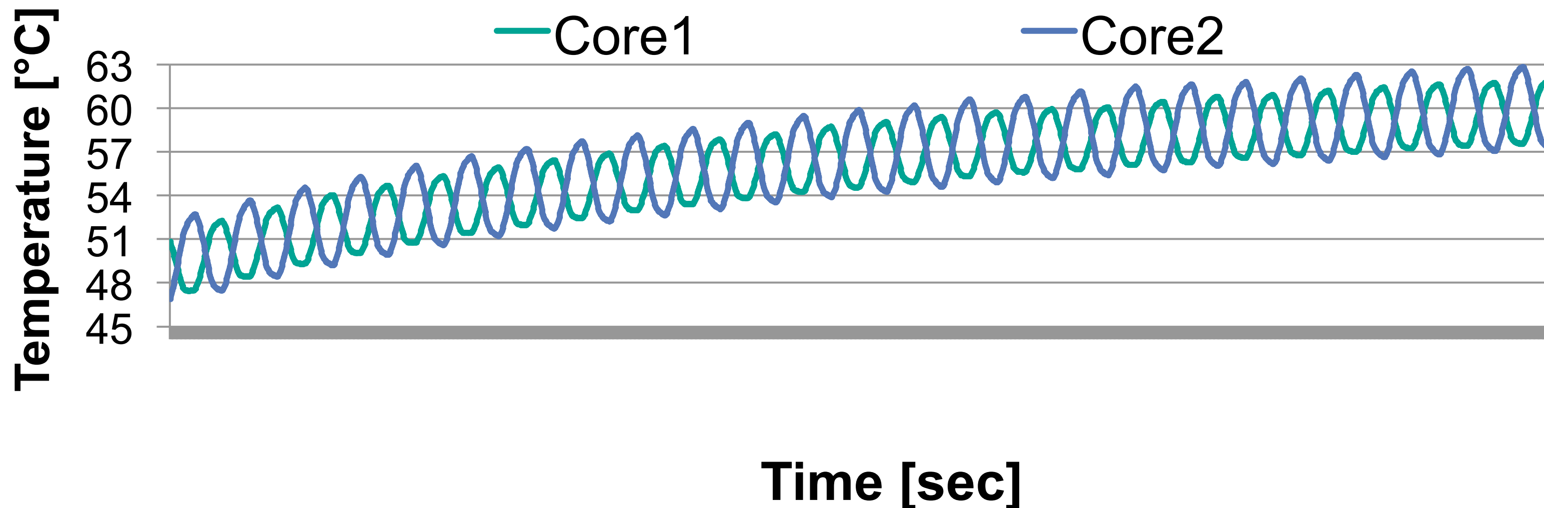


Example: Thermal Cycling in FPGAs

Scr: Amrouch, Ebi, Henkel



Activity migration between two cores at the rate of 154 MCycle



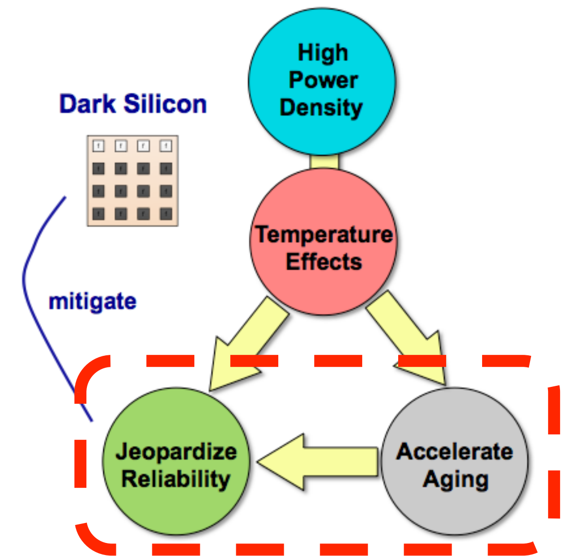
Summary:

Dark Silicon is a thermal problem due to high power density:

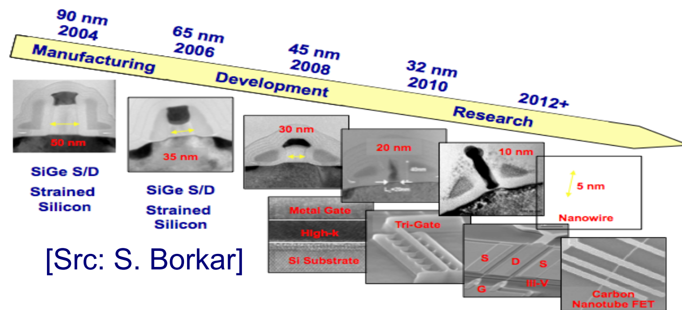
- **Average temperature**
- **Peak temperature**
- **Spatial thermal gradients**
- **Temporal thermal gradients**

=> Accelerate Aging and Jeopardize Dependability!

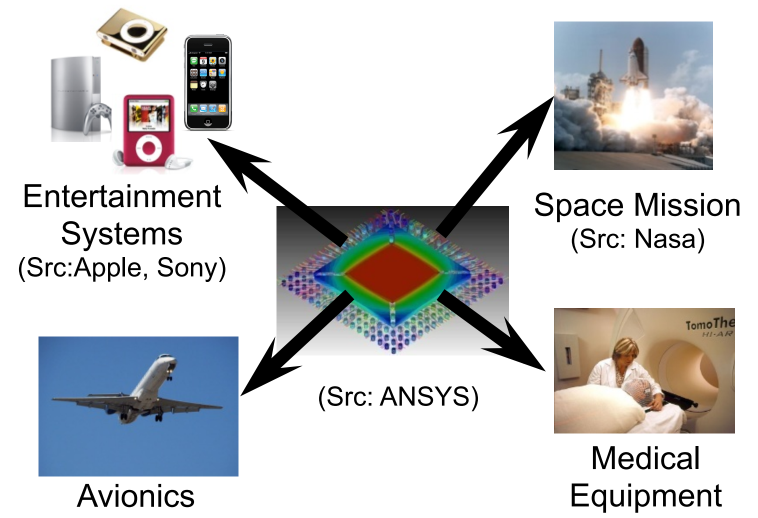
Aging Effects



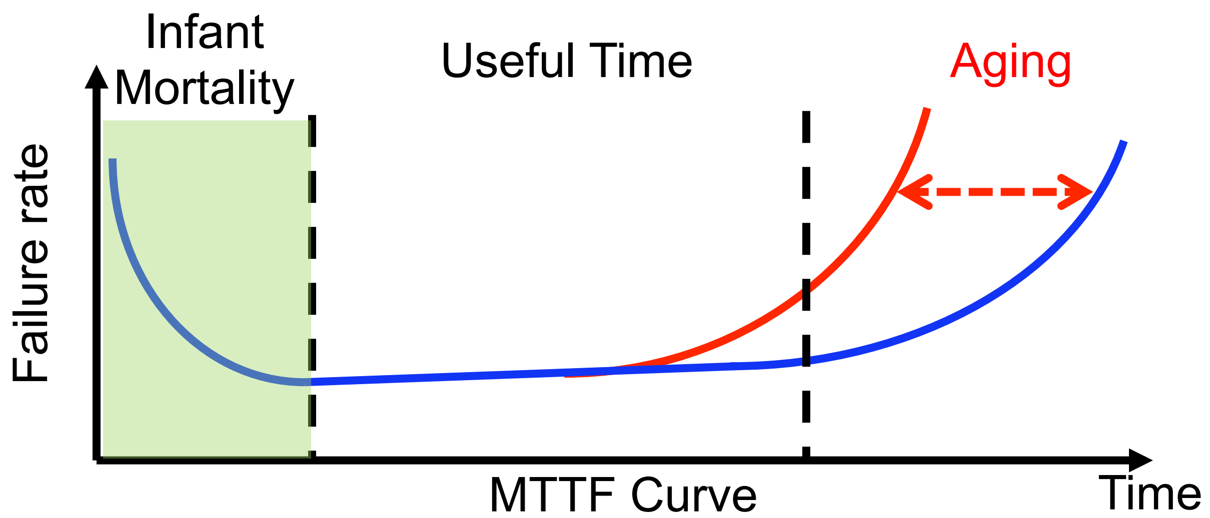
Temperature and Aging Decrease Dependability



[Src: S. Borkar]

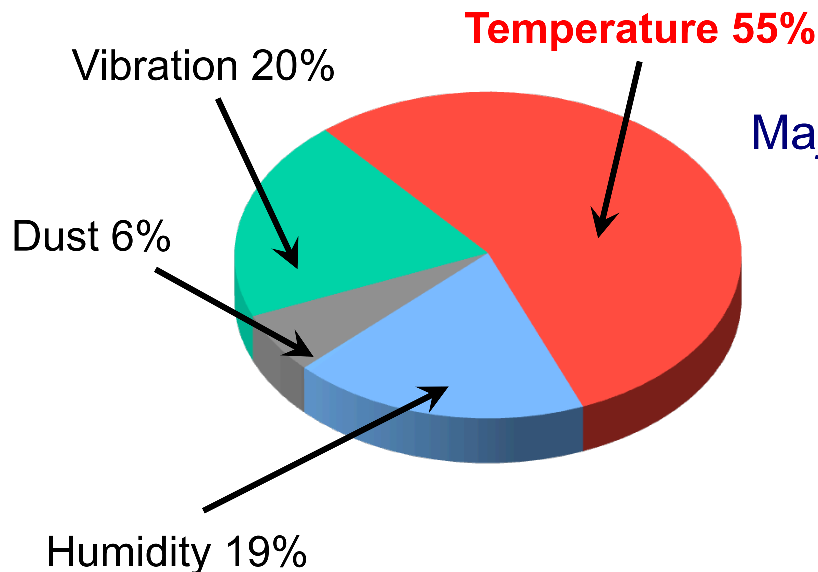


- Technology scaling has made aging-induced reliability degradation a major concern



Temperature and Aging decrease Dependability

- Thermal:
  - Accelerate aging mechanisms
  - Degrade performance
  - Increase leakage power
  - Necessitate expensive cooling



Major Causes of Electronic Failure

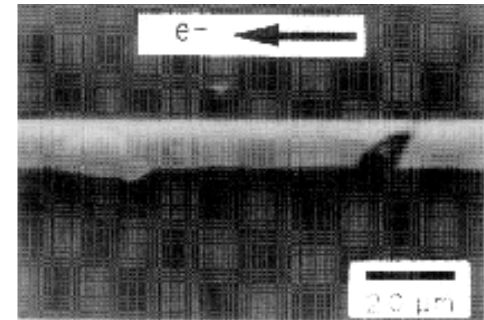
src: www.aitechnology.com/

Aging Effects: Electro-Migration, Variability

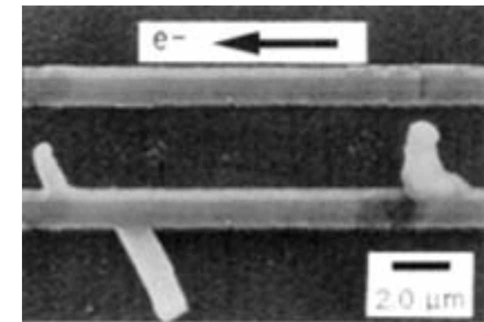
- Process variations and electromigration can result in hillocks and holes

$$MTTF = Aj^{-n}e^{\left(\frac{Q}{kT}\right)}$$

  - Lead to open failures or short circuit failures respectively
  - Failures may be temperature dependent due to material expansion
    - Holes may function normally at high temperatures but fail at low temperatures
    - Hillocks may function normally at low temperatures but short circuit at high temperatures



Hole/crack

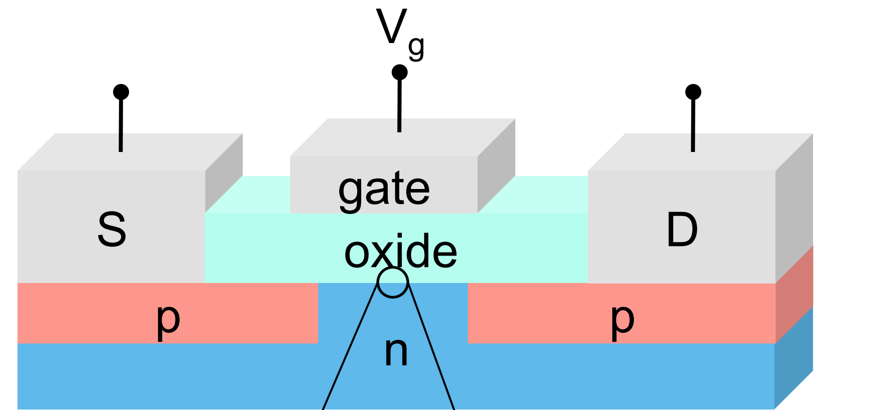


Hillock

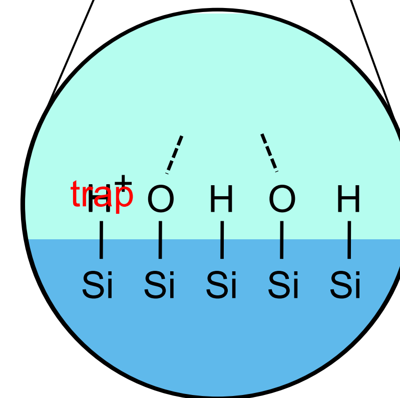
[W.D. Nix, 1992]

Aging Effects: NBTI

- Negative Bias Temperature Instability
  - Breakdown of Si-H bonds at the silicon-oxide interface due to voltage/thermal stress
    → causes interface traps
- Affects mostly P-MOSFETs because of negative gate bias
  - Effect in N-MOSFETS is negligible
- Despite research focus:
  NBTI is not yet fully understood!



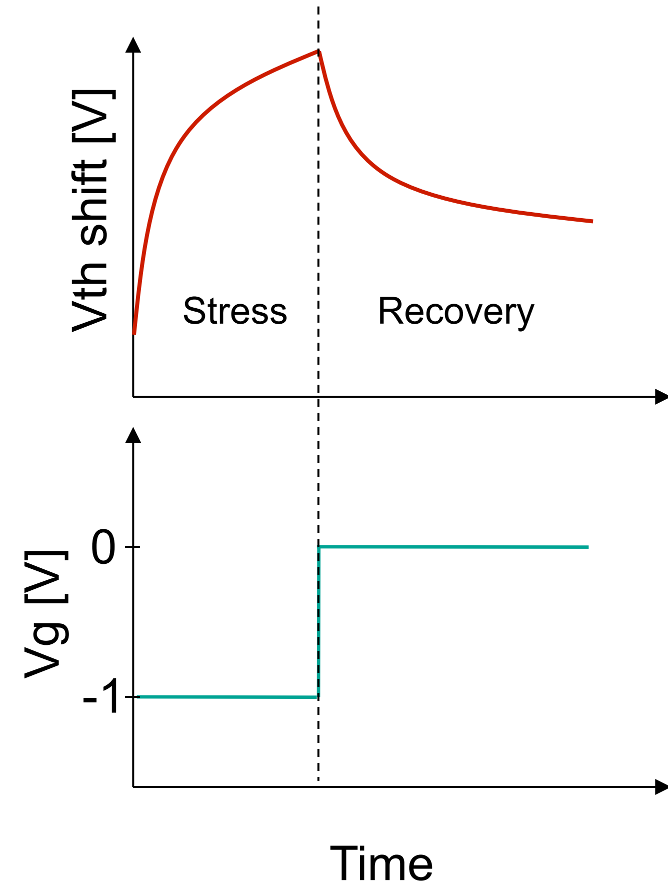
P-type MOSFET
reaction-diffusion model



$V_g < 0$ → STRESS!

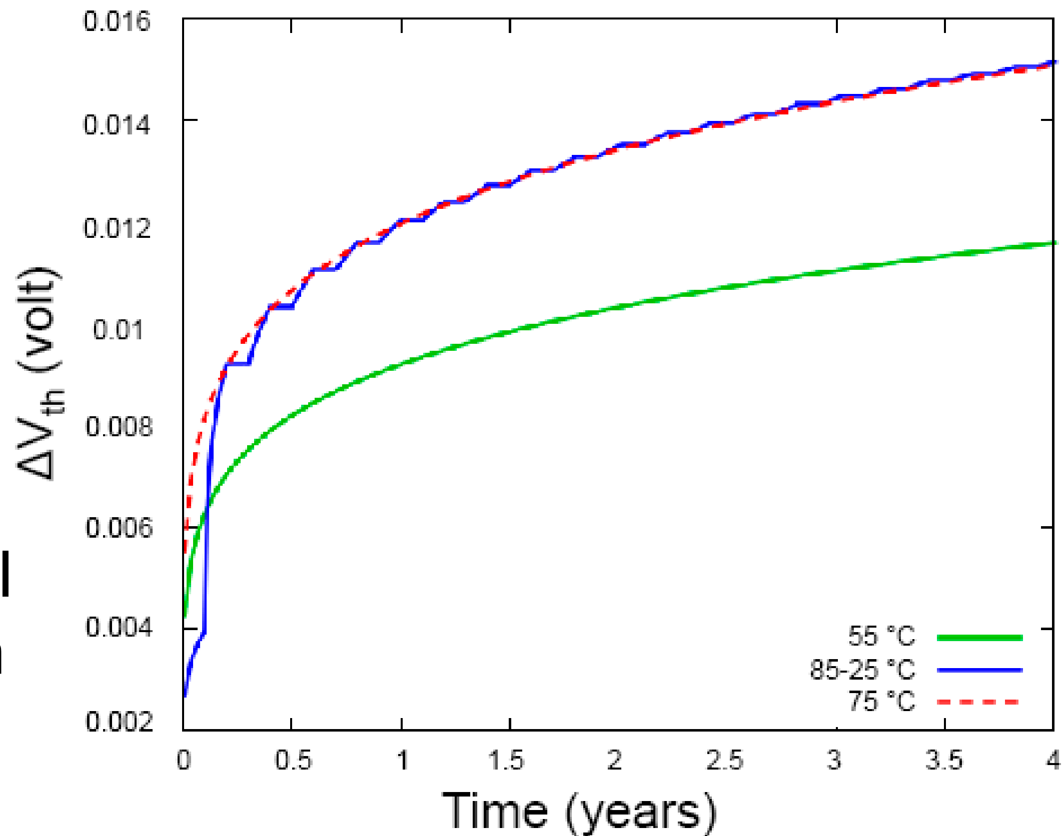
Aging Effects: NBTI

- NBTI manifests itself as a shift in V_{th}
  - Causes increase in transistor delay
  - Delay faults are responsible for NBTI induced bit-flips and resulting circuit failure
- Recovery effect in periods of no stress
  - When voltage and temperature are low, V_{th} can shift back towards its original value
  - Full recovery from a stress period only possible in infinite time
    → In practice overall V_{th} shift increases monotonously over longer periods, e.g. months/years



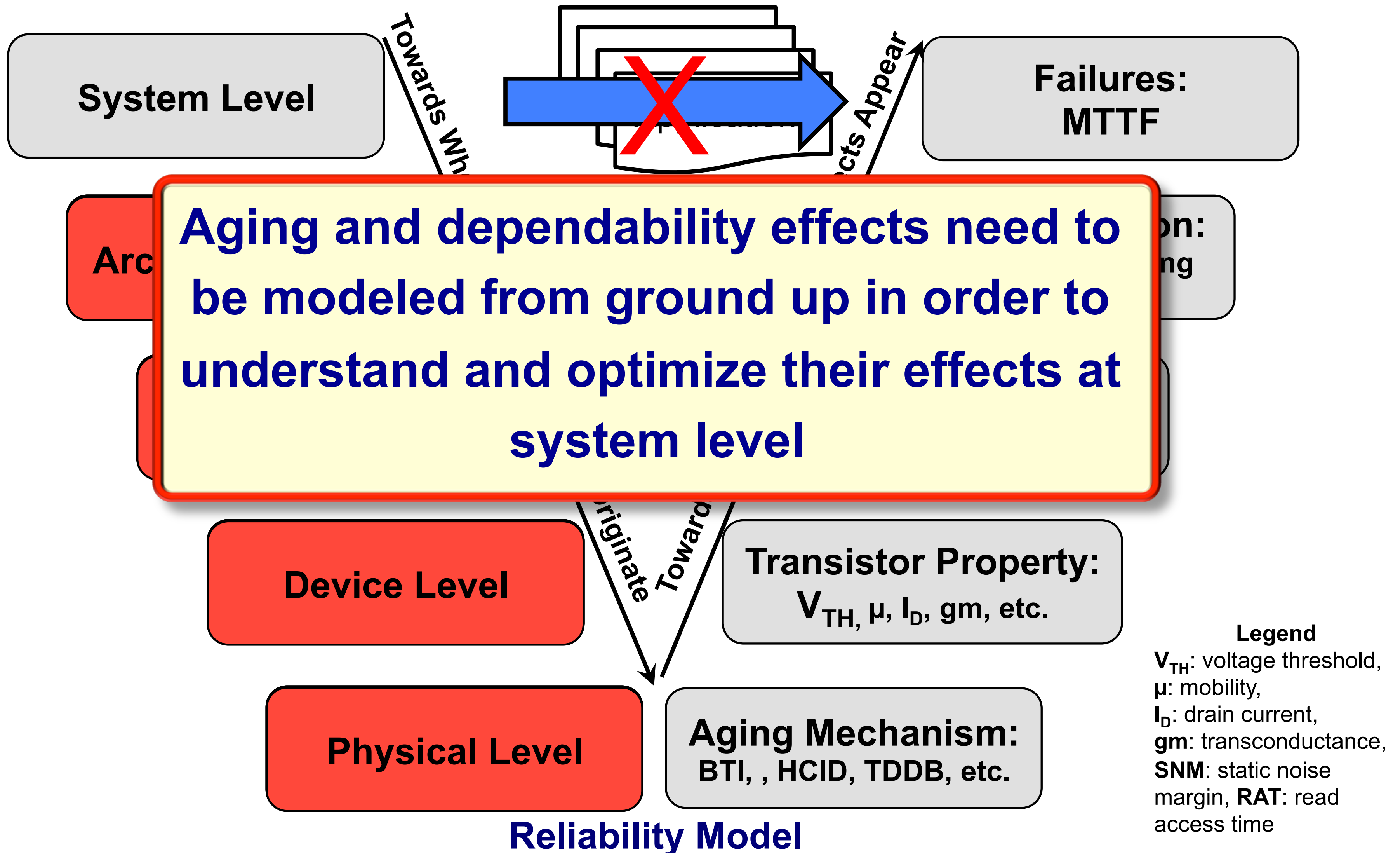
Aging Effects: NBTI and Temperature

- Temperature plays important aspect in NBTI modeling
- Higher temperatures increase shift in threshold voltage
- ΔVth approximately 50% higher at 75°C than 55°C
- NBTI effect at 75°C is approximately equal to alternating between 85°C and 25°C

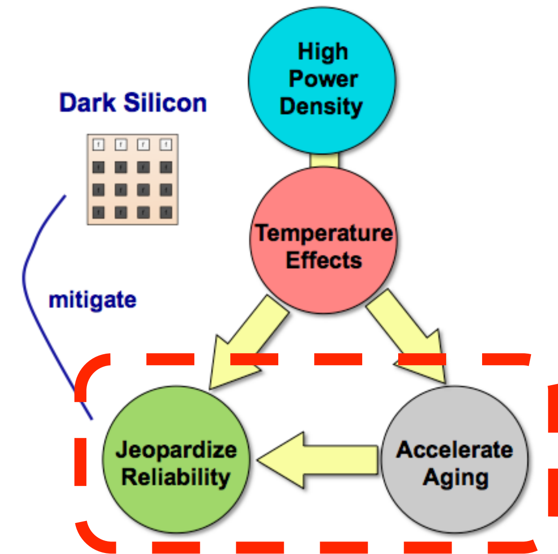


So, how to *accurately* model temperature (aging etc.) effects … ?

Temperature through abstraction levels



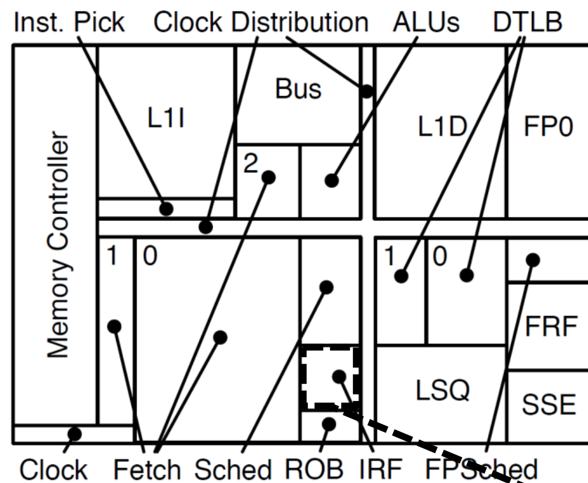
Temperature/Aging Effects
Ex: 6T SRAM cell

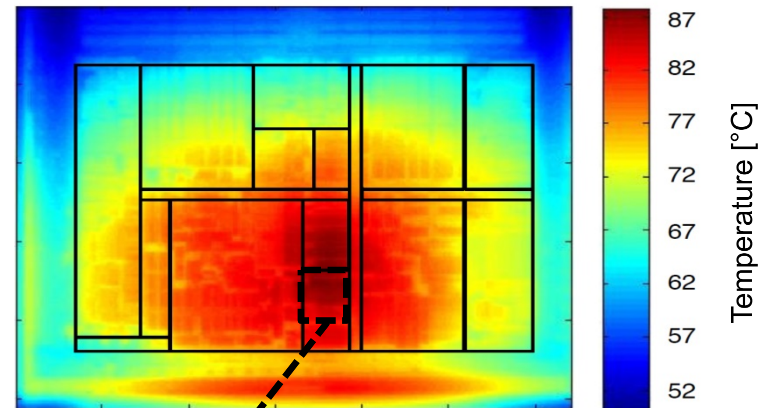


Example: Register File

- It has: relative small area footprint + frequently accessed
  → High power density → high temperature → higher temperature/aging effects

The hotspot is located at the register file in for most of the applications





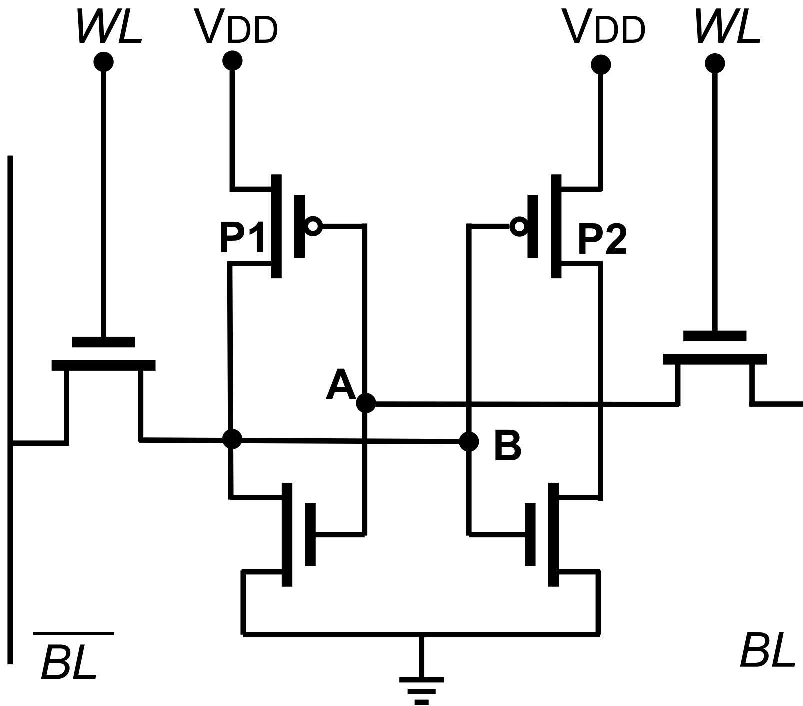
Integer Register File

AMD Athlon-64 core floorplan

Thermal Image of using infrared camera

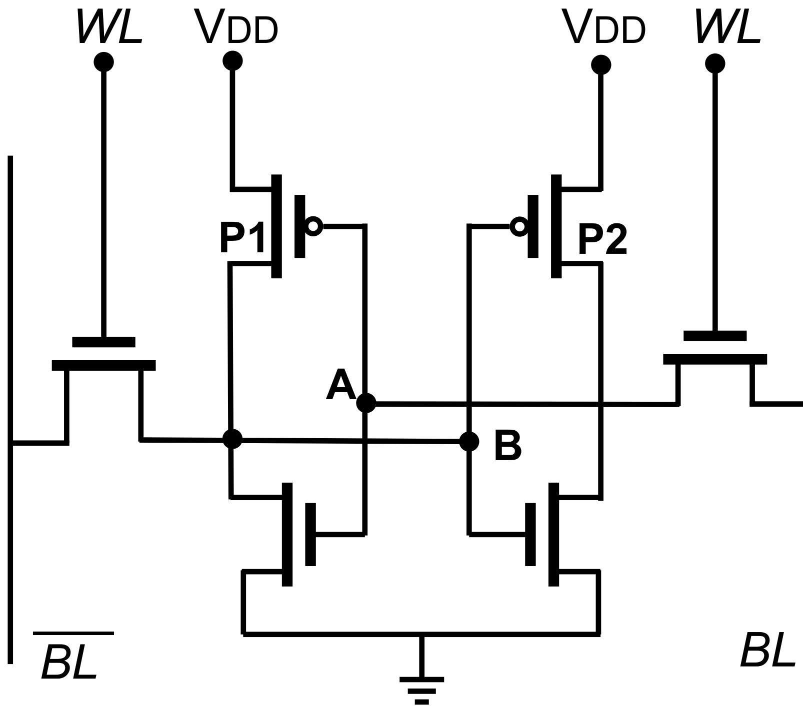
scr: Renau et al. ISCA 2007, IPDPS'08

Impact of Temperature on 6-T SRAM Reliability



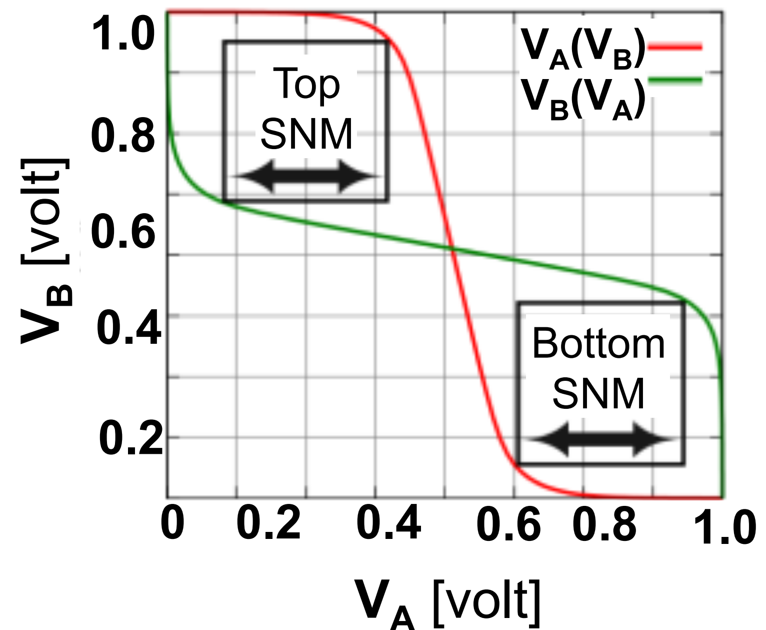
- Reliability relevant parameters
  - Static Noise Margin (SNM)
    Susceptibility to Noise
  - Read Access Time (RAT):
    Providing correct data in time
  - Critical Charge (Qcrit):
    Susceptibility to radiation

Impact of Temperature on 6-T SRAM Reliability



- Key reliability aspects
  - Static Noise Margin (SNM)

    Susceptibility to Noise during read operations



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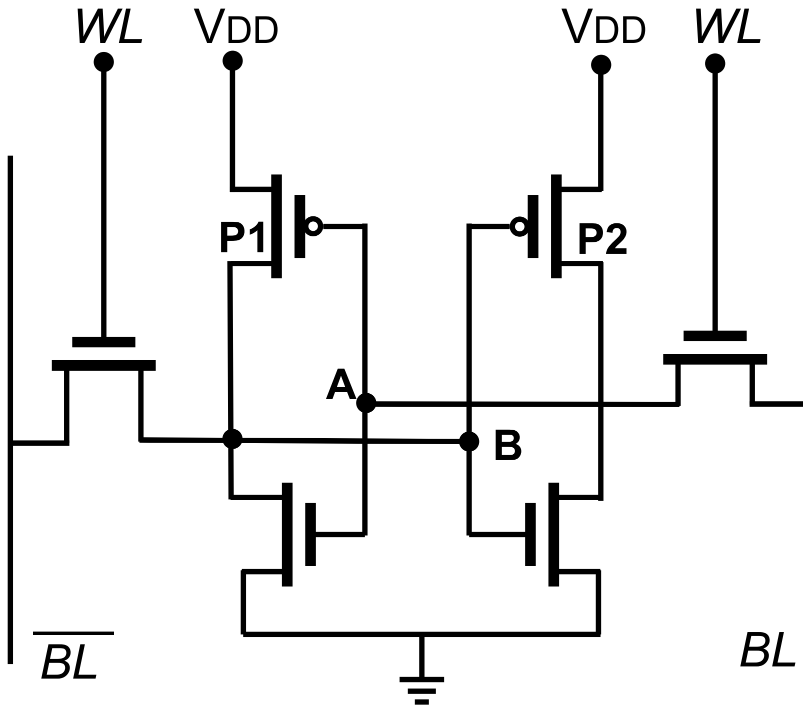

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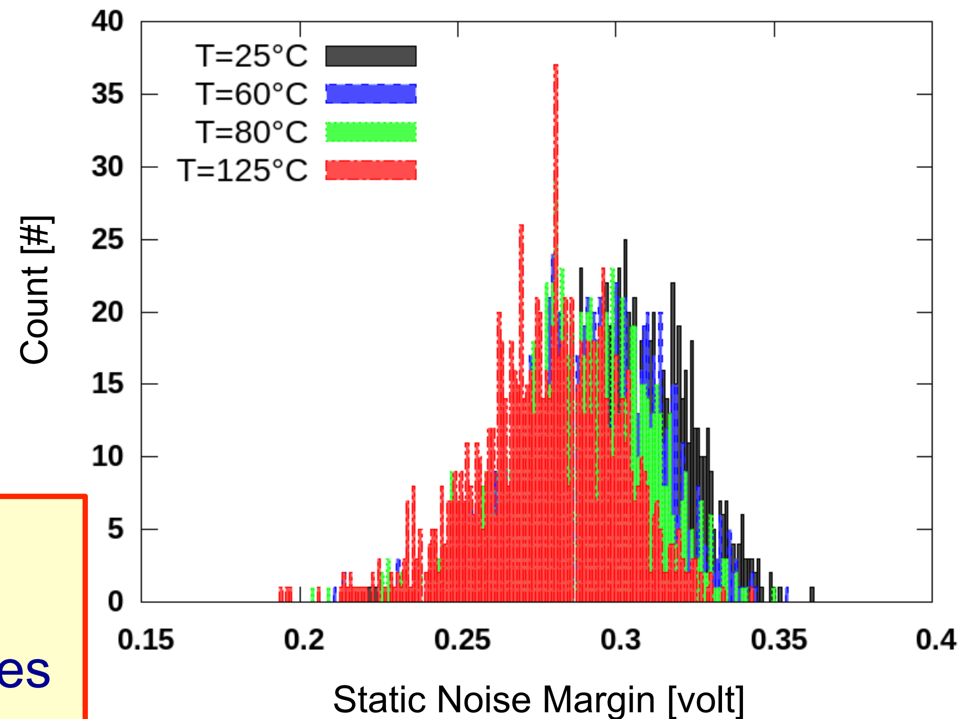
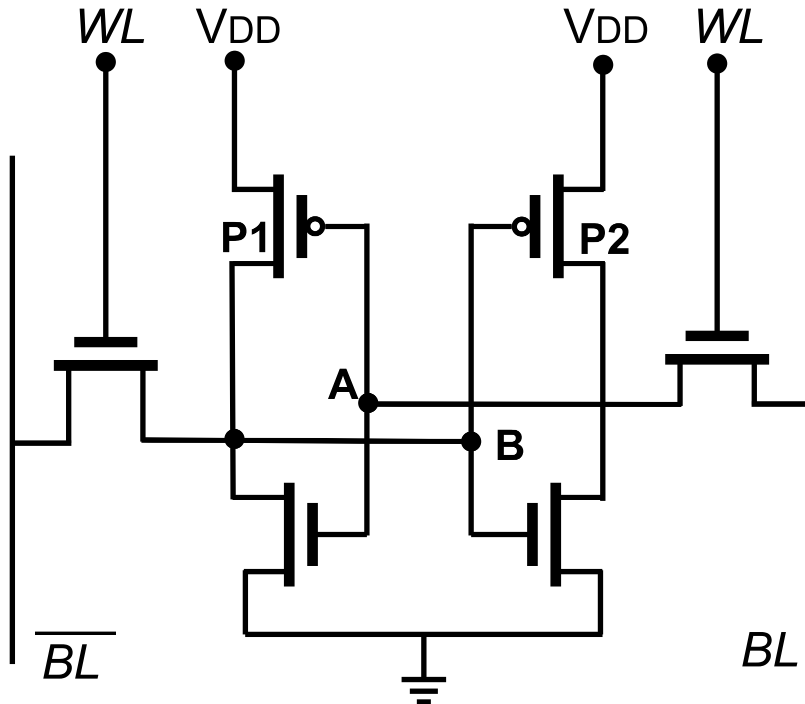
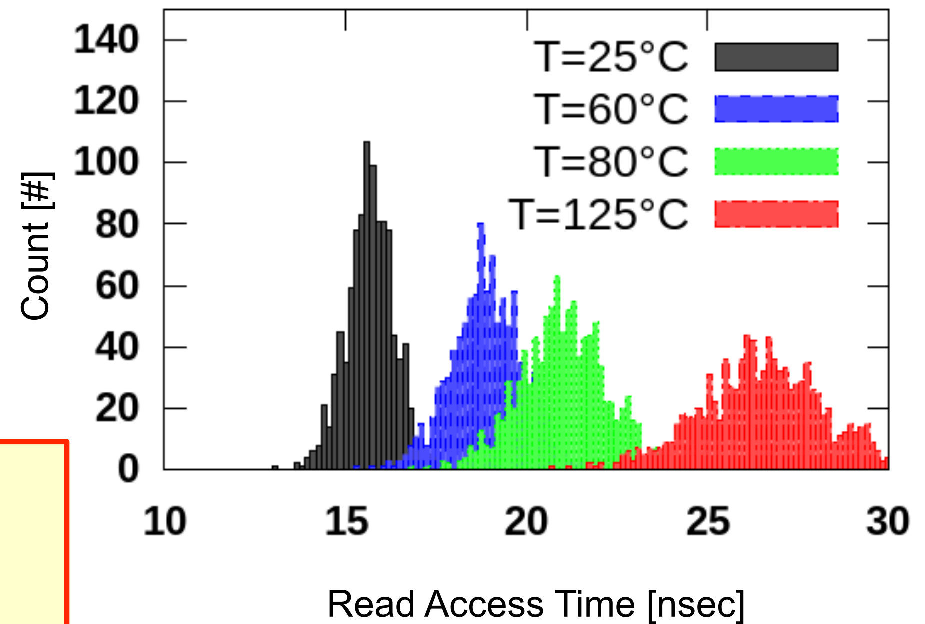


Elevated temperature reduces the SNM and thus the SRAM resiliency against noise degrades

Impact of Temperature on 6-T SRAM Reliability

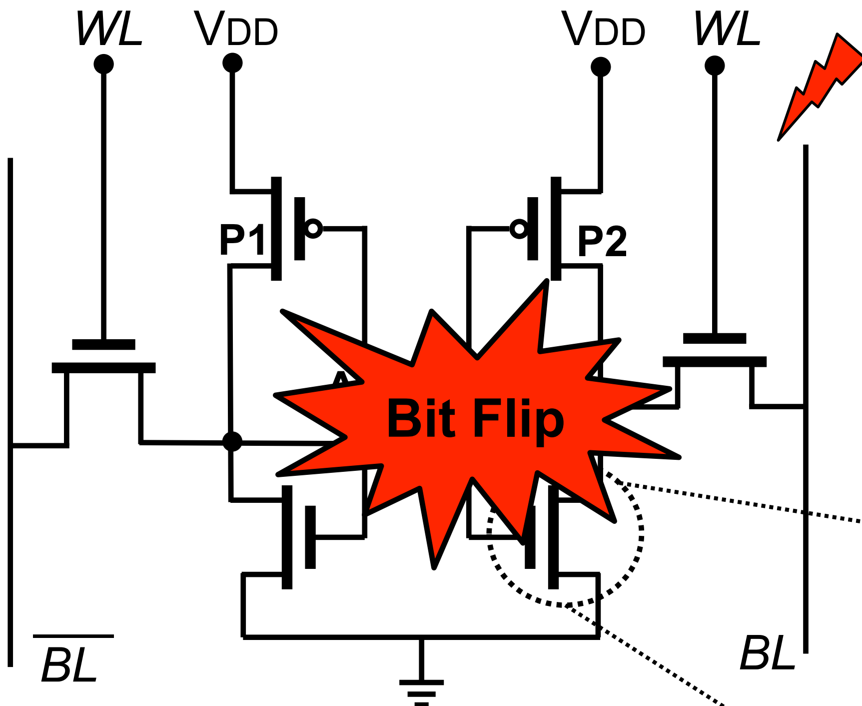


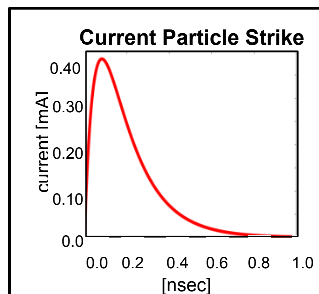
- Key reliability aspects
  - Read Access Time (RAT):
    Providing correct data in time



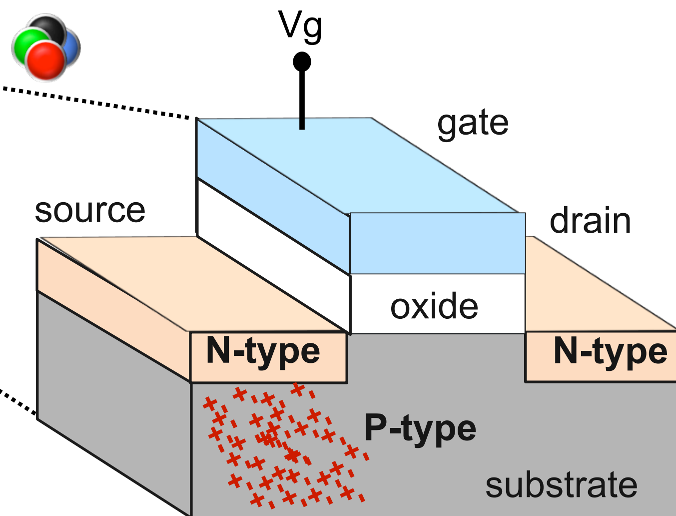
Elevated temperature increases the RAT and thus the SRAM becomes slower

Impact of Temperature on 6-T SRAM Reliability





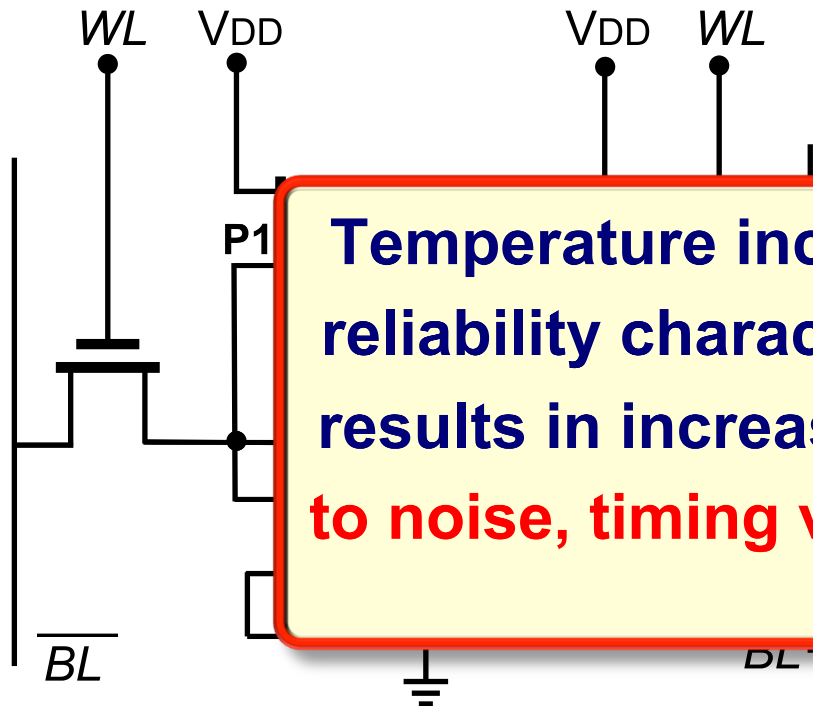
- Key reliability aspects
  - Critical Charge (Qcrit): *Susceptibility to radiation*

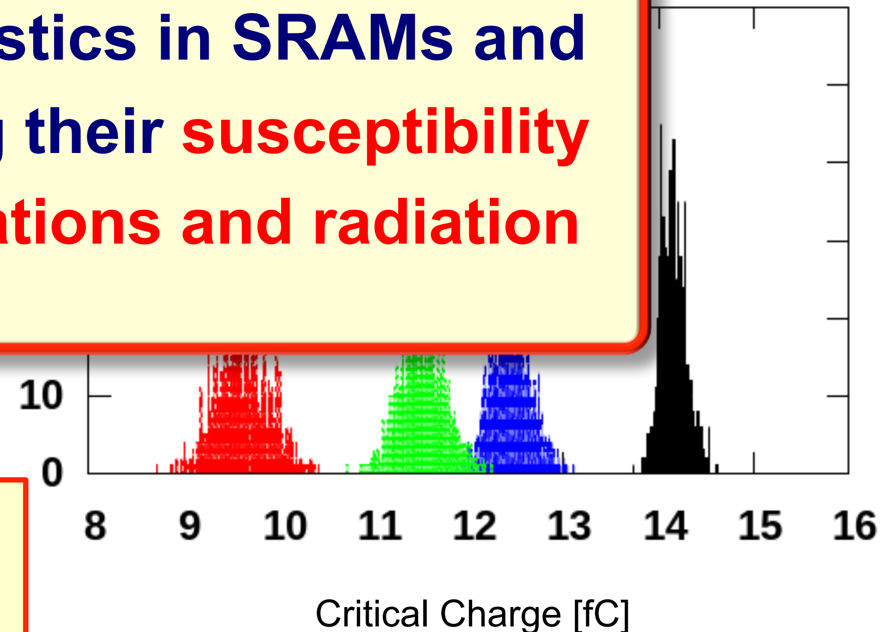


Radiation mechanism

Impact of Temperature on 6-T SRAM Reliability

- Key reliability aspects
  - Critical Charge (Qcrit): *Susceptibility to radiation*

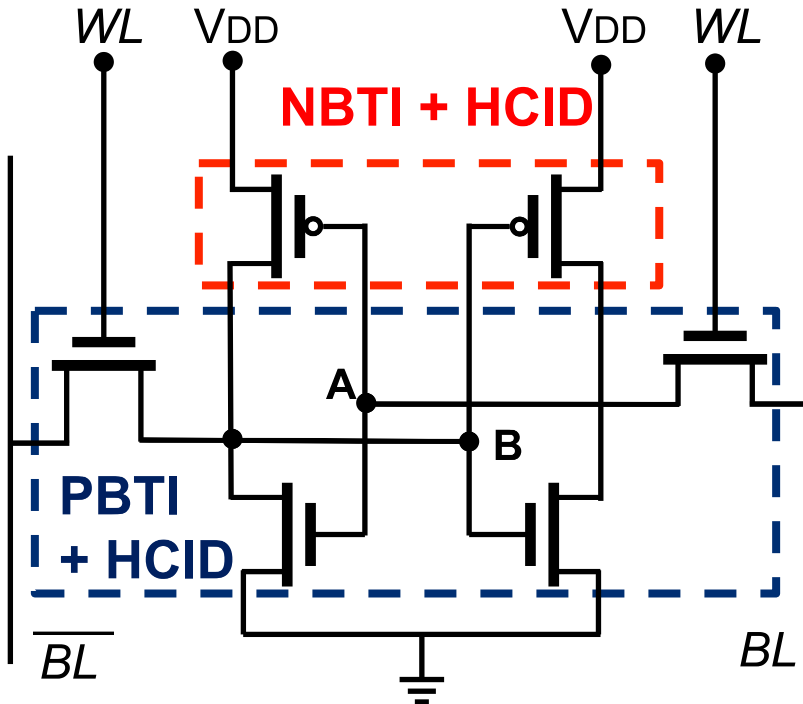




Temperature increase changes the key reliability characteristics in SRAMs and results in increasing their susceptibility to noise, timing violations and radiation

Elevated temperature reduces the Qcrit and thus weaker particles become able to cause soft errors

Aging Imapct in 6-T SRAM Cells



- Key reliability aspects
  - Read Access Time (RAT):
    Providing correct data in time
  - Critical Charge (Qcrit):
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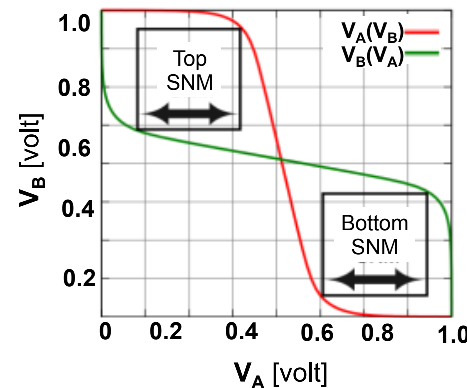
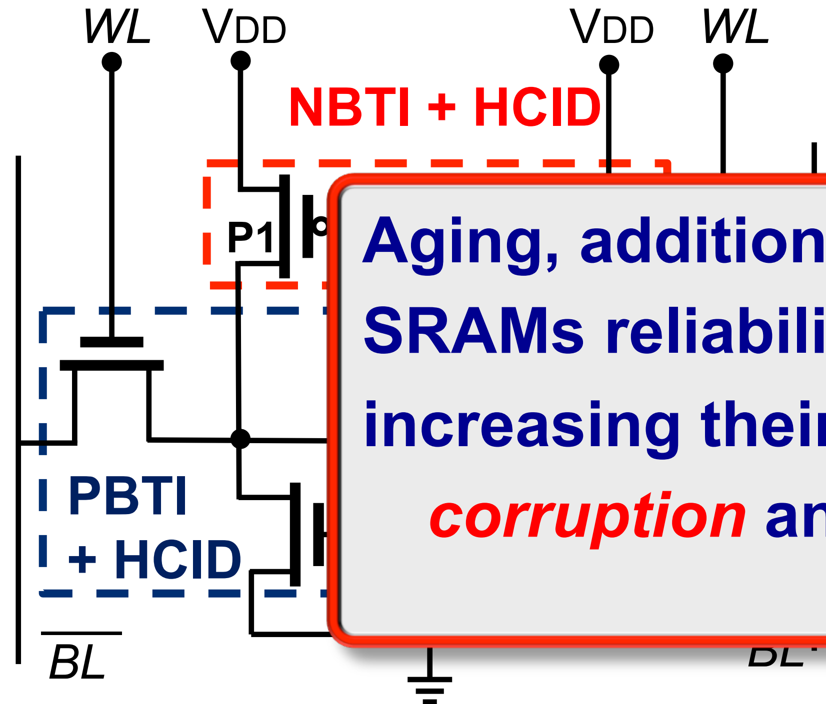
  - Static Noise Margin (SNM)
    Susceptibility to Noise

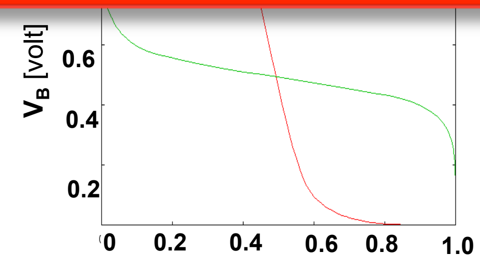


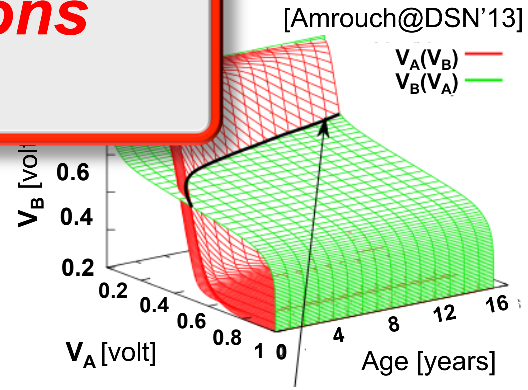
Aging Imapct in 6-T SRAM Cells



- Key reliability aspects
  - Read Access Time (RAT): *Providing correct data in time*
  - ...it):
  - ...*iation*
  - ...(SNM)
  - ...*se*

Aging, additionally, degrades the key SRAMs reliability aspects resulting in increasing their susceptibility to *data corruption* and *timing violations*





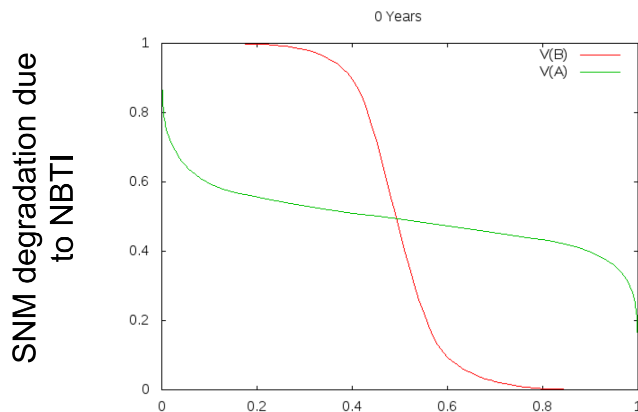
SNM overtime is represented by the space between the red (upper) curve and the green (lower) curve

NBTI Impact on aging: 6-T SRAM Cell

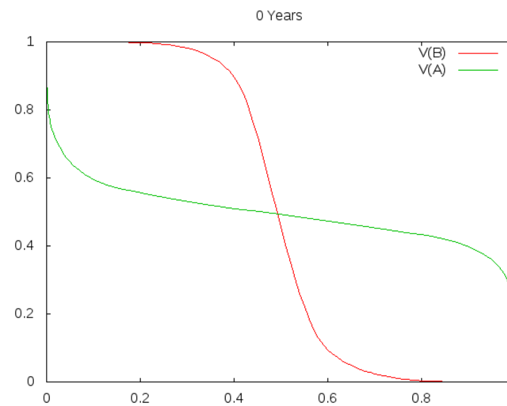
- Static Noise Margin (SNM) is one of the critical reliability metrics in an SRAM cell.
- It represents the immunity of SRAM against noise during the read or write operation
- NBTI highly affects the SNM making the SRAM more susceptible to failure

[Src: IBM, KIT]

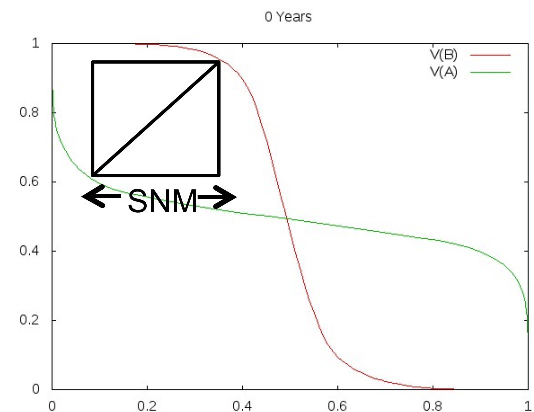
SNM degradation due to NBTI



SRAM transfer characteristics during read operation in the case of α = 0.3 over 11 years



SRAM transfer characteristics during read operation in the case of α = 0.5 over 11 years

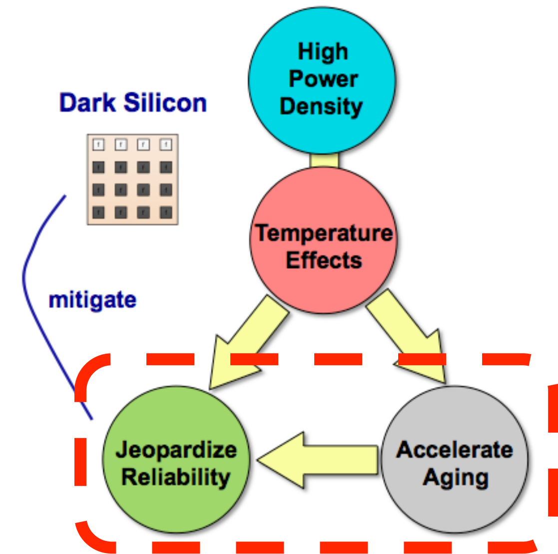


SRAM transfer characteristics during read operation in the case of α = 0.5 during the first year

Summary: Temperature/Aging in 6-T SRAM Cell

- On-chip temperatures directly stimulate underlying mechanisms behind aging phenomena and/or directly influence dependability (instantaneously or long term)
- In the following: how multiple simultaneous temperature/aging mechanisms may interact.

Interaction of Temperature/Aging Effects



Interaction of Aging Effects

physic

device

circuit

architecture

system

Application

Induced stress

NBTI/PBTI

interdependencies

HCID

V_{TH}

μ

SNM

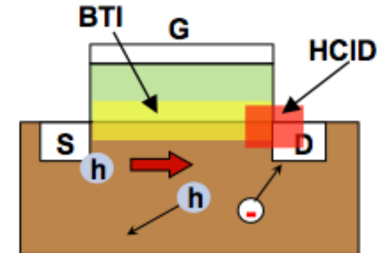
Q_{crit}

Delay

Data Corruption

Timing Violation

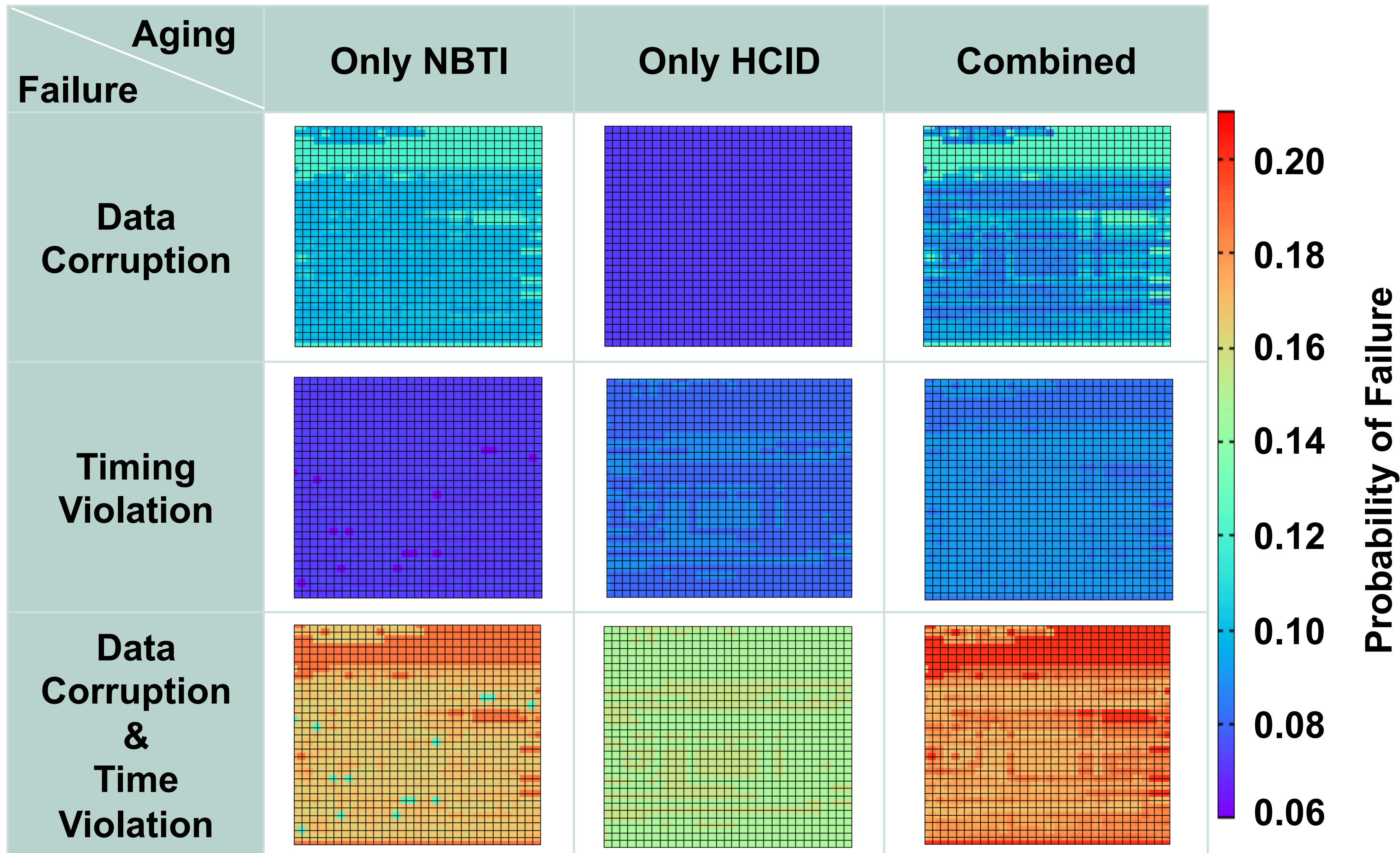
Overall Reliability Degradation



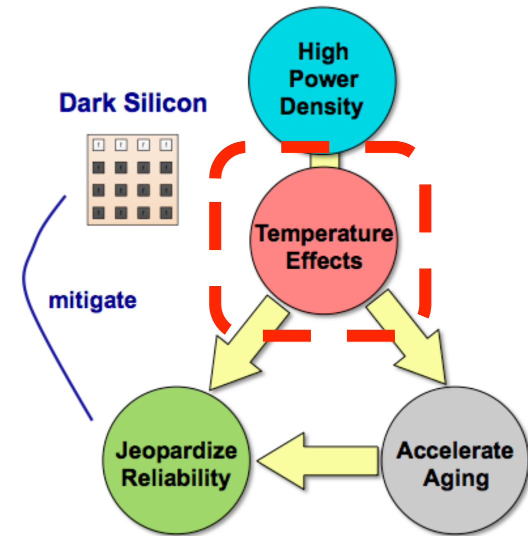
Defects location in a PMOS transistor due to aging

Register File Failure Maps

Hussam Amrouch, Victor van Santen, Thomas Ebi, Volker Wenzel, Jörg Henkel, "Towards Interdependencies of Aging Mechanisms", IEEE/ACM Int'l Conference on CAD (**ICCAD**), 2014.

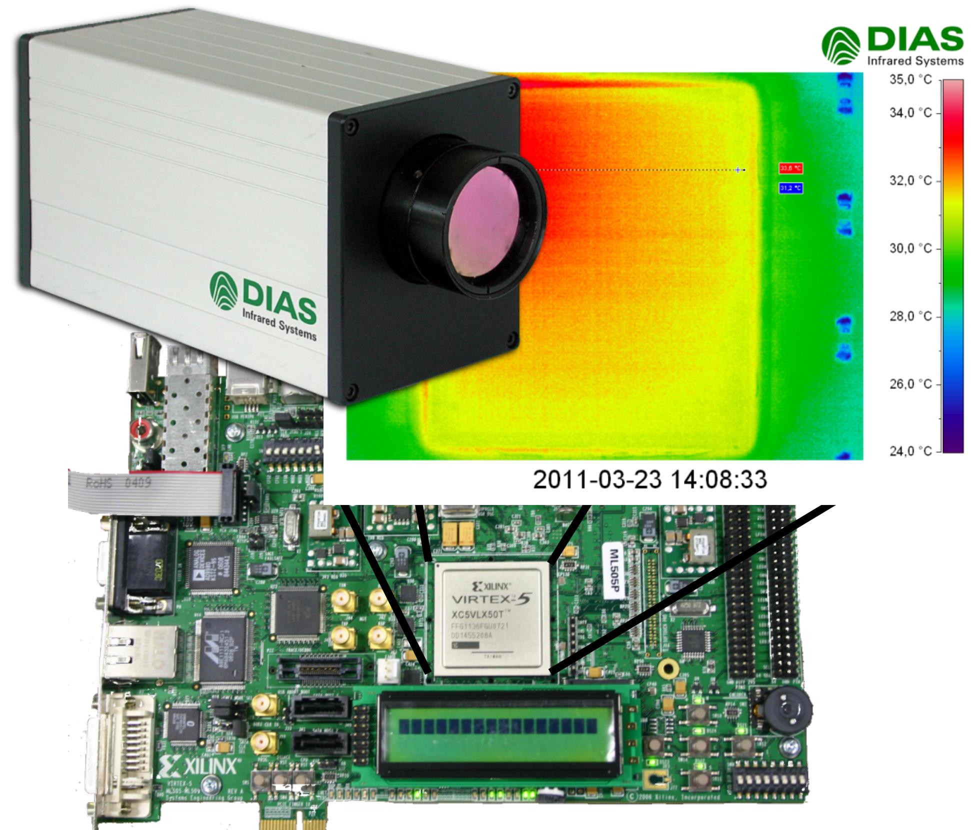


Analyzing Temperature



IR-Camera for thermal Evaluation

- DIAS Pyroview IR Camera
  - Spatial resolution macro lens: around 50µm
    - Limited by camera IR spectral range of 8µm- 14µm
  - Temperature range configurable -20 °C to 120 °C or 0°C to 500°C
  - Sampling rate of 50Hz
    - Camera transmits 50 frames per second over ethernet in real time
  - 384x288 pixels
  - Comprehensive SDK for accessing camera functionality



Src: Henkel, Amrouch, Ebi

Analyzing Temperature of CPUs

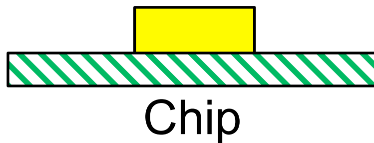
Challenges:

Infrared thermography of ASIC chips requires:

- Removing the chip cooling unit to expose the measured die.
- Building an alternative IR-transparent cooling unit to avoid burning up that:
  - allows the infrared radiation emitted from the chip to reach the thermal camera.
  - concurrently prevents the chip from burning up.

Analyzing Temperature: Basic Setup

Silicon Surface



Two additional layers on top of the measured chip:
- Fluid liquid
- IR window

IR Camera

IR Window
(e.g., Sapphire)

IR
Radiation

Liquid Flow

Inlet
Liquid

Outlet
Liquid

Pump

Liquid
Reservoir

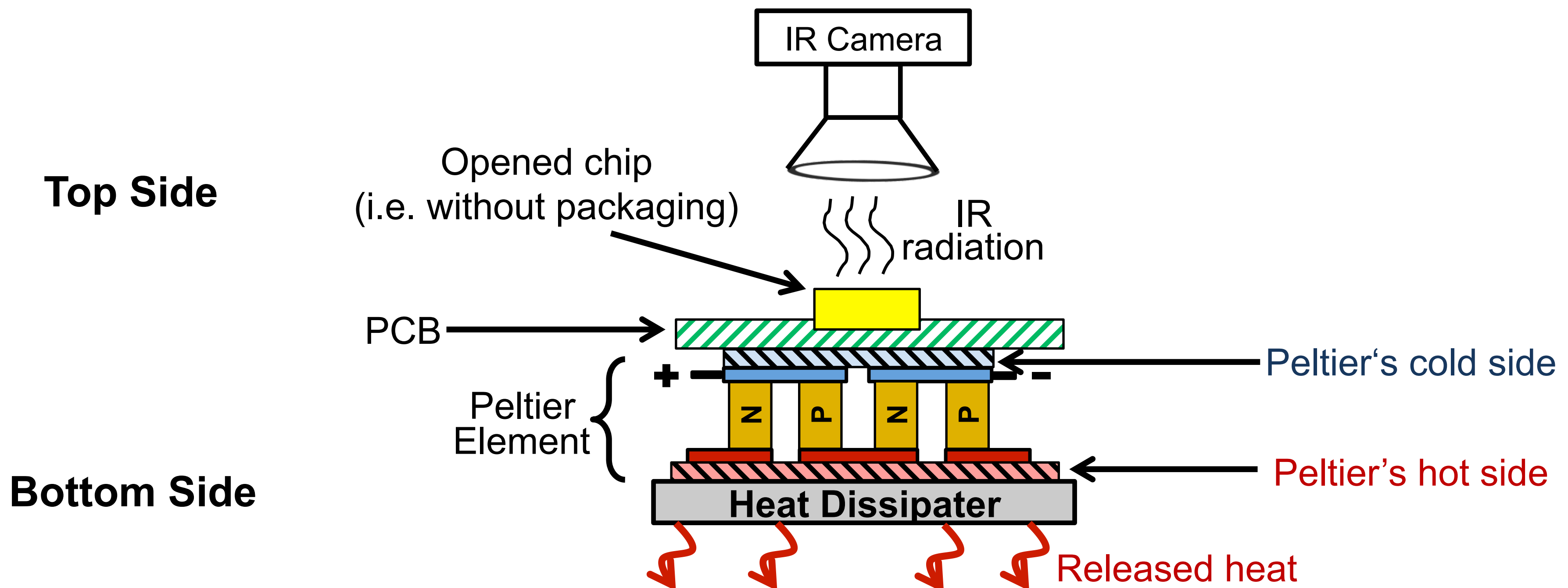
Cooling
Radiator

Hot

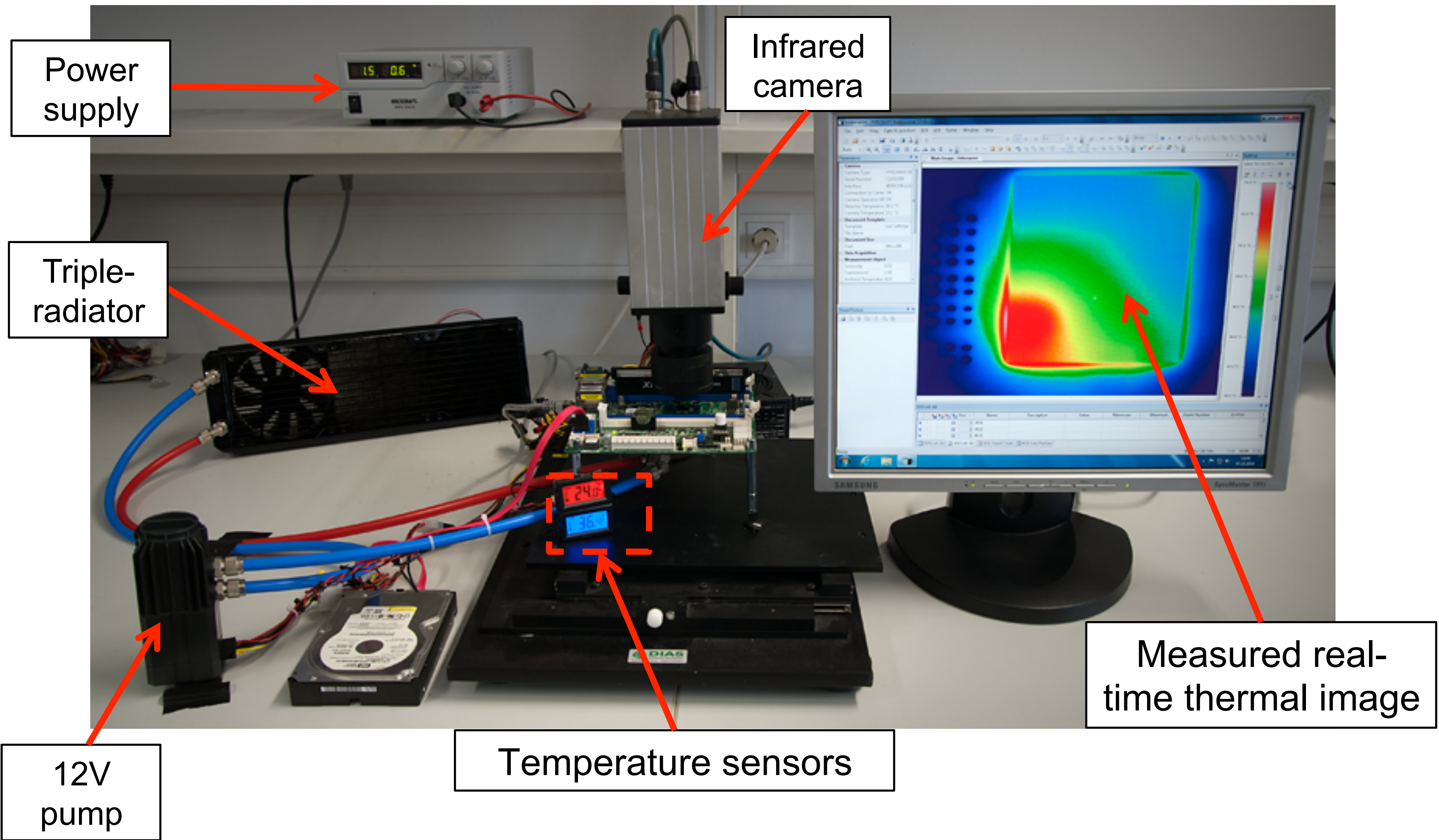
Cold

Analyzing temperature: Current Setup

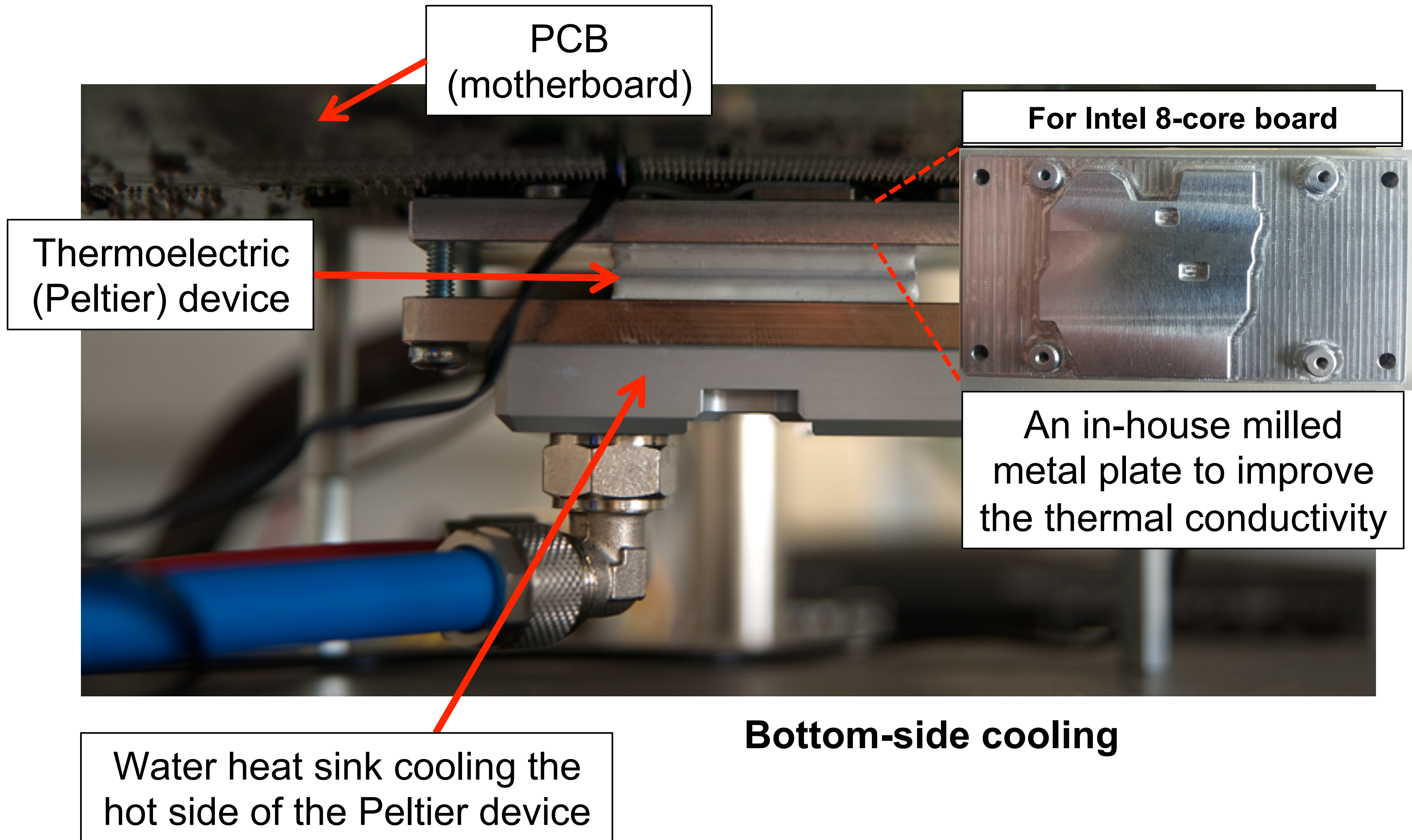
- It continuously chills the measured chip from its bottom side, i.e. through the PCB to which the chip is attached.
- Thermoelectric technology has been employed as it is can provide a stable and controlled source of cooling.



Analyzing temperature: Current Setup



Analyzing temperature: Current Setup

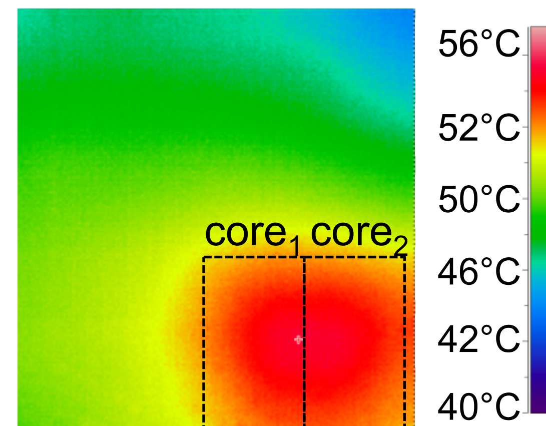


Analyzing temperature: Current Setup

No layer on top of the measured chip

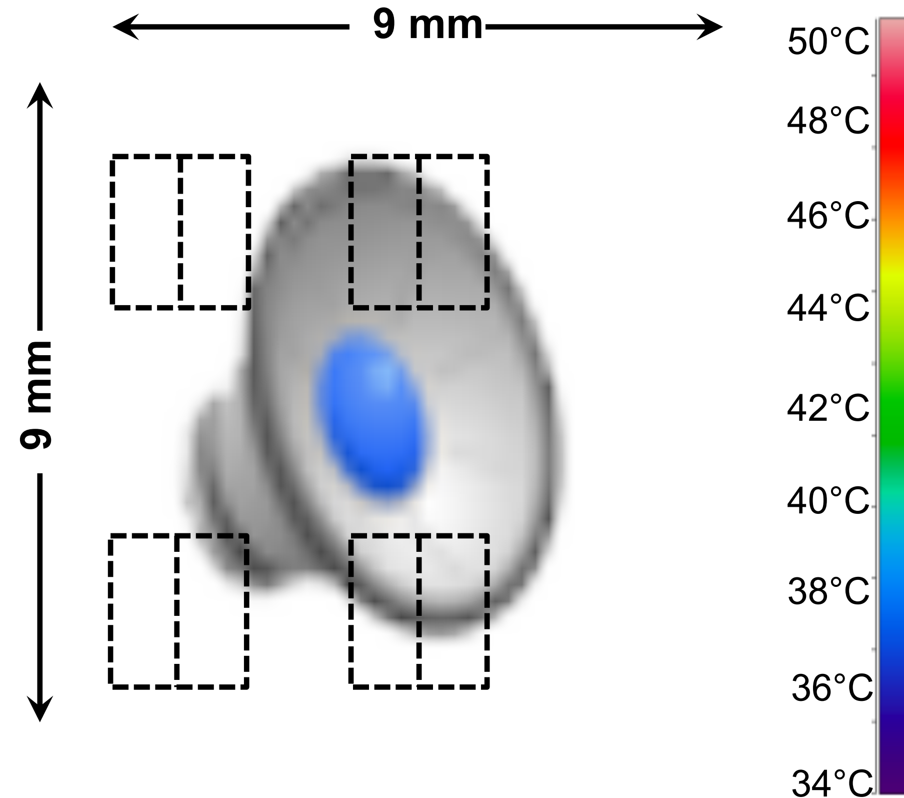
→ the camera can directly and clearly capture the infrared emissions

Example of the captured infrared thermal image of the Atom Intel Dual-Core (45nm) running at 1.8Ghz



Thermal (real-time) Video of an *8-Core* Processor

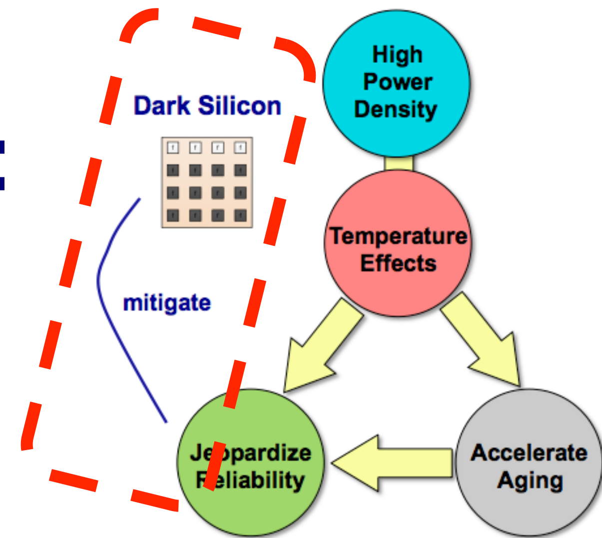
sor



- Operating frequency is **2.4GHz**
- *Two CPUBurn* programs are running and migrated each *3sec* among cores

- *CPUBurn* is designed to load x86 CPUs as heavily as possible for the purposes of maximizing heat production from the CPU

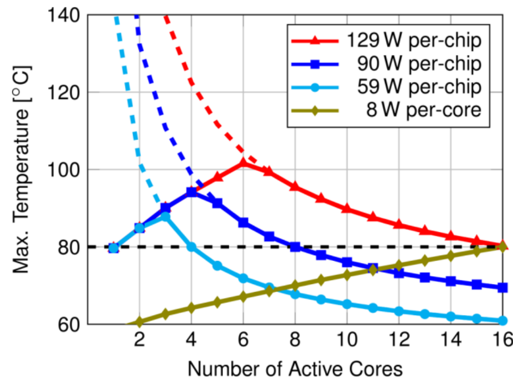
Mitigating Dark Silicon: Overview



Mitigating Dark Silicon

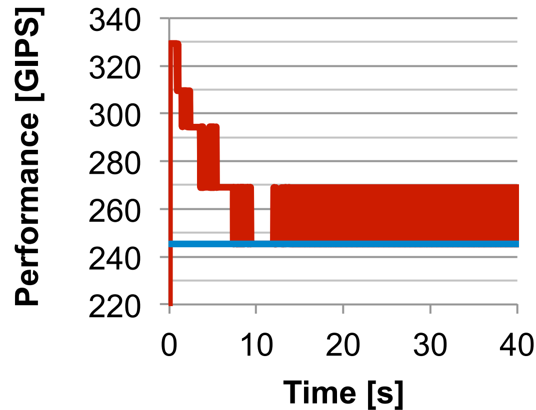
Thermal Safe Power (TSP)

(Abstract from temperature using efficient power budgets)



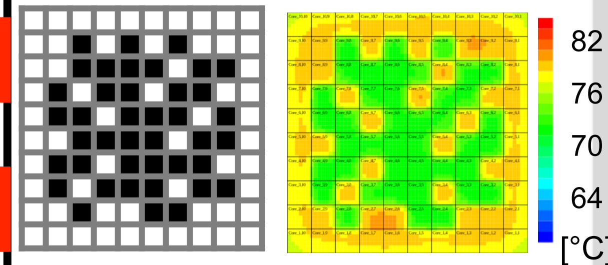
STC / NTC vs. Boosting

(Constant frequency vs. control-loop based boosting)

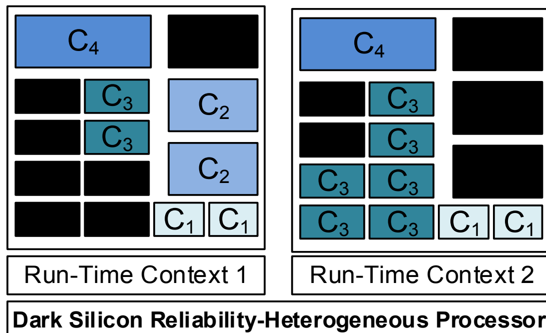


Dark Silicon Management

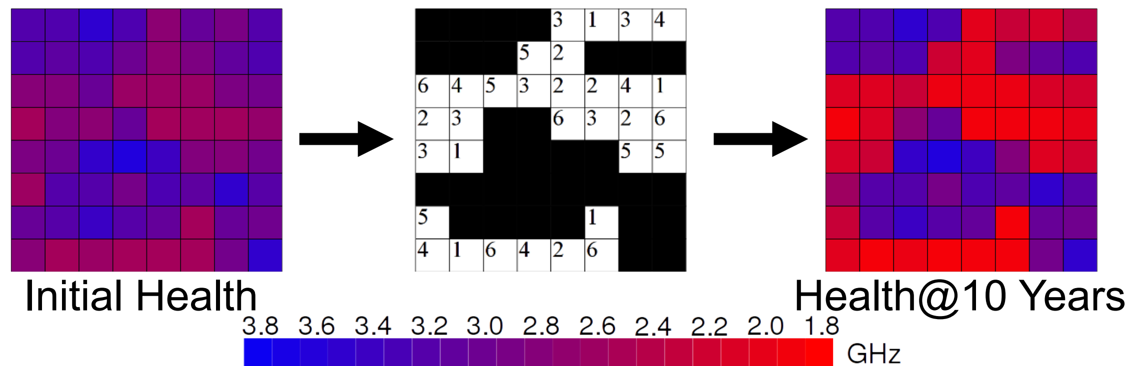
(Patterning and Resource Management)



Dark Silicon-Aware Soft Error Tolerance

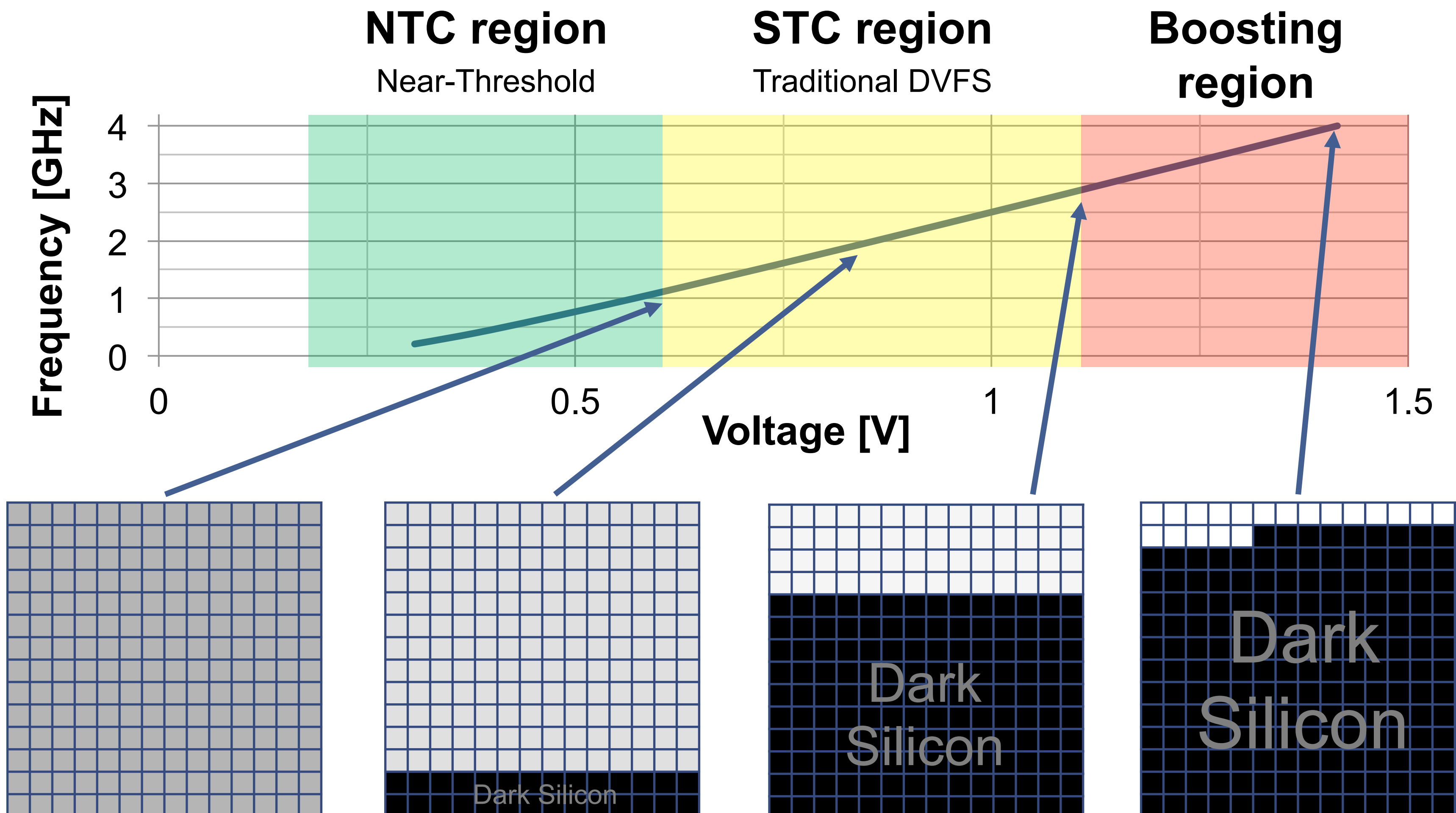


Dark Silicon-Aware Aging Optimization



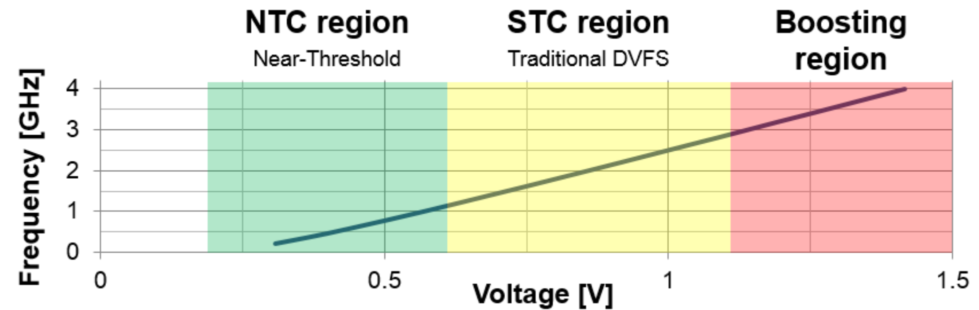
Handling Dark Silicon

- Tradeoff between NTC, Sprinting/Boosting, STC



Power Management Paradigms

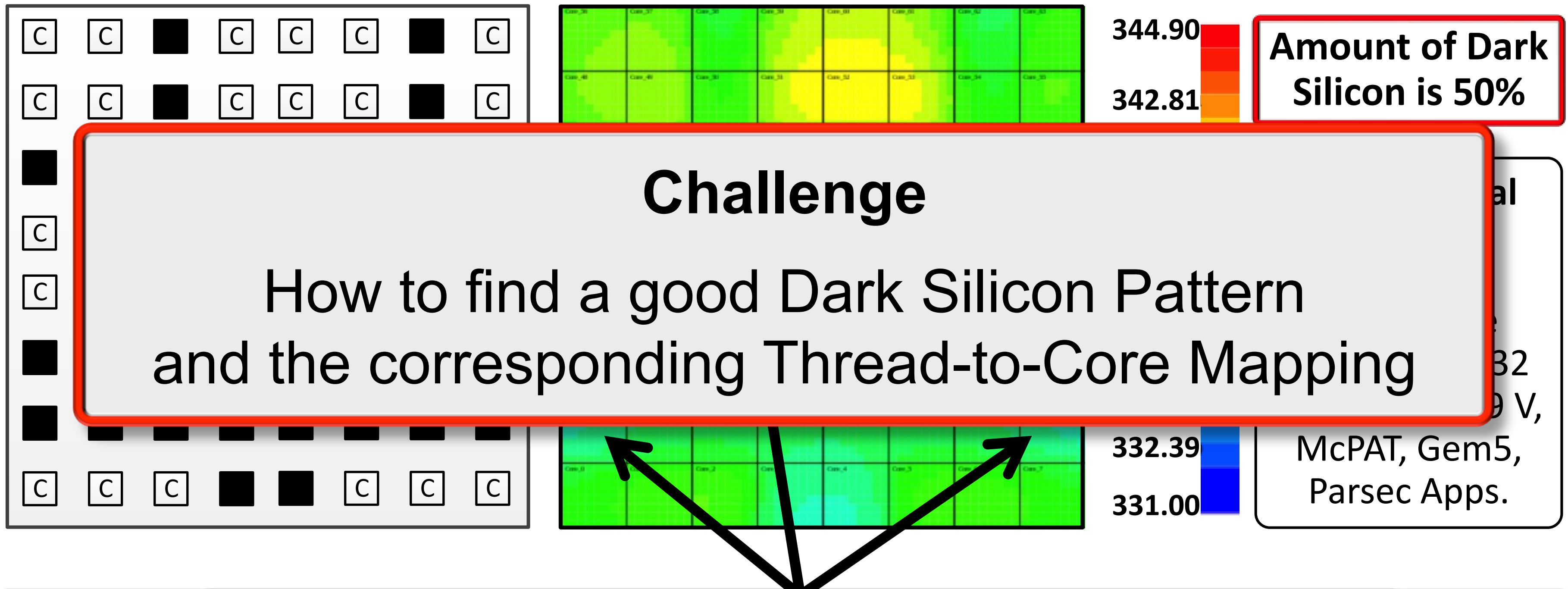
So, when to use what?



Technique	Features	Limitations
DVFS		
NTC		
Boosting		
Computational Sprinting		

Mitigating the Power Density and Dark Silicon: Dark Silicon Patterning

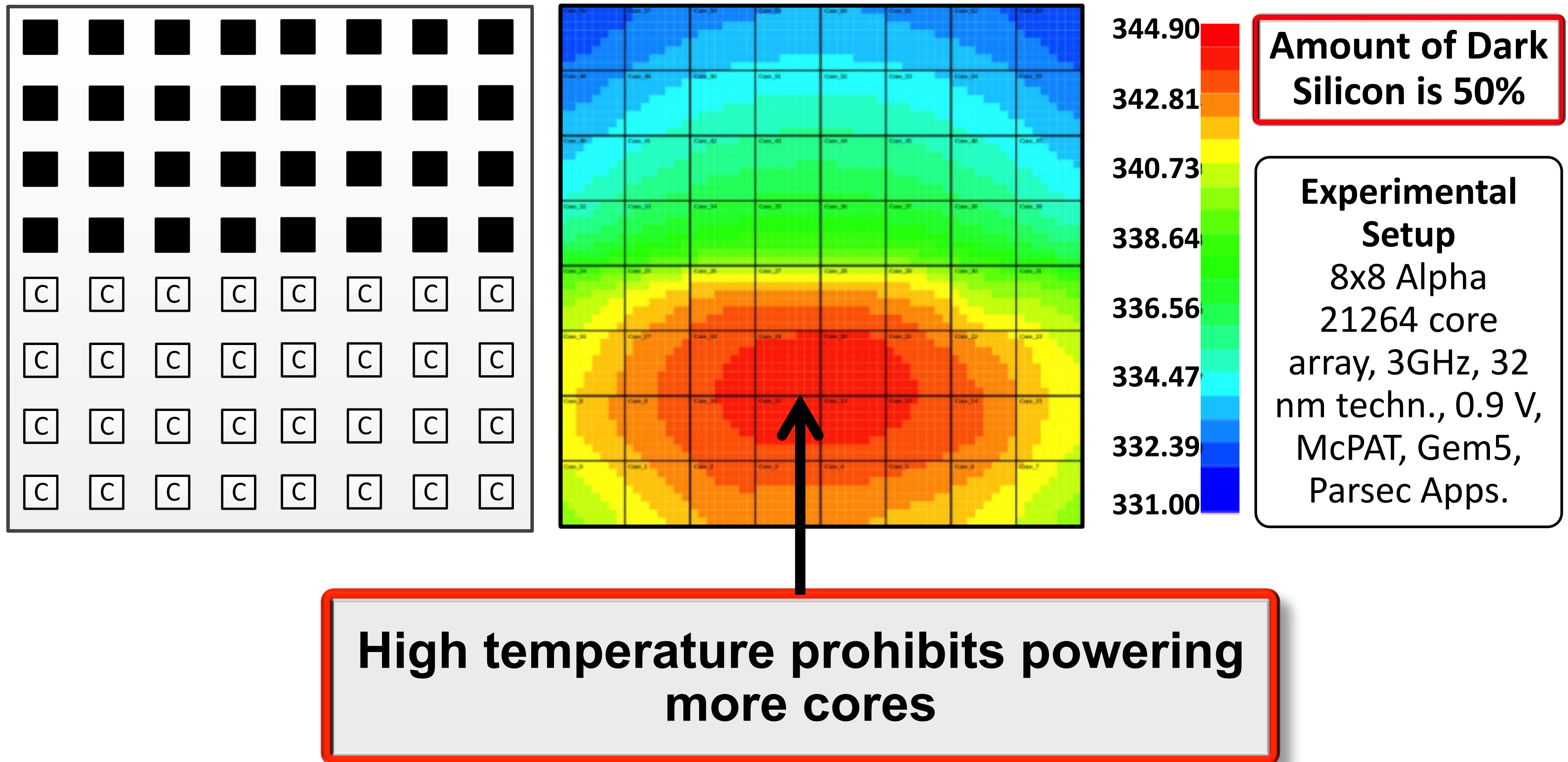
- minimizing peak temp => more effective use of the power budget
- => allows for further parallelization and multi-threading



Other Factors: Workload of Threads and Process Variations

Mitigating the Power Density and Dark Silicon: Dark Silicon Patterning

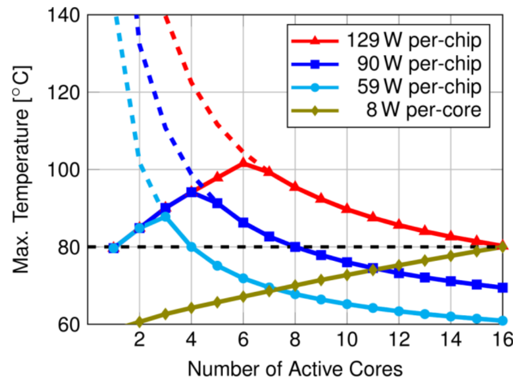
- Spatial and Temporal shutdown -> minimizing peak temp



Mitigating Dark Silicon

Thermal Safe Power (TSP)

(Abstract from temperature using efficient power budgets)



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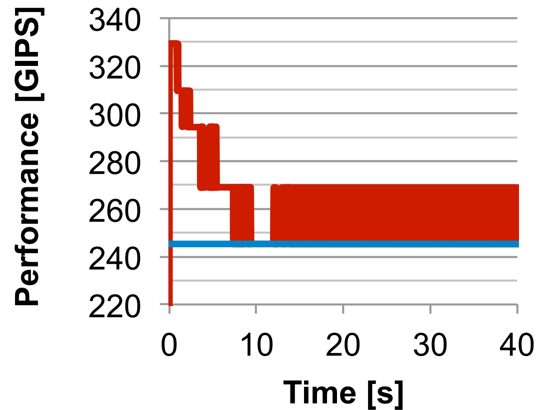
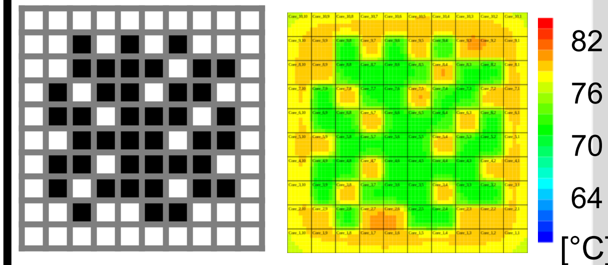
(Constant frequency vs. control-loop based boosting)

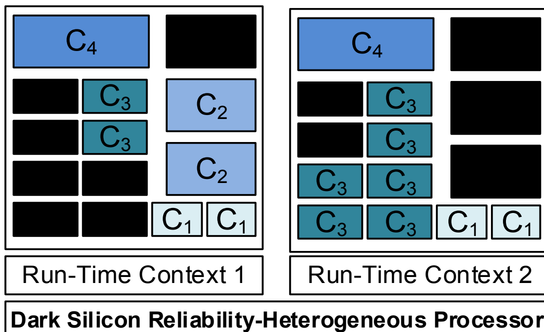


Dark Silicon Management

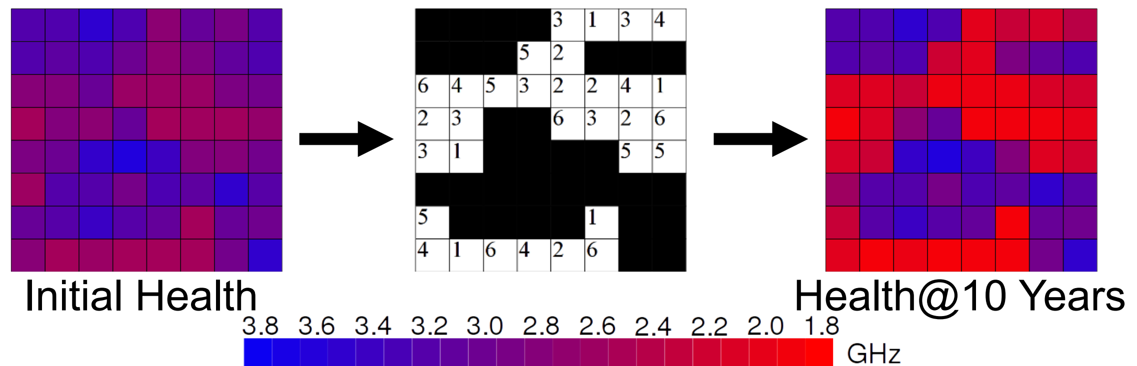
(Patterning and Resource Management)



Dark Silicon-Aware Soft Error Tolerance

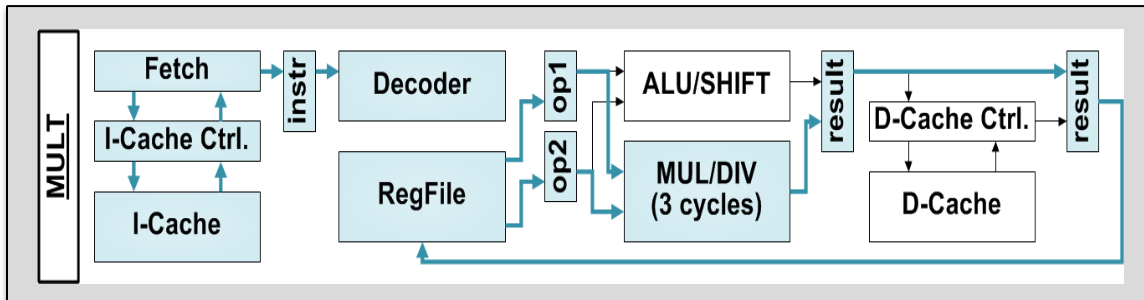


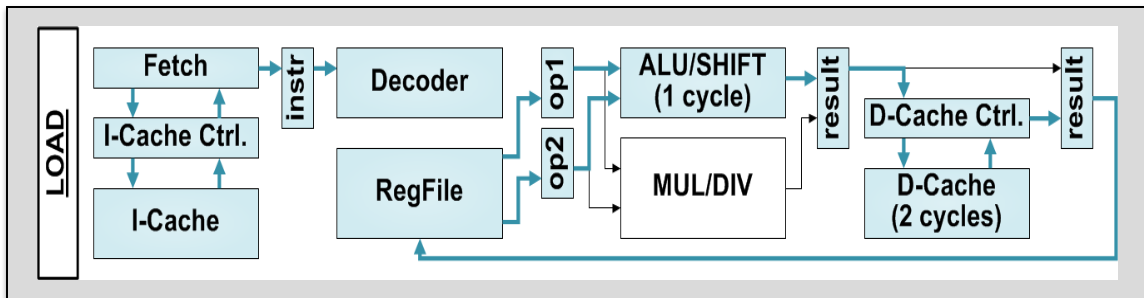
Dark Silicon-Aware Aging Optimization

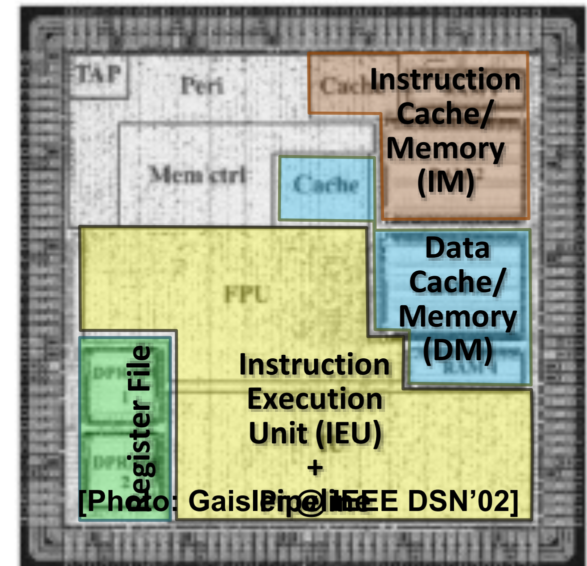


Instruction Vulnerability

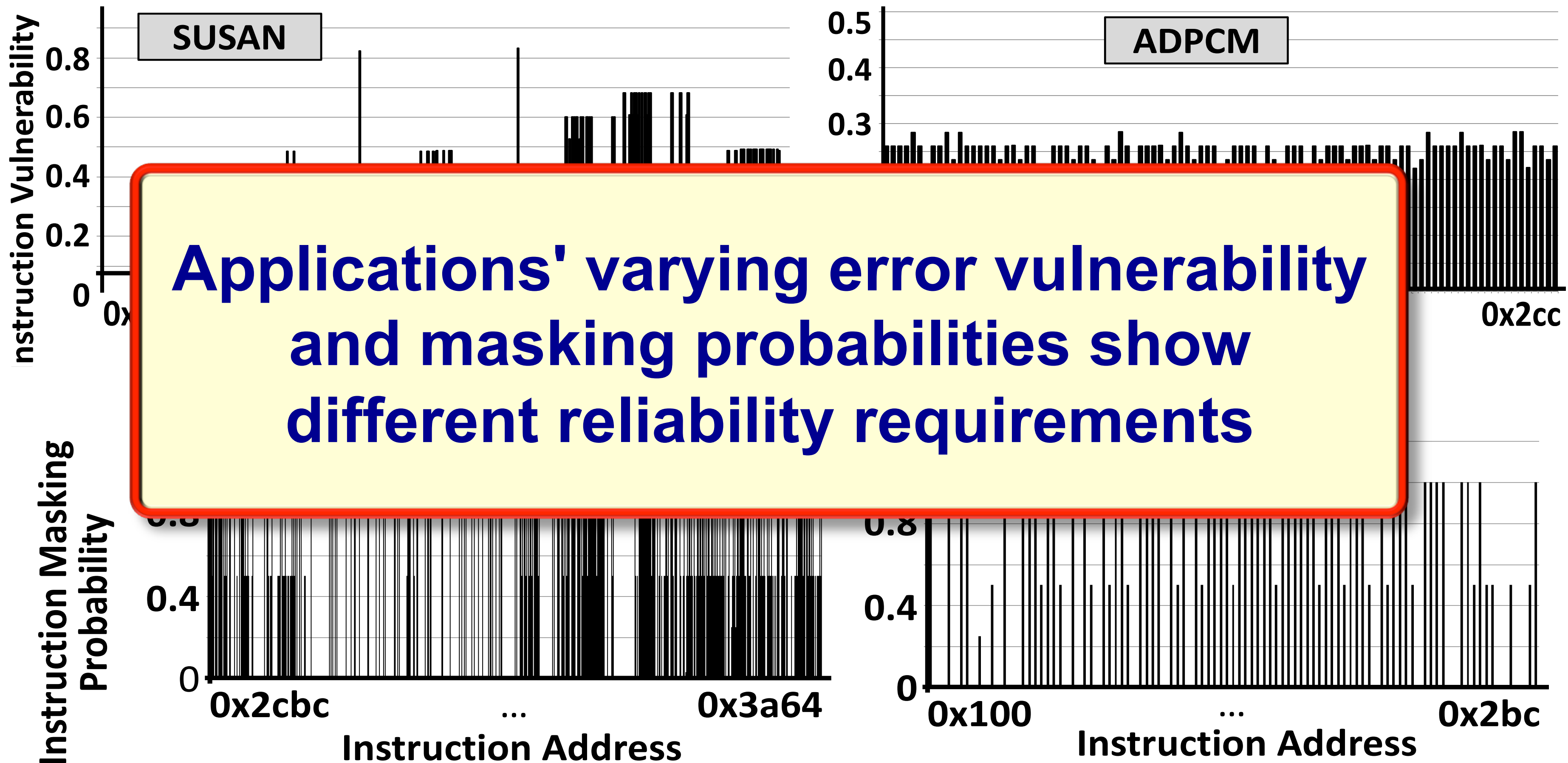
- **Spatial vulnerability**: probability of an error depending upon the area of specific processor resources used by the instructions
- **Temporal vulnerability**: probability of a fault depending upon the vulnerable periods of an instruction in a certain pipeline stage







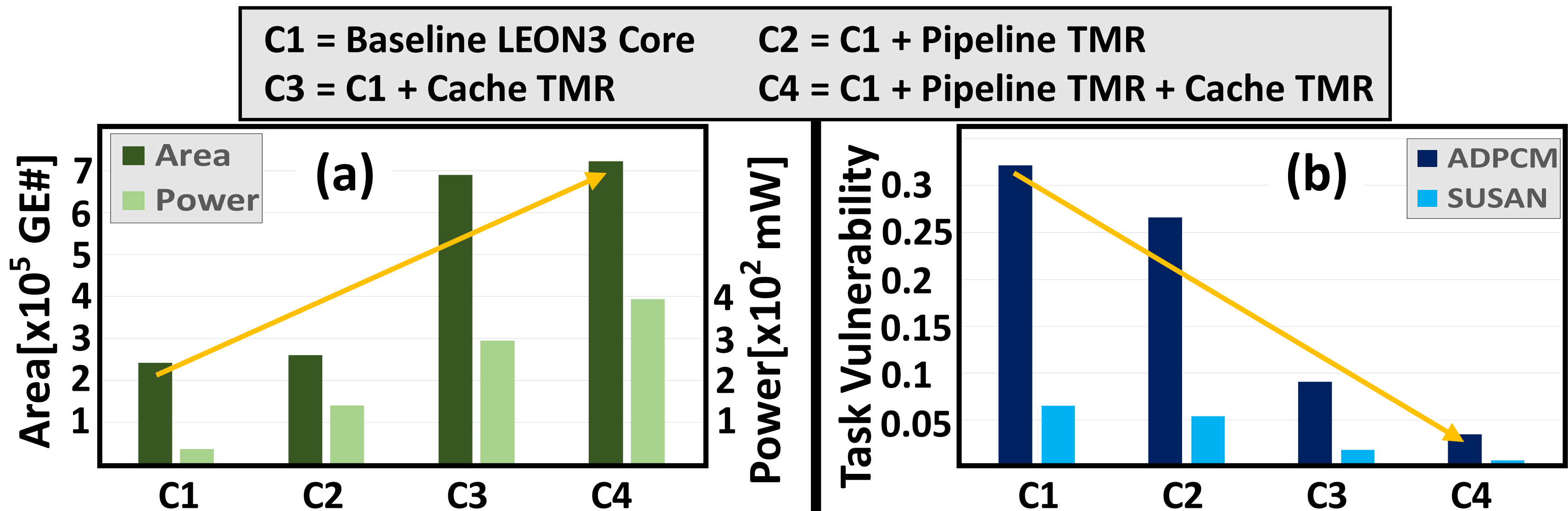
Motivation: Varying Instruction Vulnerability & Error Masking Properties



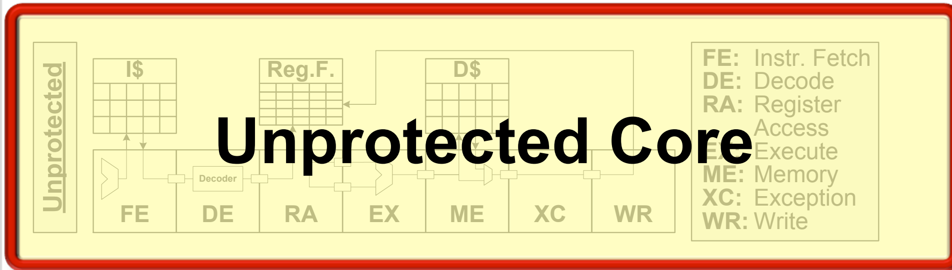
Applications' varying error vulnerability and masking probabilities show different reliability requirements

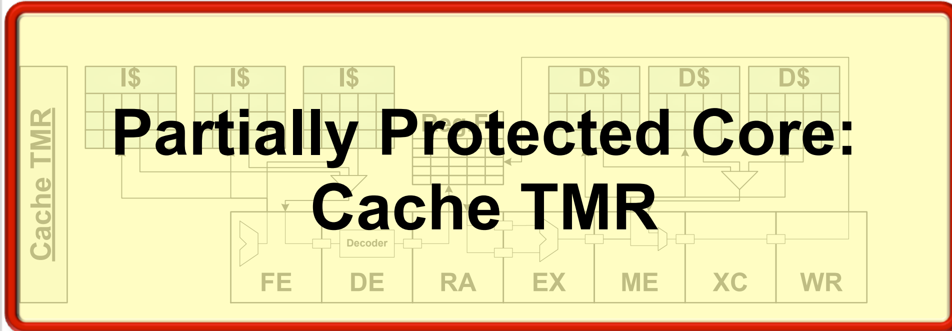
Turning Dark Silicon Problem into a Solution!

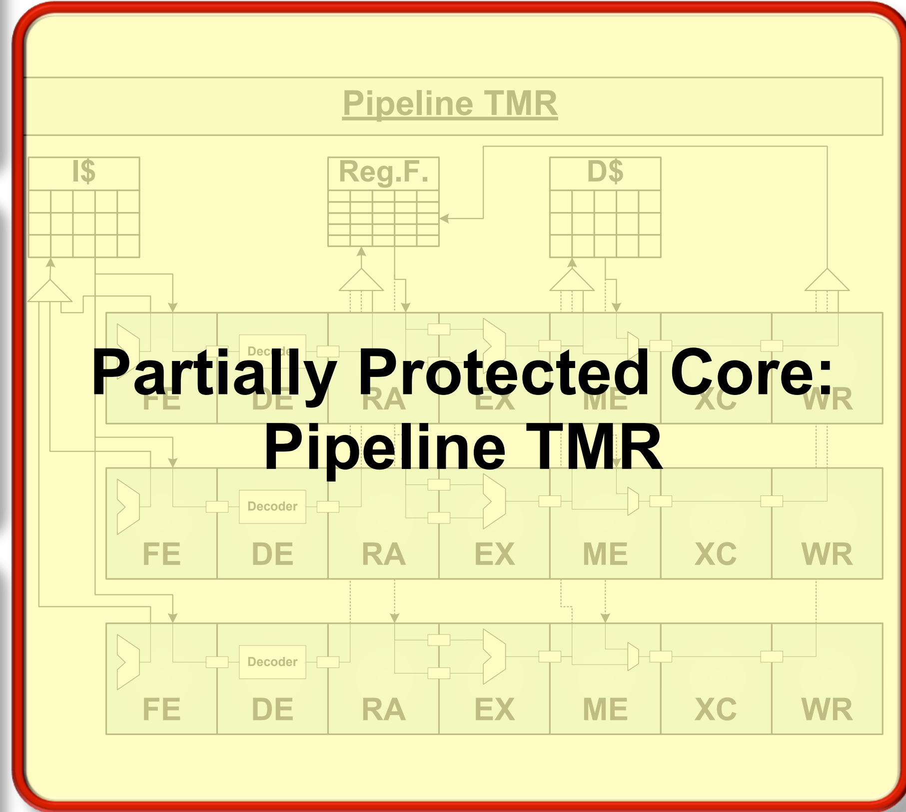
- Leverage available dark silicon chip with reliability-wise specialized cores offering distinct degree of reliability, i.e., protection against soft errors
  - Multiple "iso-ISA reliability-heterogeneous cores"
  - Higher protection against soft error => more power and area



Example: Reliability Heterogenous Cores



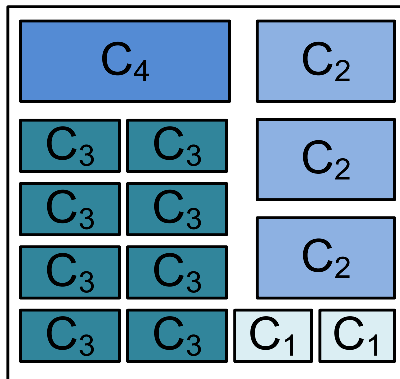


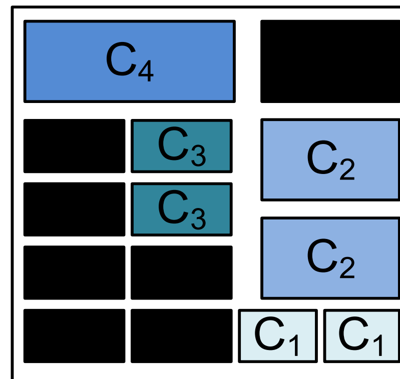


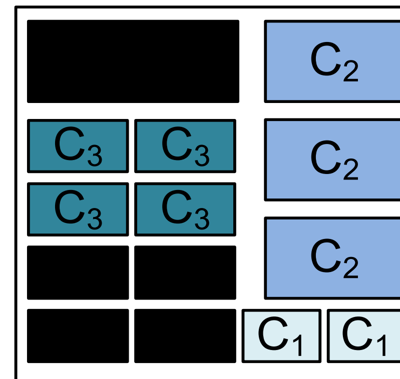
Turning Dark Silicon Problem into a Solution!

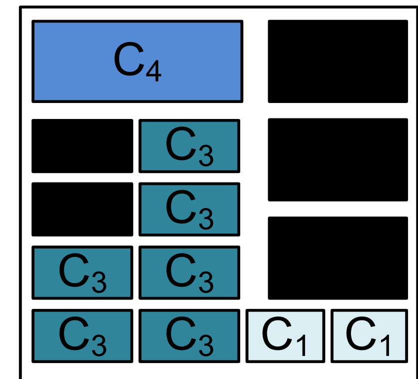
- Within the chip's TDP constraint, only a subset of cores can be powered-on at run-time and remaining cores stay dark

- A run-time system to manage reliability under thermal constraints.



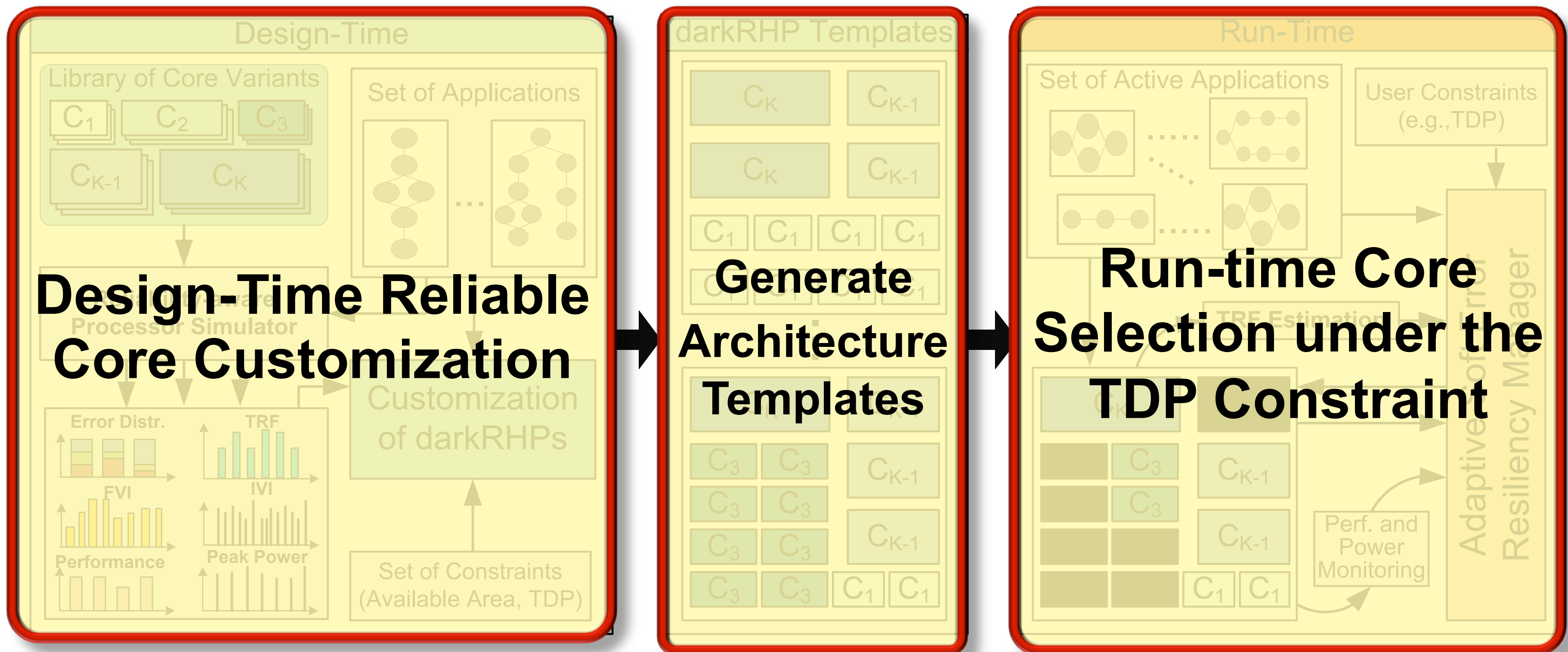






ASER: Adaptive Soft Error Resilience

- **Design-Time:** reliability-heterogeneous core customization
  - Formulated as the **Bounded Knapsack Problem**
- **Run-Time:** adaptive soft error resiliency manager allocates set of cores to concurrent applications under the given TDP constraint



Reliability Heterogenous Cores: Synthesis Results

	frequency = 250 MHz				frequency = 1 GHz			
	area[# of gate Eq.*10^5]	Power[mW]			area[# of gate Eq.*10^5]	Power[mW]		
		leakage	dynamic	total		leakage	dynamic	total
C1	**4,83**	**4,36**	**78,19**	**82,55**	**5,00**	**4,76**	**269,58**	**274,34**
C2	4,99	4,50	79,75	84,25	5,20	4,98	274,91	279,89
C3	13,62	12,26	223,39	235,65	14,26	13,83	767,73	781,56
C4	5,41	4,88	86,46	91,35	5,58	5,23	298,21	303,44
C5	13,77	12,40	224,96	237,36	14,46	14,08	773,52	787,60
C6	5,56	5,03	88,02	93,05	5,77	5,52	303,45	308,98
C7	14,19	12,79	231,73	244,51	14,94	14,35	796,26	810,61
C8	**14,35**	**12,93**	**233,30**	**246,23**	**15,02**	**14,56**	**801,79**	**816,34**

- **TSMC 45nm technology library**
- **Different process corners & frequencies**

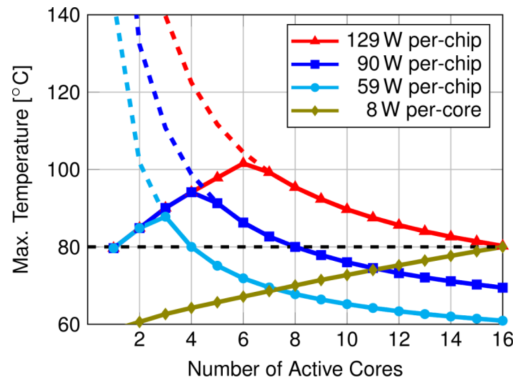
Reliability Savings are 20%-60% compared to state-of-the-art

C1	Baseline core
C2	Pipeline TMR
C3	Cache TMR
C4	Register File TMR
C5	Pipeline TMR + Cache TMR
C6	Pipeline TMR + Register File TMR
C7	Cache TMR + Register File TMR
C8	Pipeline TMR + Cache TMR + Register File TMR

Mitigating Dark Silicon

Thermal Safe Power (TSP)

(Abstract from temperature using efficient power budgets)



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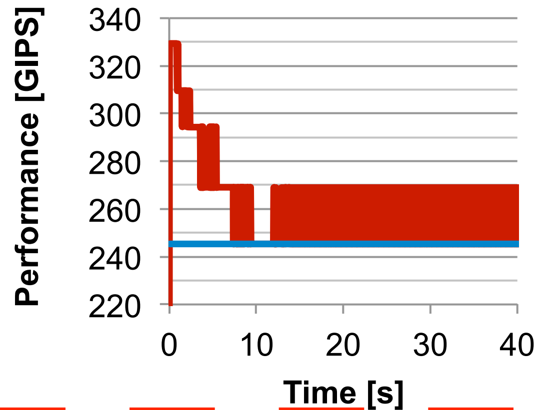
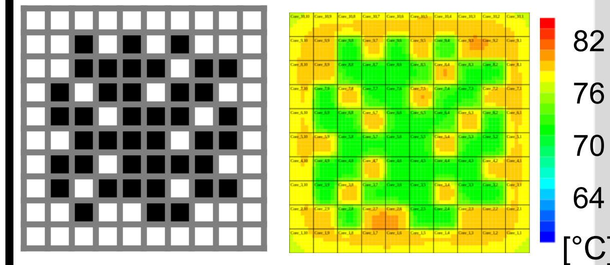
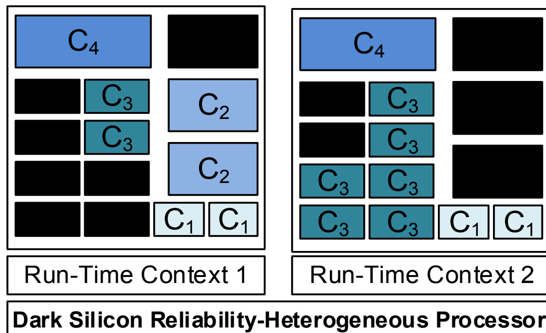


Dark Silicon Management

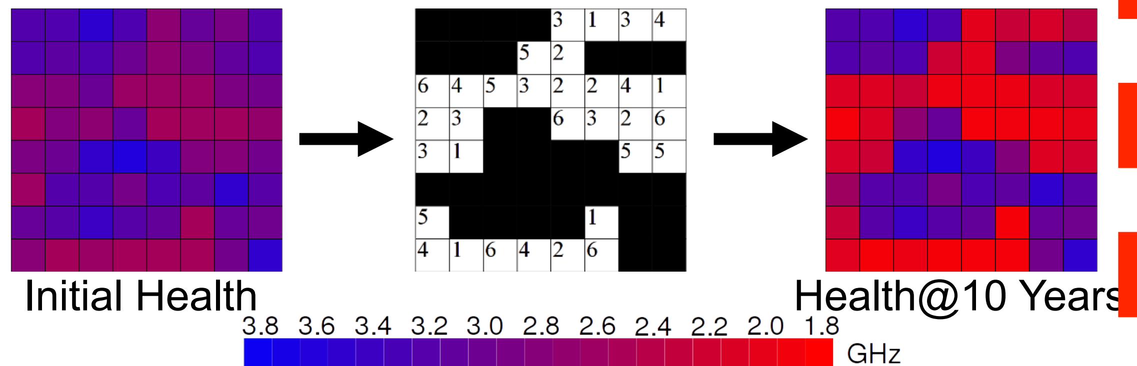
(Patterning and Resource Management)



Dark Silicon-Aware Soft Error Tolerance

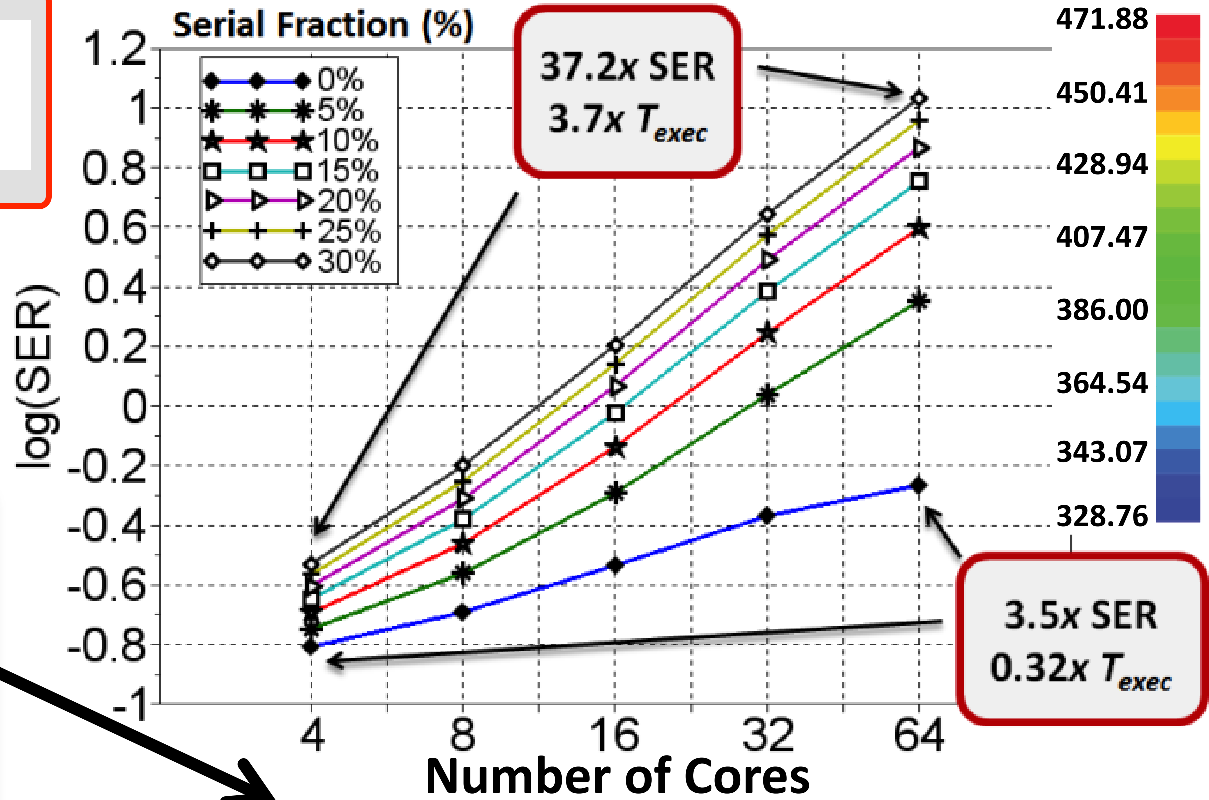


Dark Silicon-Aware Aging Optimization

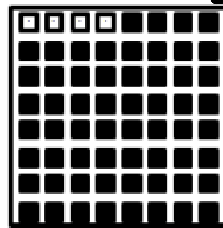


Reliability: trade-off aging <-> SER

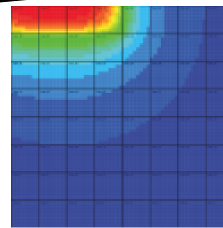
$$T_{exec} = \frac{T_{serial}}{f} + \frac{T_{par}}{f \times N_{cores}}$$



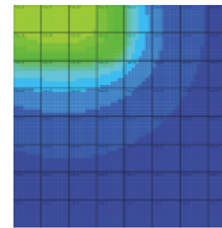
Low Soft Error Rate but High Temperature that accelerates Aging



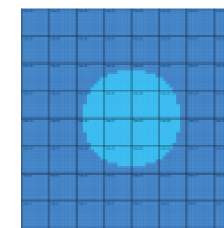
TL-4 Cores



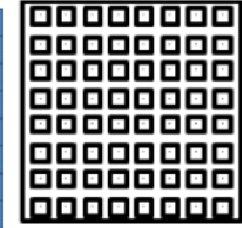
TL-4 Cores



TL-8 Cores



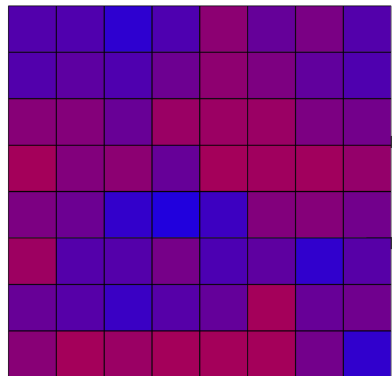
All-64 Cores



All-64 Cores

Hayat: Harnessing Dark Silicon and Variability for Aging Optimization

Initial Health Under Process Variation

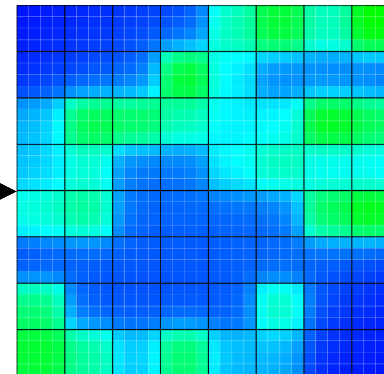


f_{avg} = 3.01 GHz

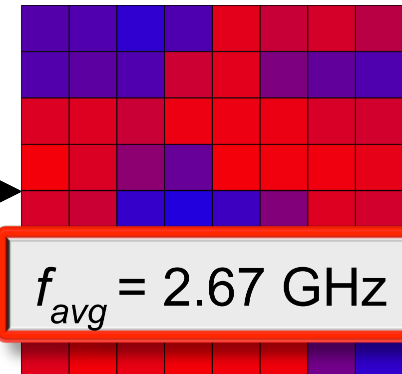
Initial Task Pattern, DTM at run-time

				3	1	3	4
			5	2			
6	4	5	3	2	2	4	1
2	3			6	3	2	6
3	1					5	5
5					1		
4	1	6	4	2	6		

Steady-State Temperature

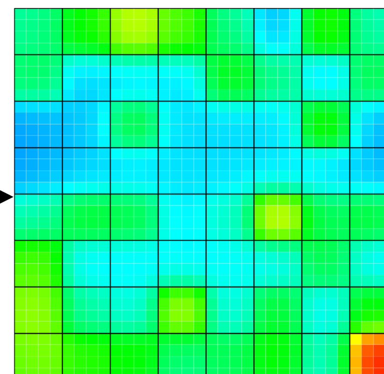


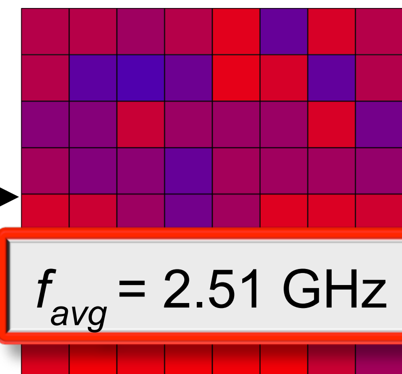
Health after 10 Years



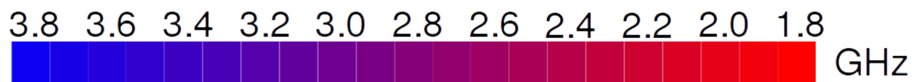
f_{avg} = 2.67 GHz

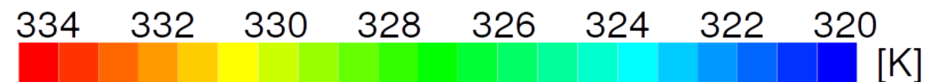
2	3	6	2	6	4	2	3
1	2	6	2	4	2	5	1
4	1	4	1	3	3	6	3
5	5	5	6	3	5	4	1





f_{avg} = 2.51 GHz





Conclusions

- "Dark Silicon" is a problem triggered through high power density => hardware is operated at thermal limits
  - Temperature decreases reliability

- "Dark Silicon" can be minimized/exploited through:
  - Efficient dark silicon management under peak power and thermal constraints
  - New thermal safe power budgets
  - Scalable power and thermal management
  - Increasing different forms of heterogeneities: functional, power, reliability, etc.
  - Increasing reliability
  - …

- Power/energy efficiency and reliability should jointly be optimized at multiple HW and SW layers of the system stack

If all this is considered, good chance there is no Dark Silicon problem at all!

Some of our recent publication on Dark Silicon

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- Hussam Amrouch, Victor van Santen, Thomas Ebi, Volker Wenzel, Jörg Henkel, "Towards Interdependencies of Aging Mechanisms", IEEE/ACM Int'l Conference on CAD (**ICCAD**), 2014.
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