Particularly in the last decade, Deep Neural Networks (DNNs) have shown outstanding improvements in machine learning. These improvements have allowed them to be used in various applications such as natural speech recognition, pattern recognition, etc. As the number of DNN application domains grows, there is a need for efficient DNN implementations, so that with reasonable effort, good outcomes may be achieved.

There is a large design space when it comes to mapping DNNs to a particular architectural hardware platform like FPGAs and others, as far as design techniques are concerned. Finding an optimal or near-optimal design point requires a systematic design-space exploration (DSE) process.

This project aims to explore the architectural design space of mapping DNNs onto FPGA platforms, leveraging techniques such as systematic DSE and evolutionary algorithms. Depending on your interest and depending on whether it is a BA or MA, the tasks could include but are not limited to:

- Evaluate existing DSE Frameworks
- Enumerate and explore the Architectural Design Space

- Explore Evolutionary Algorithms for DSE
- Deploy Neural Networks to FPGAs

Skills required/beneficial for the thesis

- Programming skills (C/C++, Python)
- Background in deep neural networks
- For topics regarding hardware implementations on FPGAs, background in VHDL/Verilog or FPGAs is beneficial

Skills acquired within the thesis

- Apply your programming experience to research
- Gain practical insight in DNN implementations, accelerators for DNNs, data-locality challenges when mapping DNNs to accelerators, FPGA-implementations for DNNs, design-space alternatives, and/or algorithms and tools for automatic DSE

Language

- The collaboration with colleagues can be in English.

Contact

- Zeynep Gübeyaz Demirdag: zeynep.demirdag@kit.edu
- Lars Bauer: lars.bauer@kit.edu