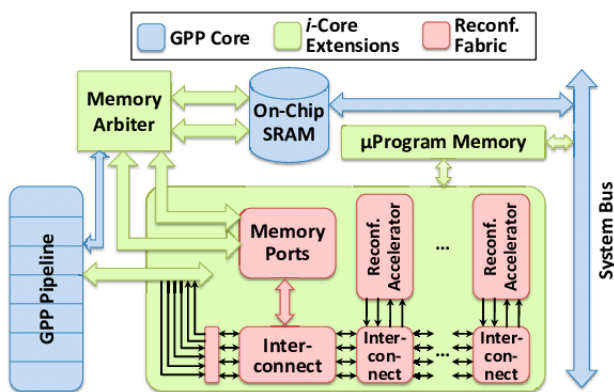


# Chair for Embedded Systems

Prof. Dr. J. Henkel

## Multiple Bachelor/Master Theses Dynamic Execution of Accelerators for a Run-Time Reconfigurable Processor



The *i-Core* is a run-time adaptive reconfigurable processor. It has *containers* that can be reconfigured (like in FPGAs) and that are used to load hardware accelerators at runtime, i.e. while the application is running. These accelerators are used to execute so-called Special Instructions (SIs). The SIs improve the overall execution time of the processor.

Several SIs are already developed for the *i-Core*. Some of the SIs deal with accelerating the execution of complex floating-point algorithms. These algorithms include object detection or water bodies flow prediction.

The SIs previously required a predetermined static control-flow. Recently, we implemented support for dynamic control-flow for the *i-Core* SIs. This flyer advertises multiple theses. The main goals are to use this dynamic control-flow for the above-mentioned SIs and to develop new SIs and automatic test for new/existing SIs.

### Possible Tasks for the Student

Tasks will vary according to whether it is a bachelor or master thesis. Mainly hardware development will be performed. However, software development is also possible. The tasks could include but are not limited to:

- Testing and evaluating the existing SIs
- Extending the developed SIs with dynamic execution
- Automated scheduling of the SIs
- Developing new SIs that benefit of dynamic execution, e.g.
  - Machine Learning SIs
  - Encryption and security SIs

### Skills beneficial for the thesis

- Programming Skills (C, C++, Python)
- Knowledge of VHDL
- Background on Processor Architecture and/or reconfigurable computing (FPGAs)

### Skills acquired with the Thesis

- Work in a research environment
- Technical writing skills
- In depth knowledge of adaptive reconfigurable processors

### Contact

• Hassan Nassar, M.Sc., [hassan.nassar@kit.edu](mailto:hassan.nassar@kit.edu)  
<http://ces.itec.kit.edu/~nassar>

• Dr.-Ing. Lars Bauer, [lars.bauer@kit.edu](mailto:lars.bauer@kit.edu)  
<http://ces.itec.kit.edu/~bauer>