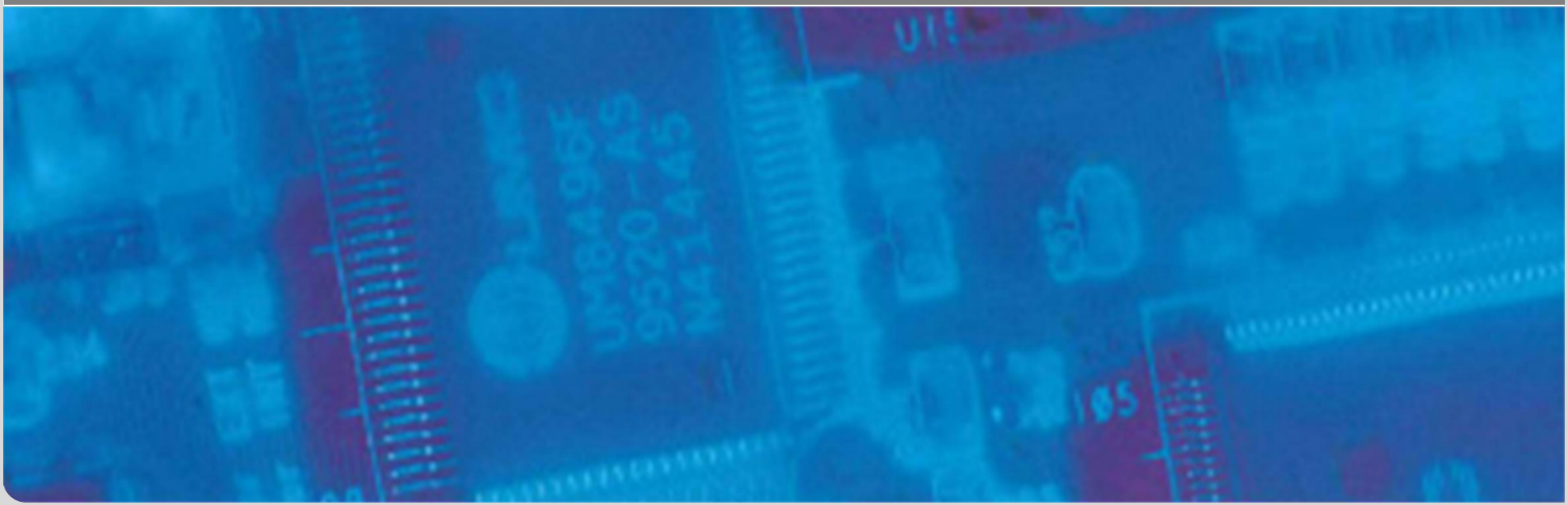
Karlsruhe Institute of Technology

TSP: Thermal Safe Power - Efficient Power Budgeting for Many-Core Systems in Dark Silicon

S. Pagani, H. Khdr, W. Munawar, J.-J. Chen, M. Shafique, M. Li, and J. Henkel

CHAIR FOR EMBEDDED SYSTEMS (CES)



Outline

- Introduction and State-of-the-art
- Motivation
- Objective and Contributions
- System Model
- Thermal Safe Power (TSP)
  - For Given Mappings
  - For the Worst-Case Mappings
- Evaluations
- Conclusions

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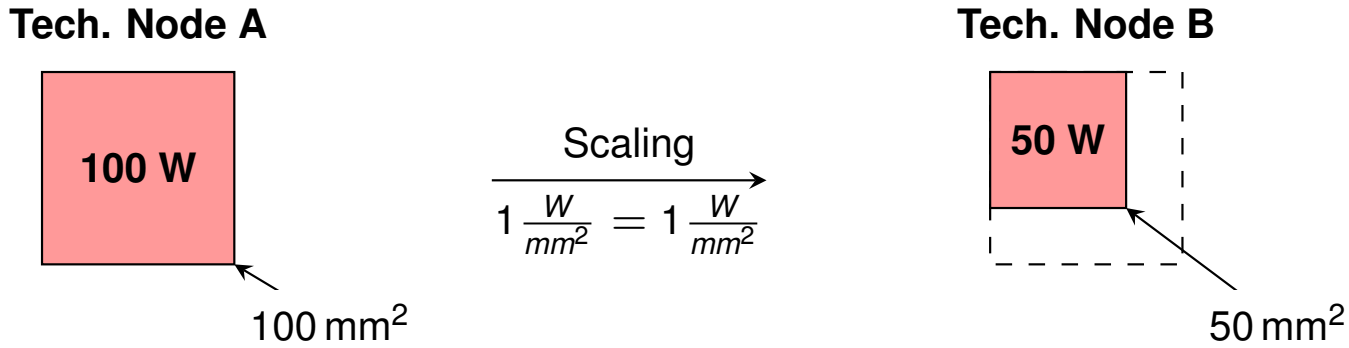
Dark Silicon:

- Up to now: Constant power density between technology nodes.



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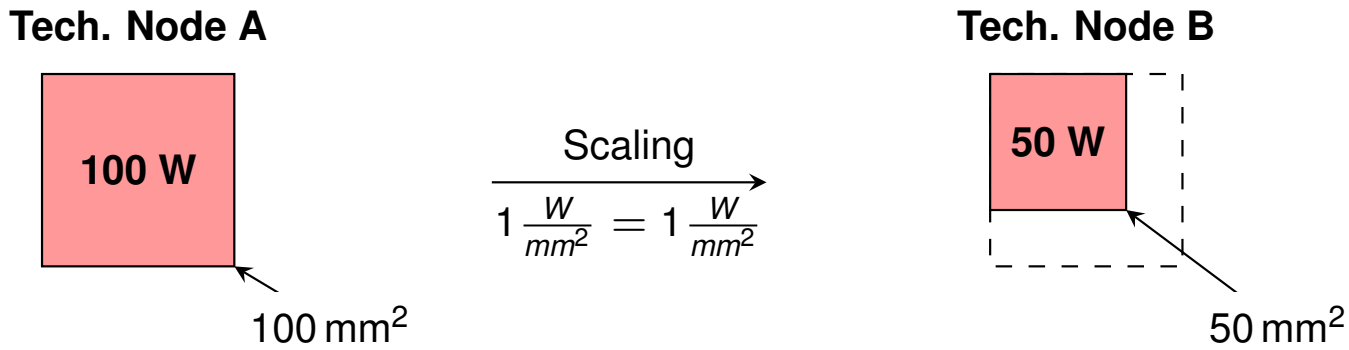

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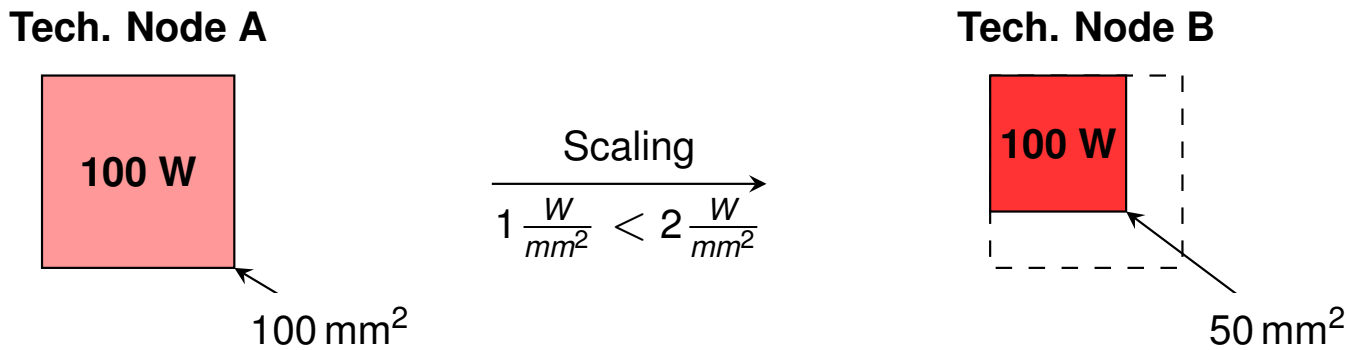

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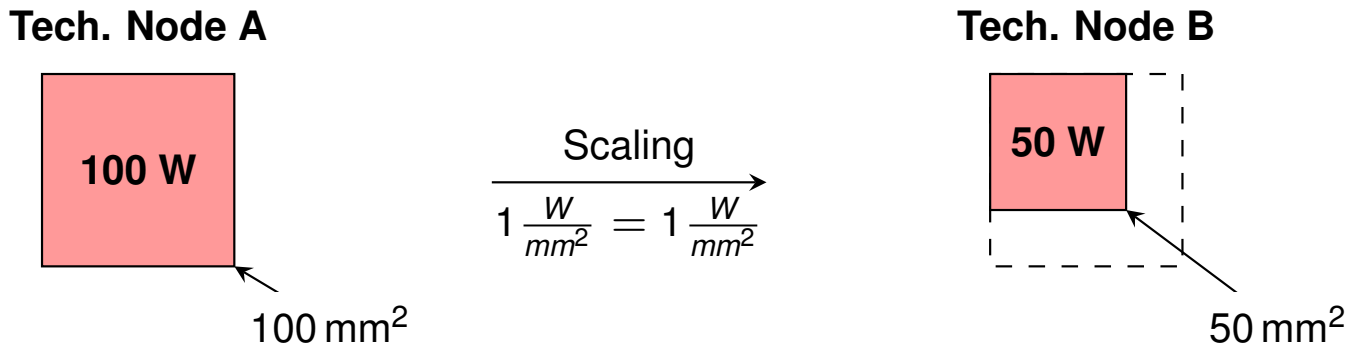

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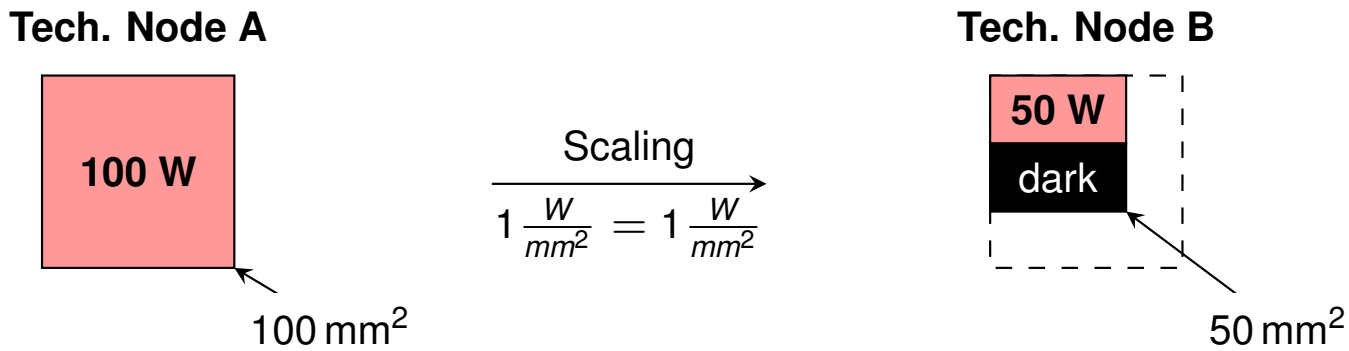


Introduction

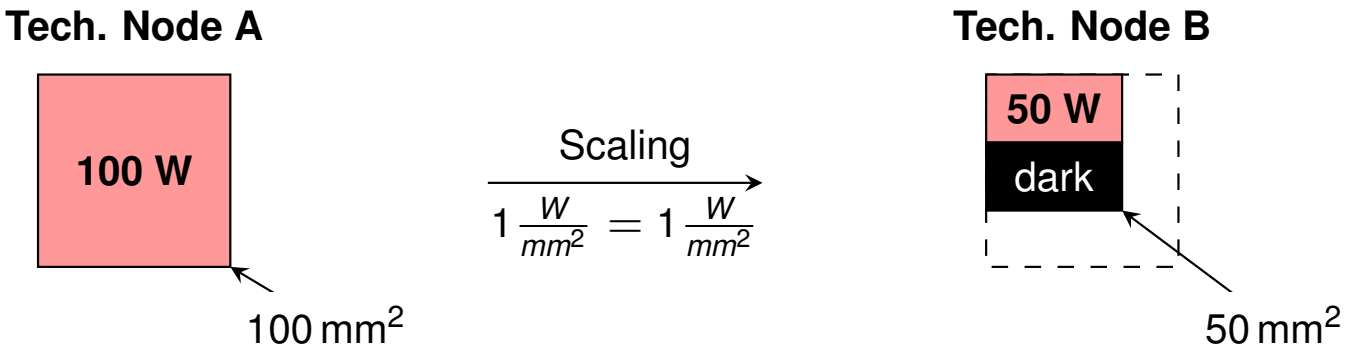
Dark Silicon:

- Up to now: Constant power density between technology nodes.

Dark silicon motivates:

- Very efficient power budgets.

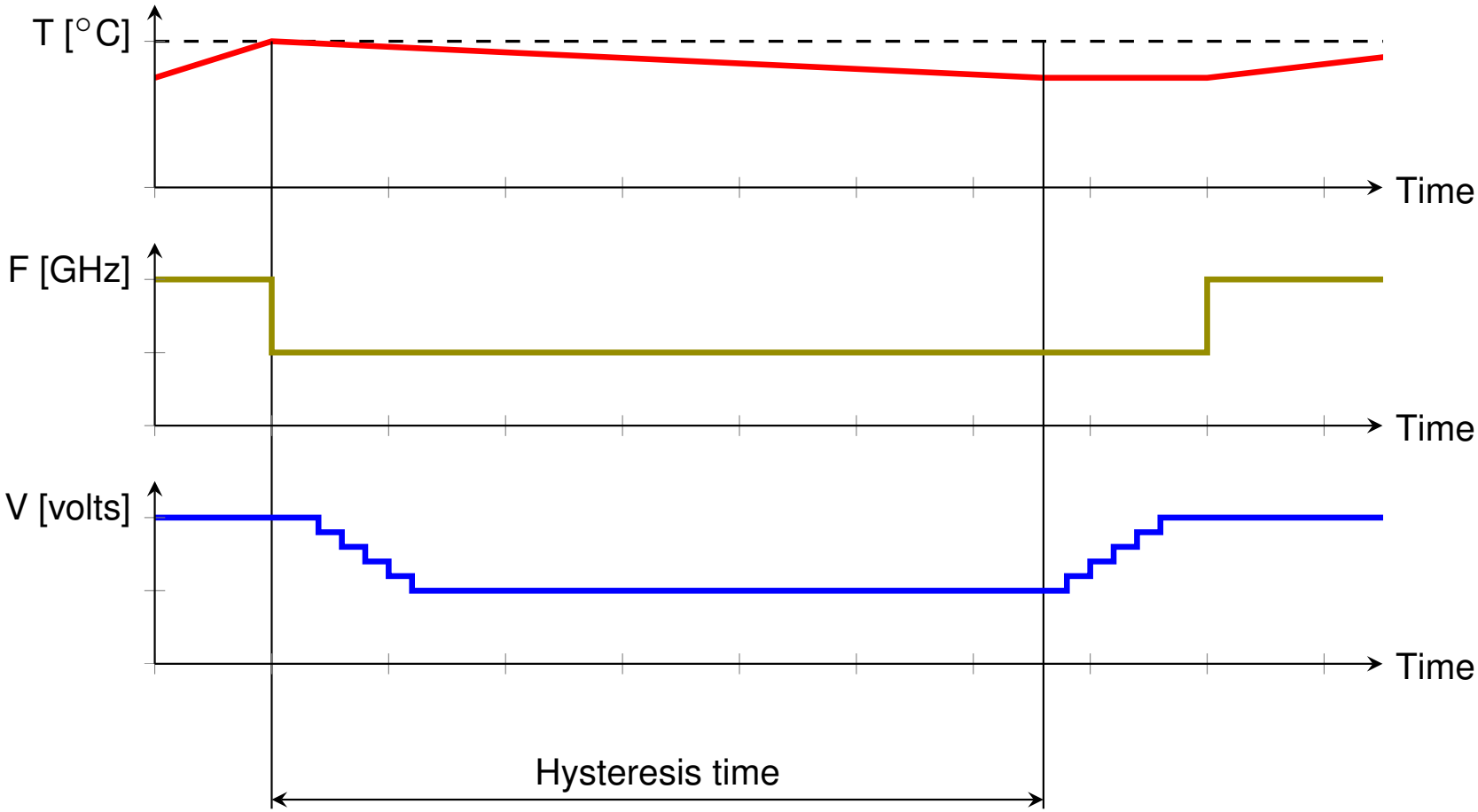
- Expected: Power density doubles between technology nodes.



Introduction

Dynamic Thermal Management (DTM):

- Avoids possible overheating of the chip.



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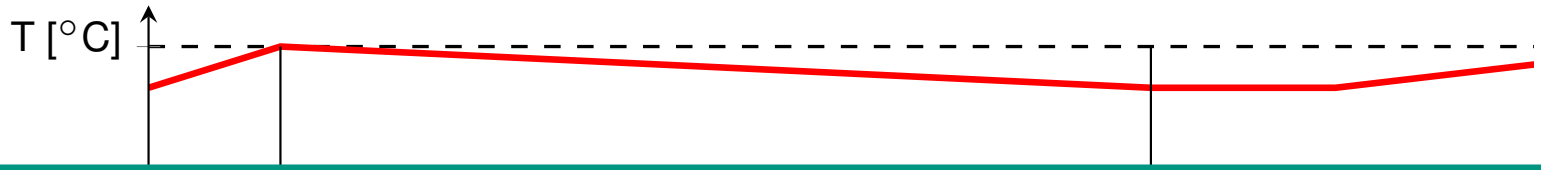
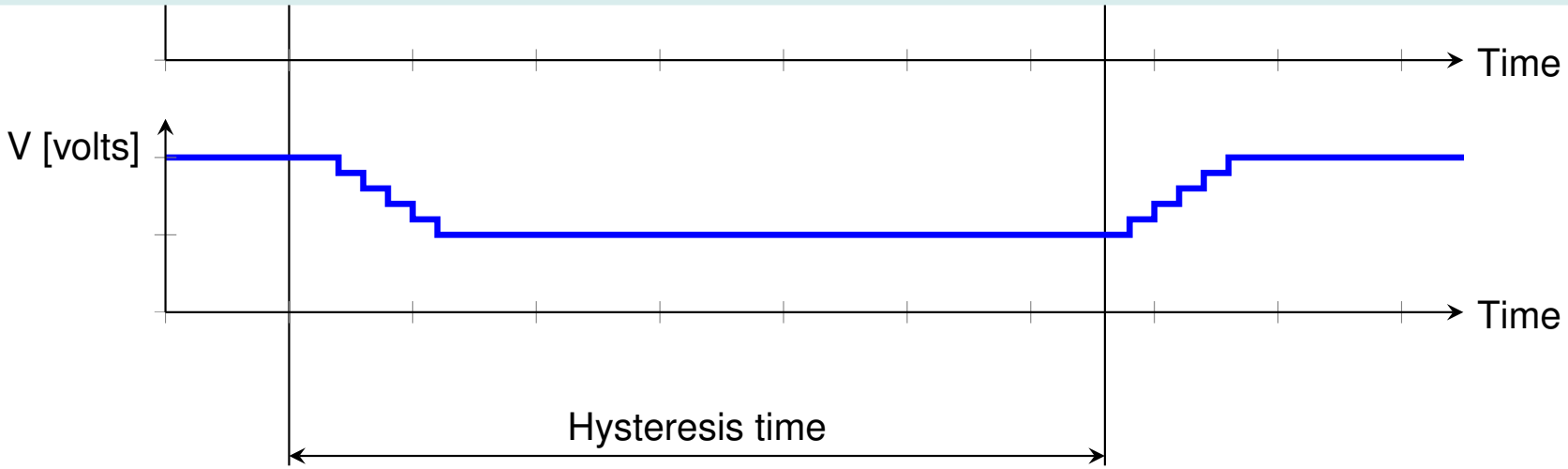


DTM activation:

- Frequent triggers of aggressive DTM → Decrease the performance.



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Thermal Design Power (TDP):

- Highest expected power for power intensive applications.
- The chip can consume more power than TDP.
- Should be safe to run the system at TDP.
- Manufacturers recommend to design the cooling solution for TDP.

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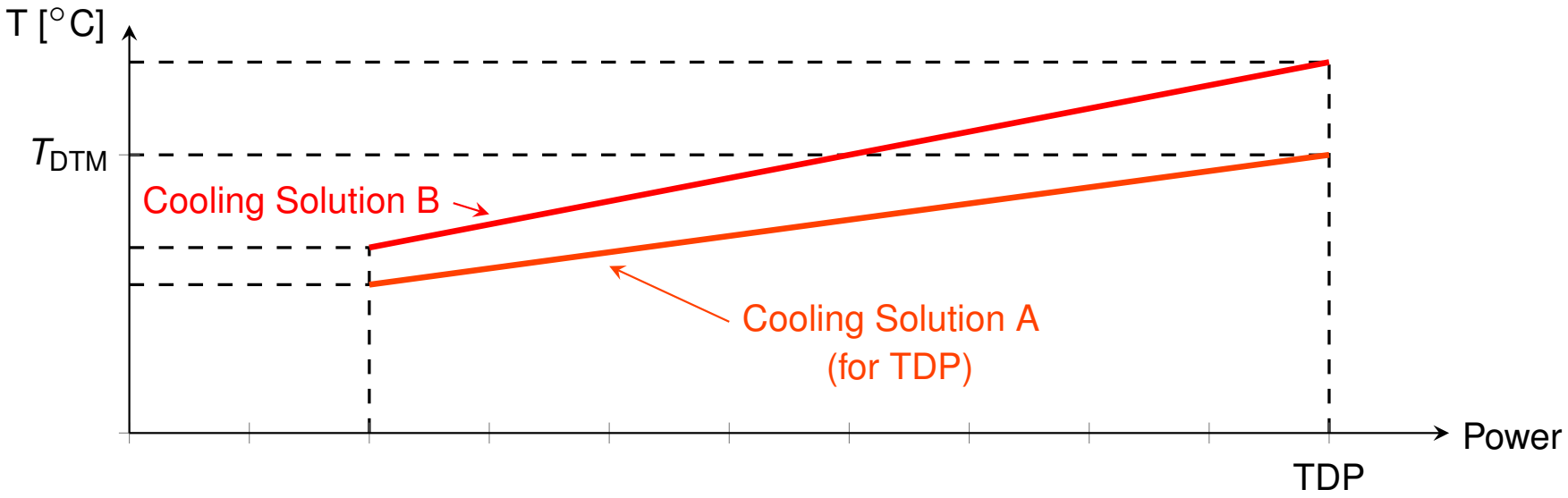

State-of-the-art

Power Budget / Power Constraint:

- Abstraction: Not deal directly with temperature.
  - Thermal models of applications depend on ***neighbouring*** cores.
  - Leakage power depends on the core's ***own*** temperature.

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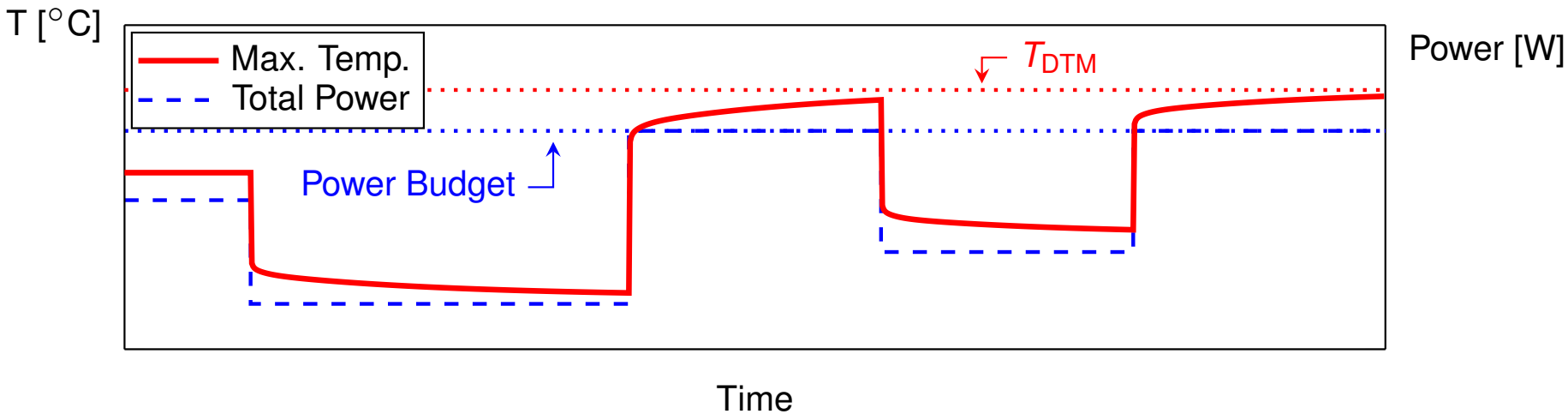
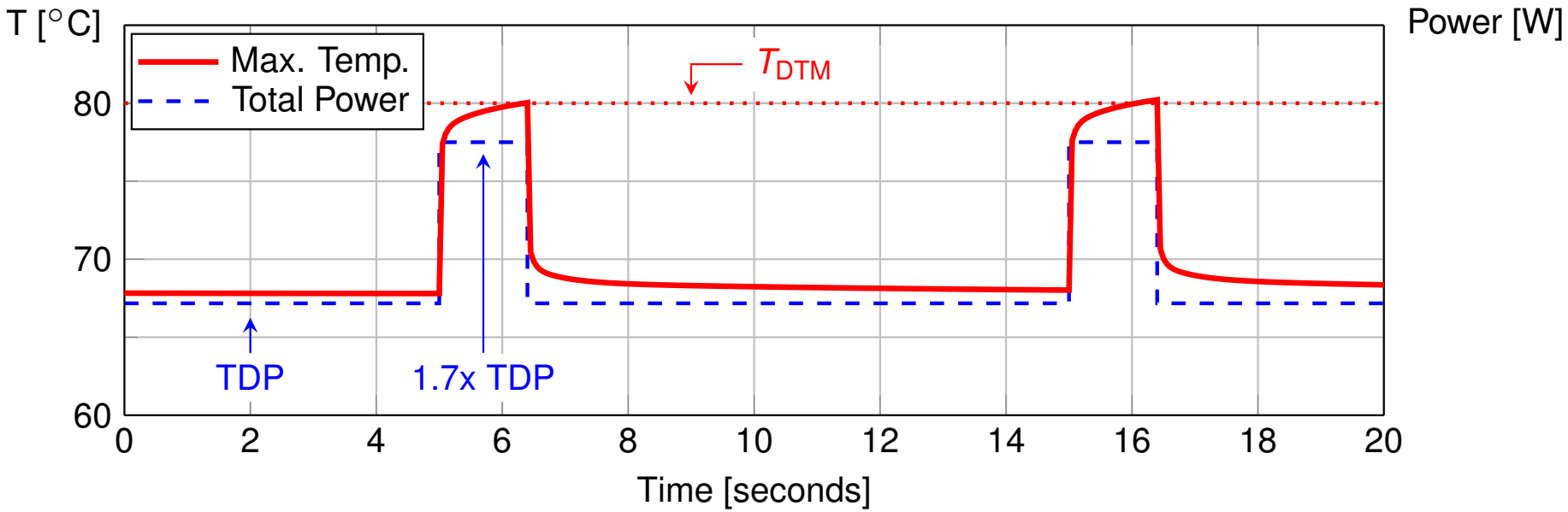
- Abstraction: Not deal directly with temperature.
  - Thermal models of applications depend on ***neighbouring*** cores.
  - Leakage power depends on the core's ***own*** temperature.
- Generally, a power budget is a ***single*** and ***constant*** value:
  - For each core (per-core).
  - For the entire chip (per-chip), e.g., TDP.



State-of-the-art

Boosting Techniques:

- Allow power levels above the budget for ***short time intervals***.
- For example:
  - Intel's Turbo Boost.
  - AMD's Turbo CORE.



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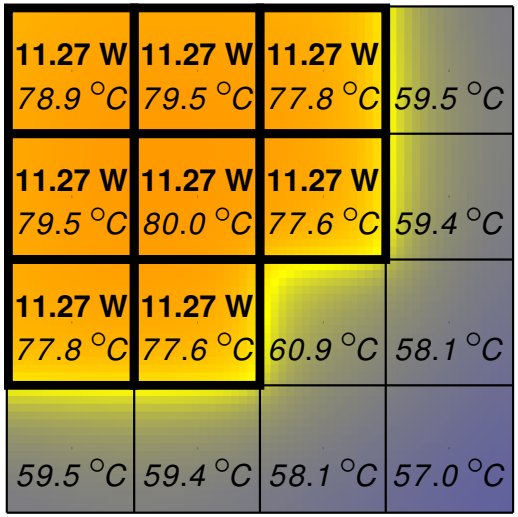
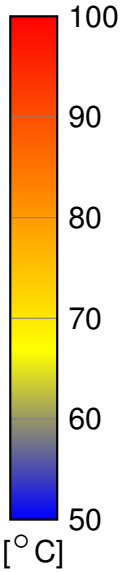
- Power budget: 90 W.



Highest Temperature: 80.0°C

(a) 8 active cores



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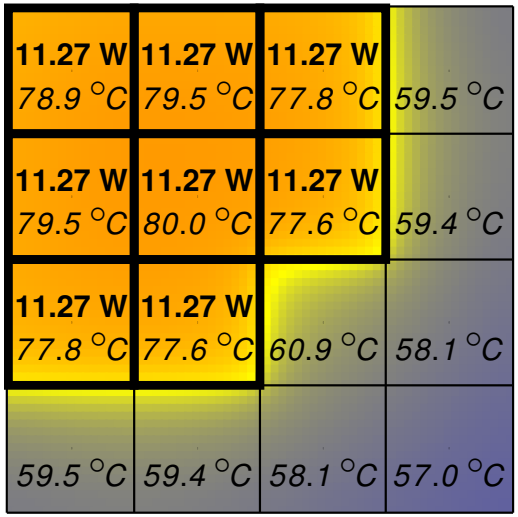

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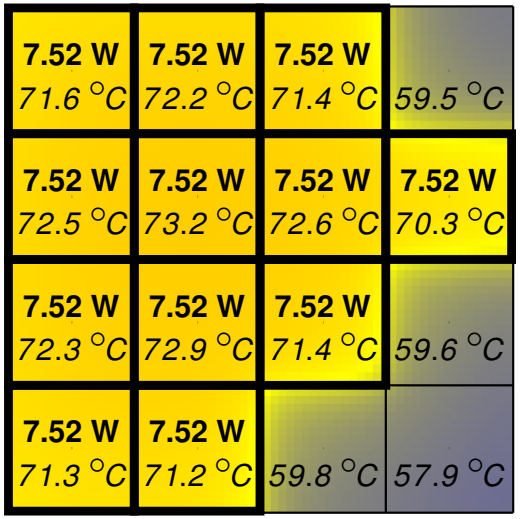
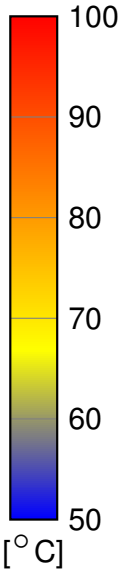


Highest Temperature: 73.2°C

(b) 12 active cores



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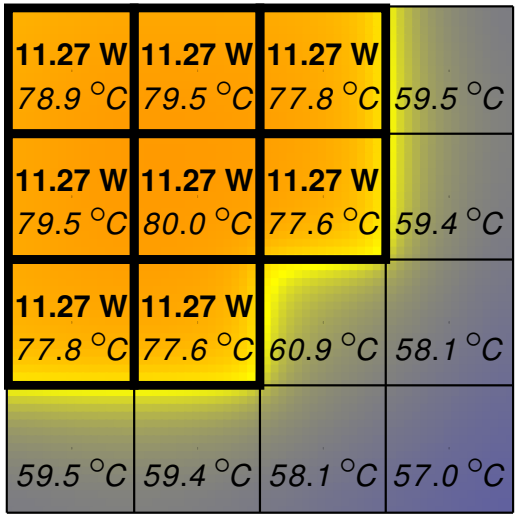

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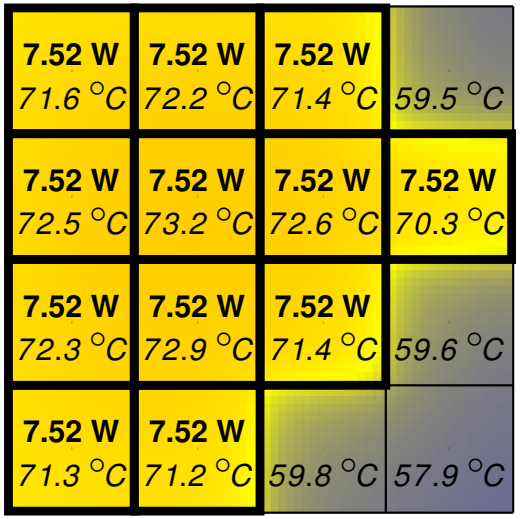

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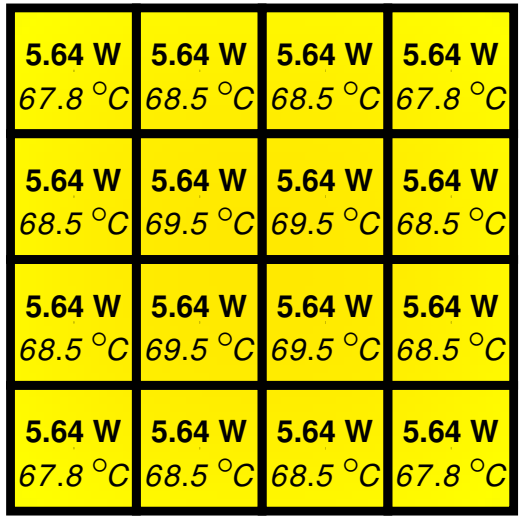
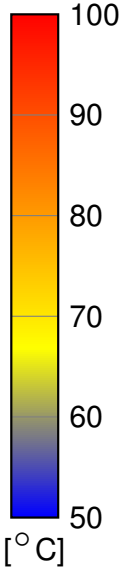


Highest Temperature: 69.5°C

(c) 16 active cores



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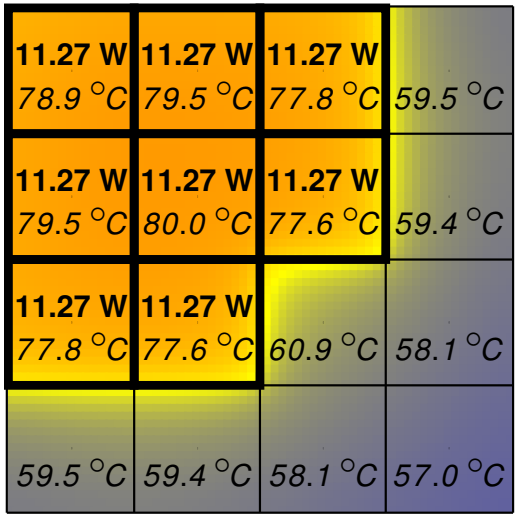

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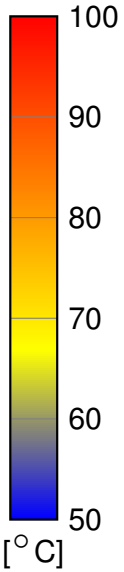

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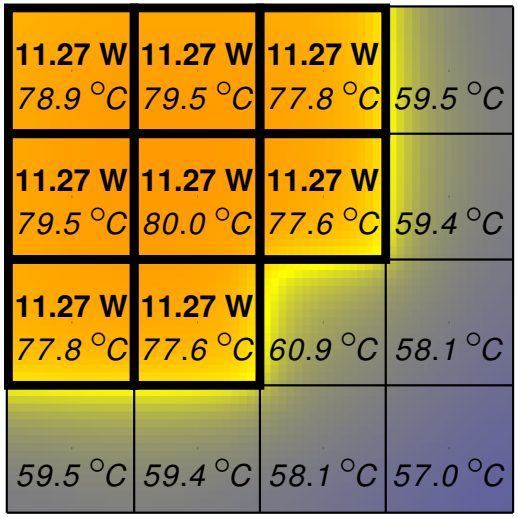

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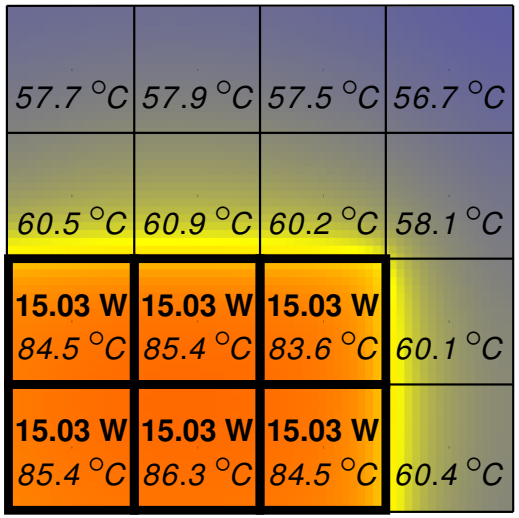
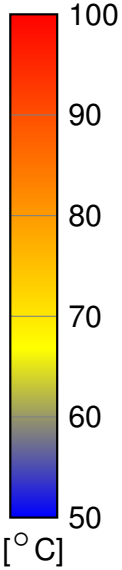


Highest Temperature: 86.3°C

(b) 6 active cores



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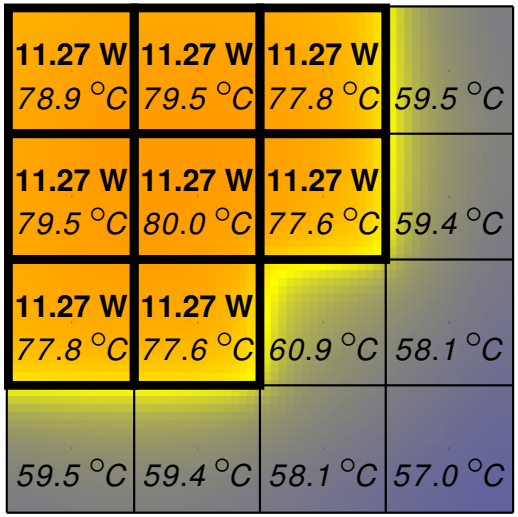

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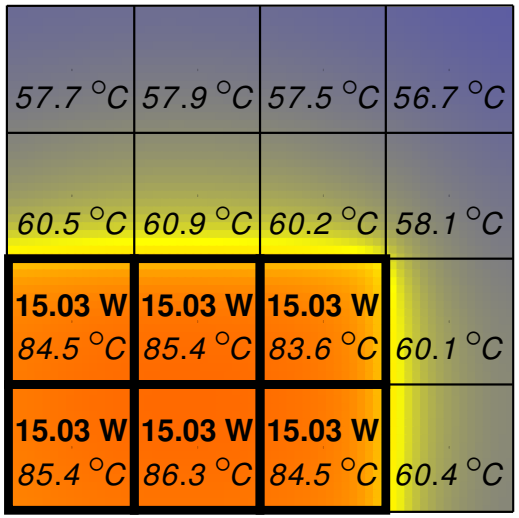

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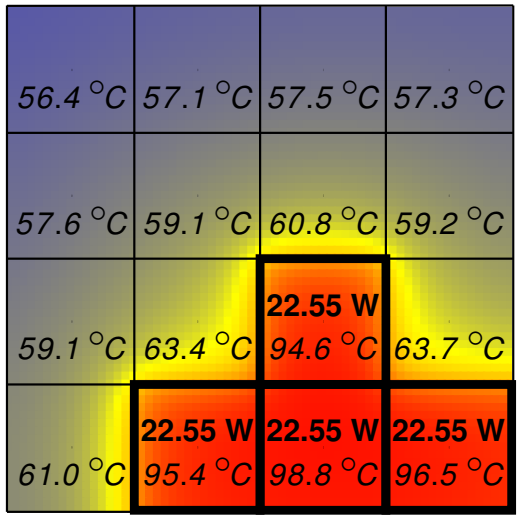
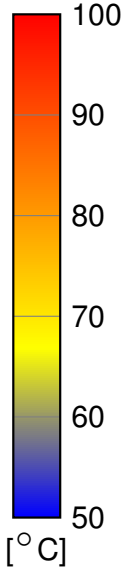


Highest Temperature: 98.8°C

(c) 4 active cores



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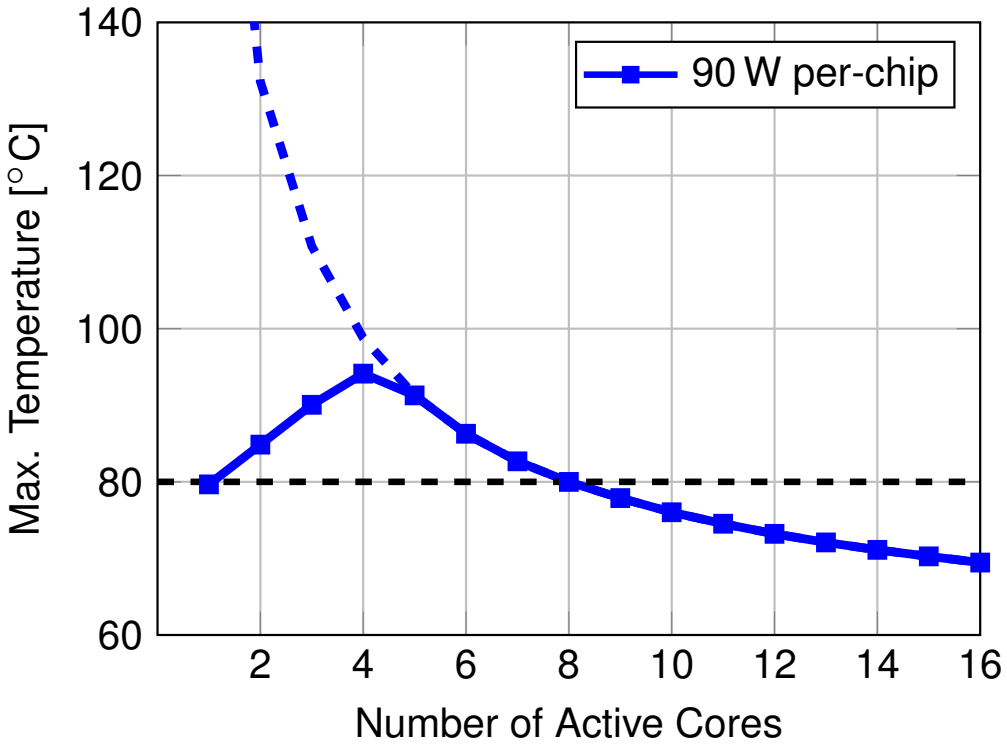

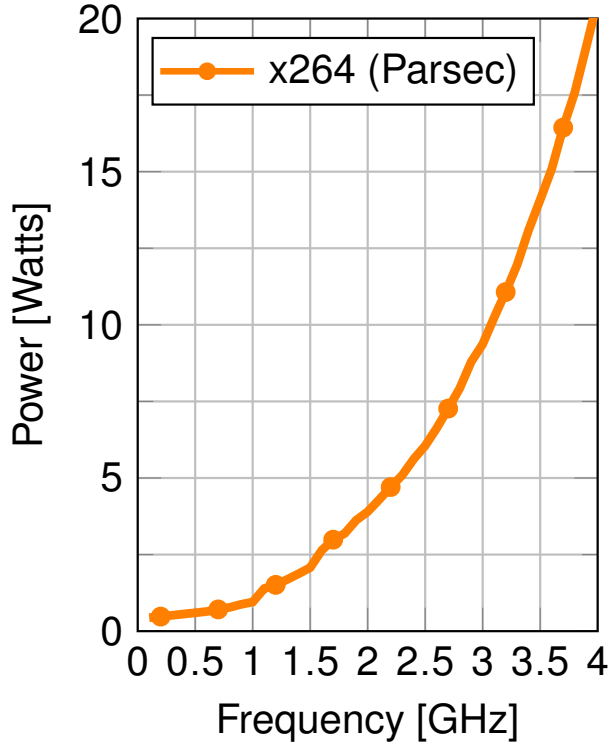

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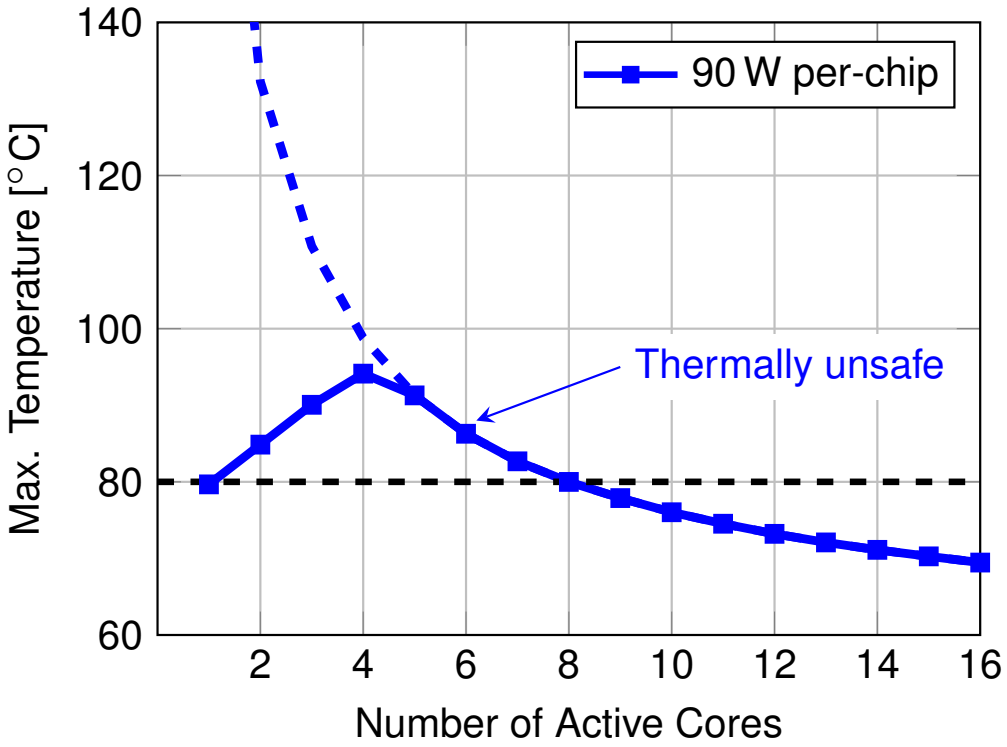

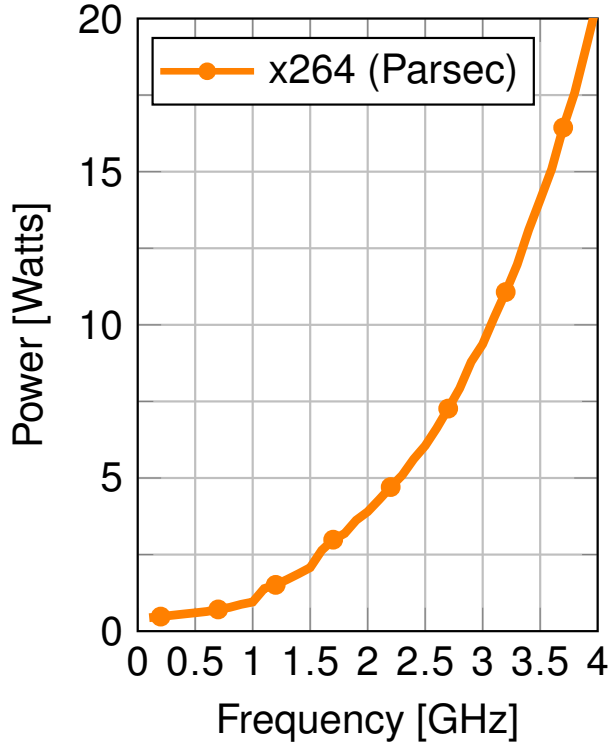

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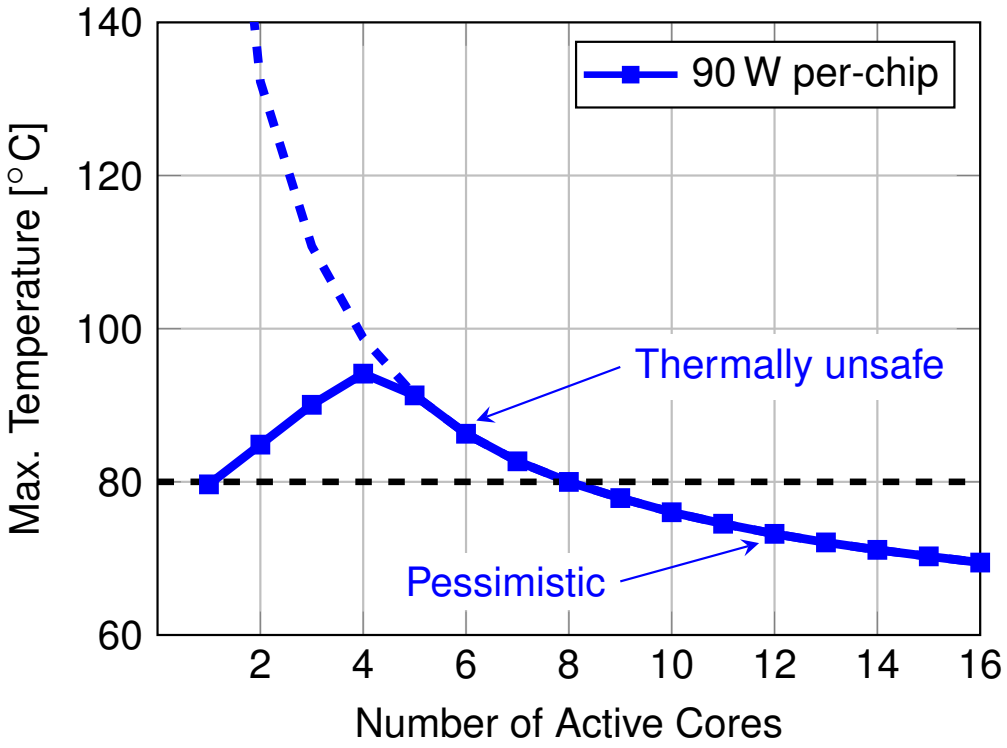

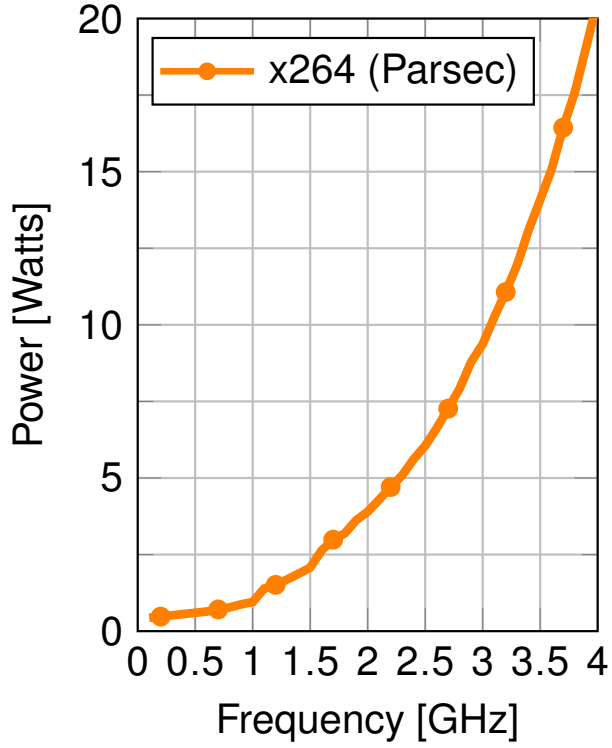

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- 16 cores with area 5.3 mm^2.
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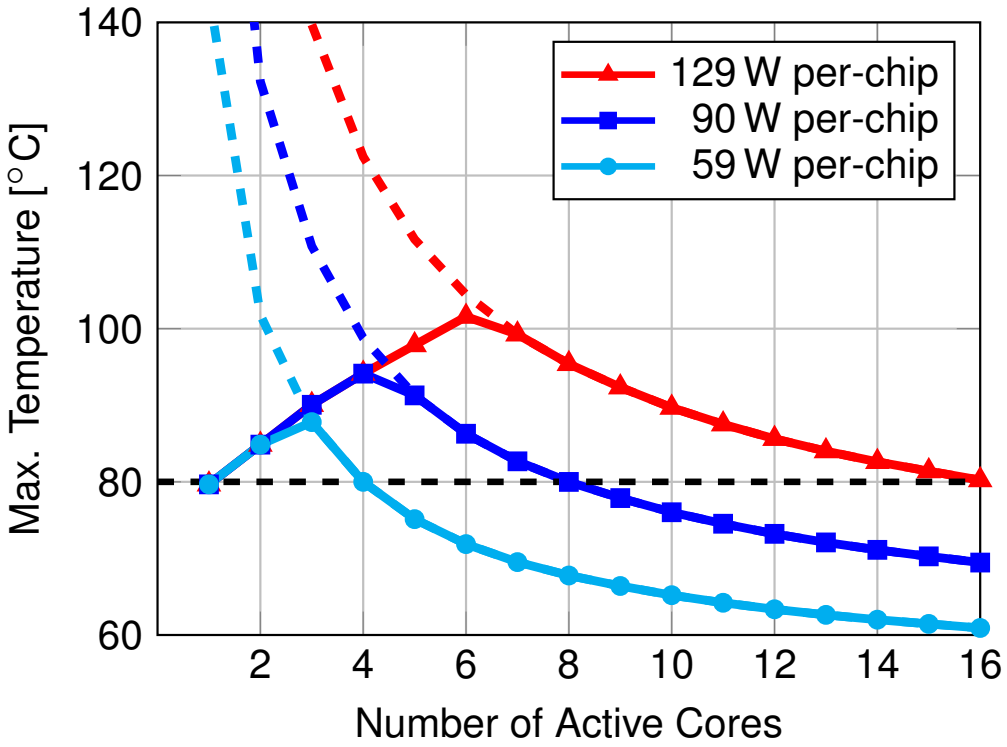
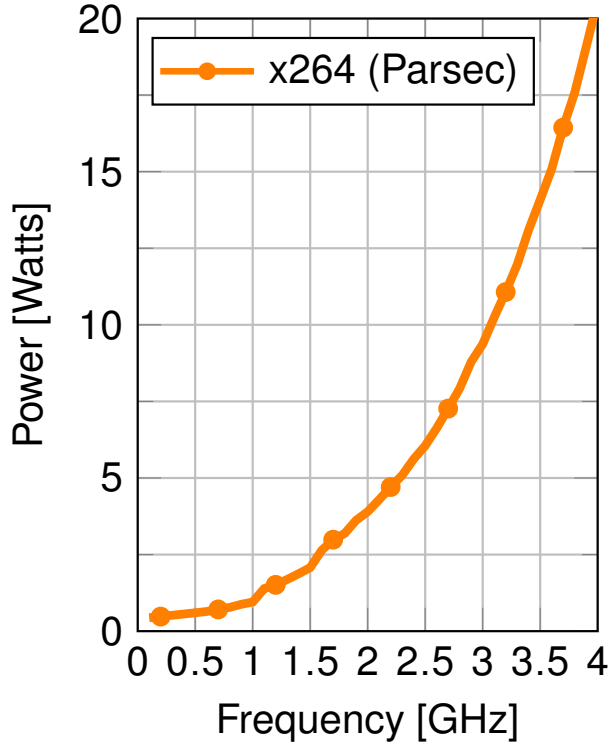
- Budgets: 129 W, 90 W, and 59 W per-chip.





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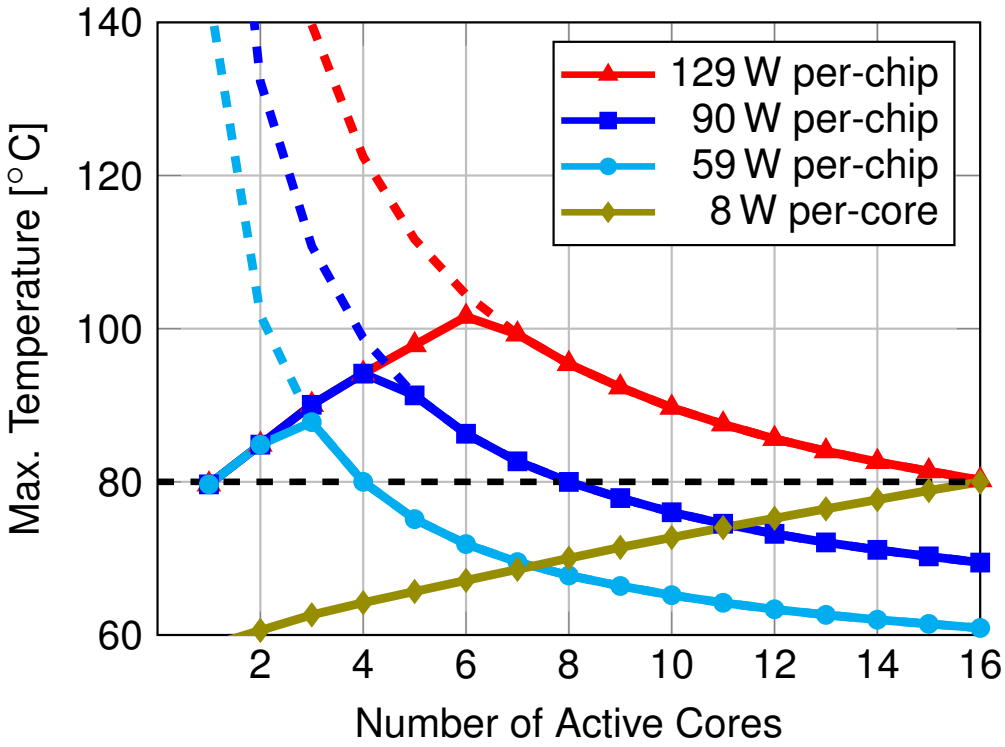

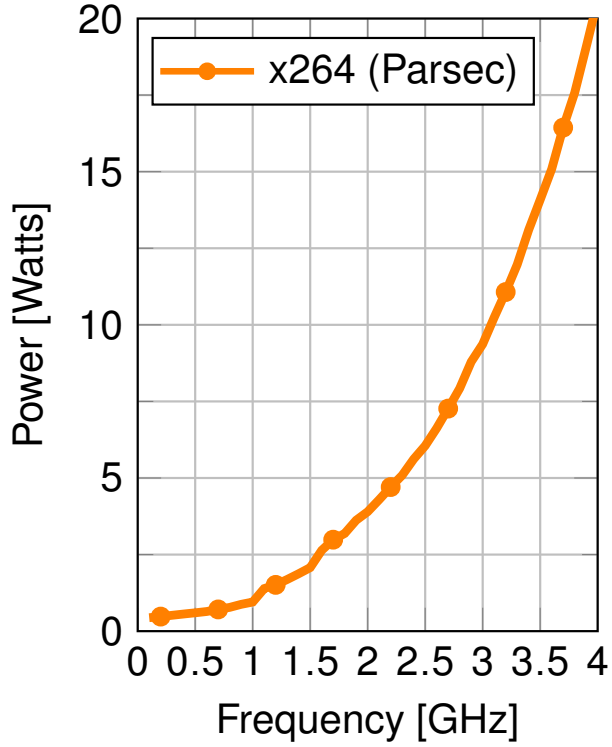

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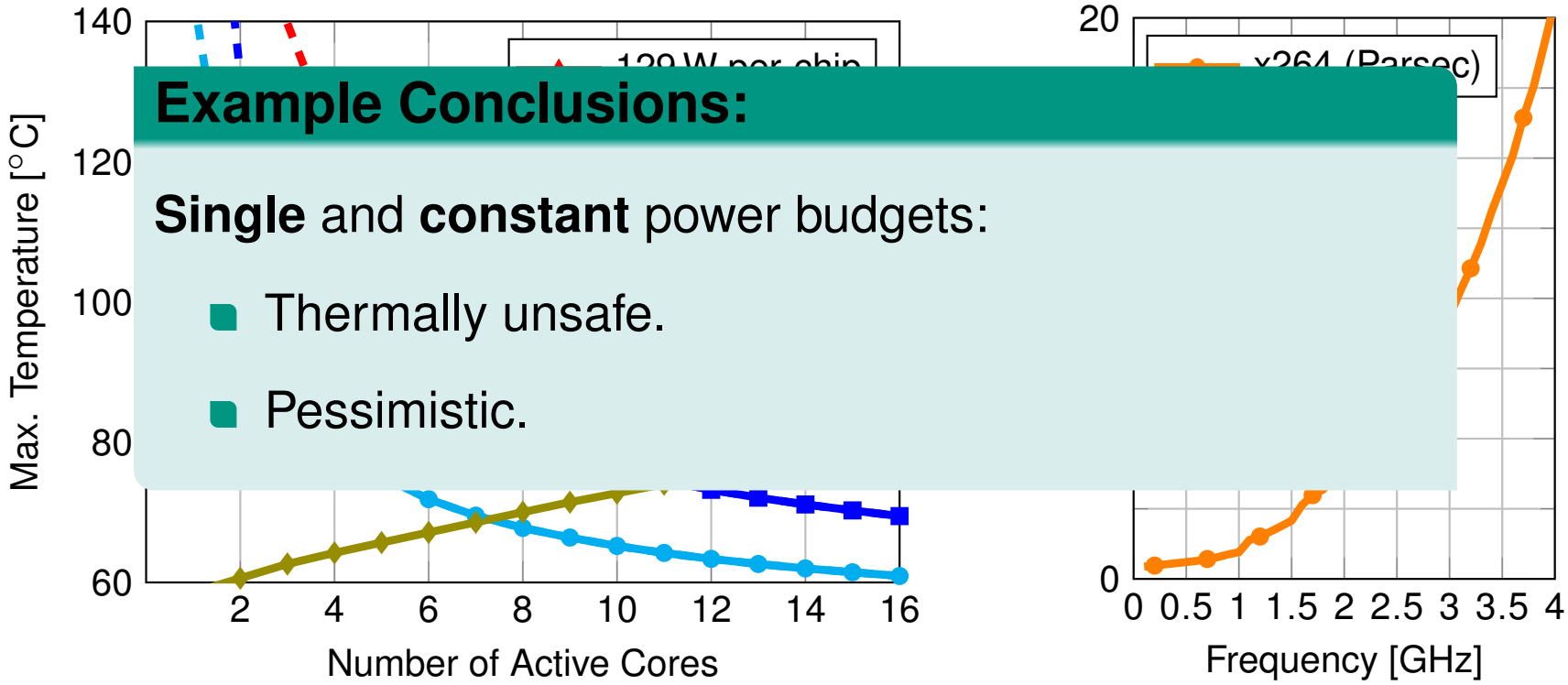


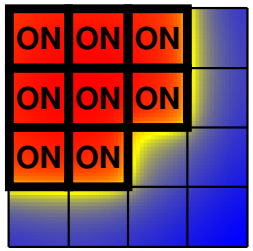
Example Conclusions:

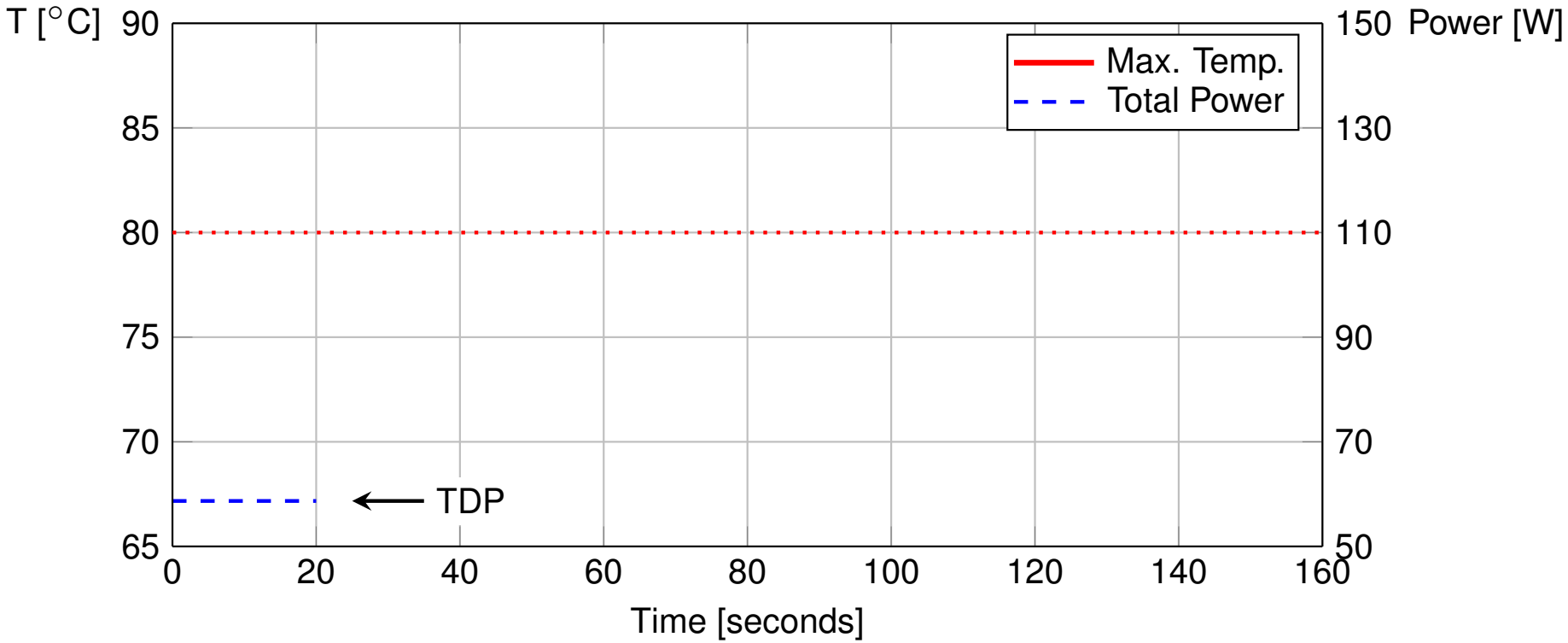
Single and **constant** power budgets:

- Thermally unsafe.
- Pessimistic.

Motivational Example

- **Boosting** over a TDP of 59 Watts.
- 8 active cores:





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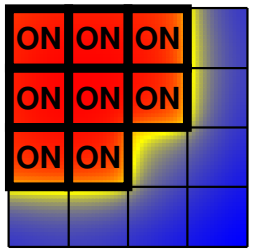

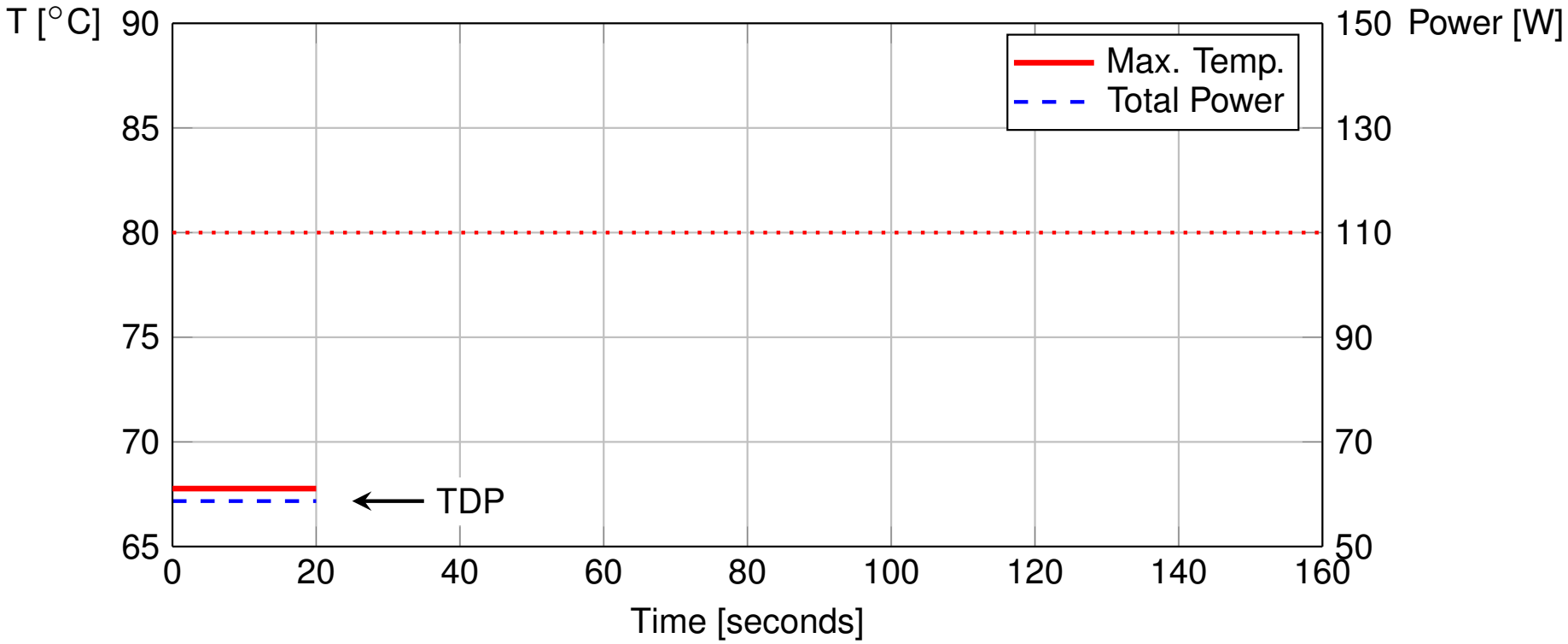

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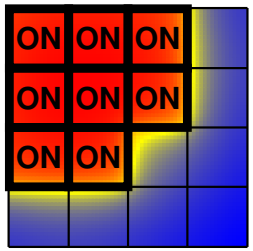

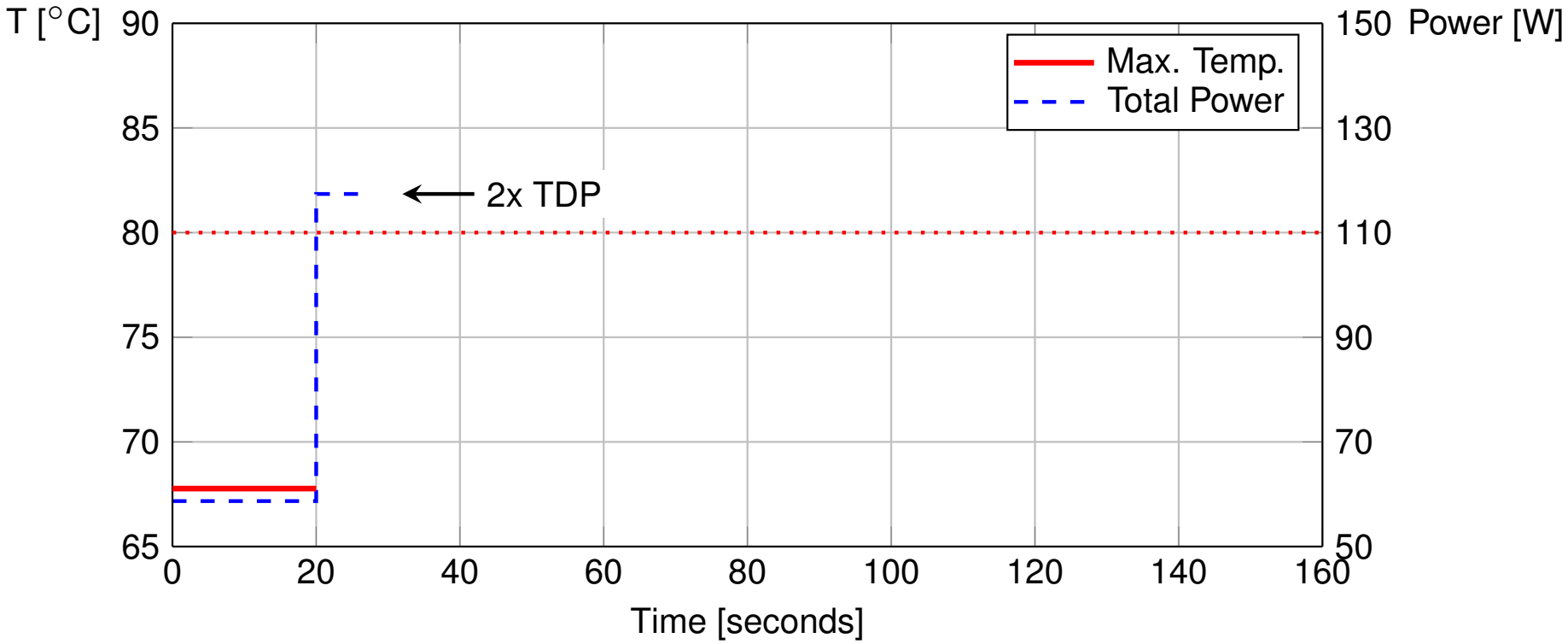

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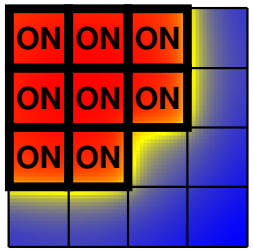

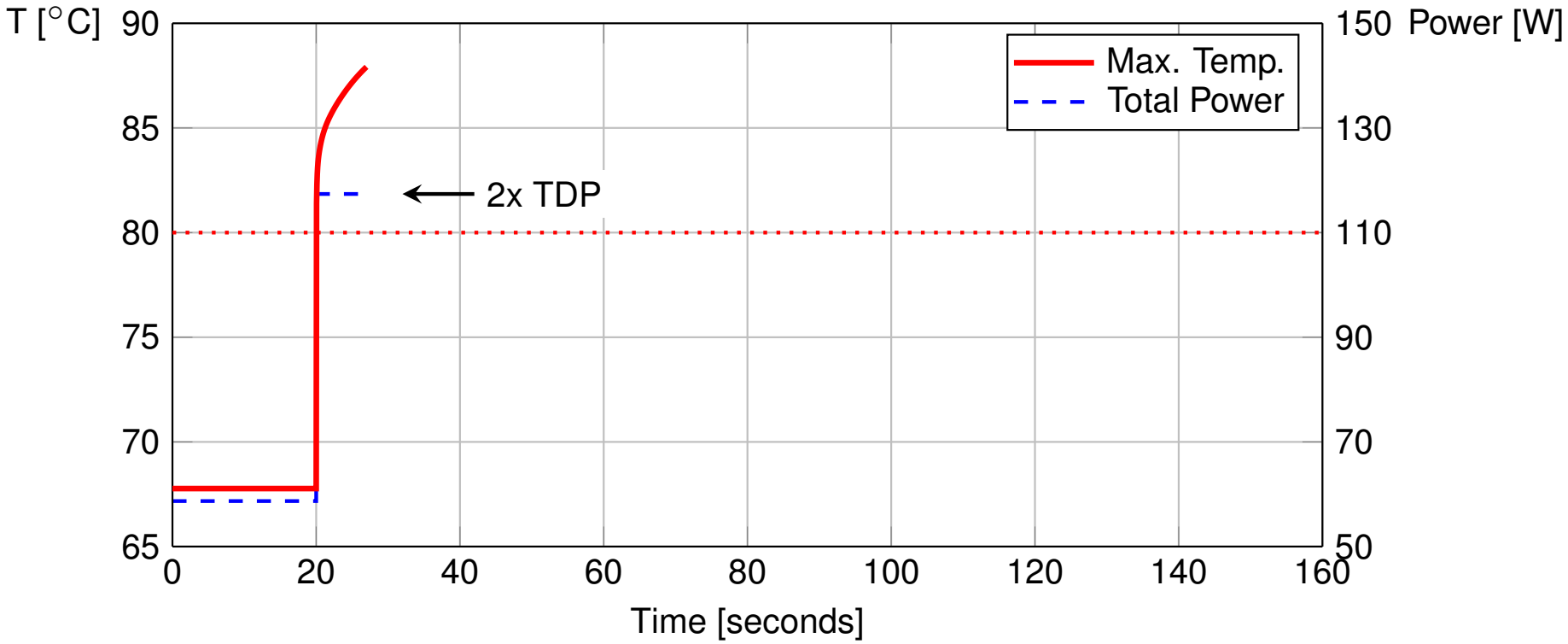

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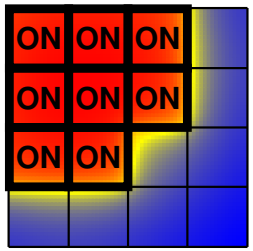

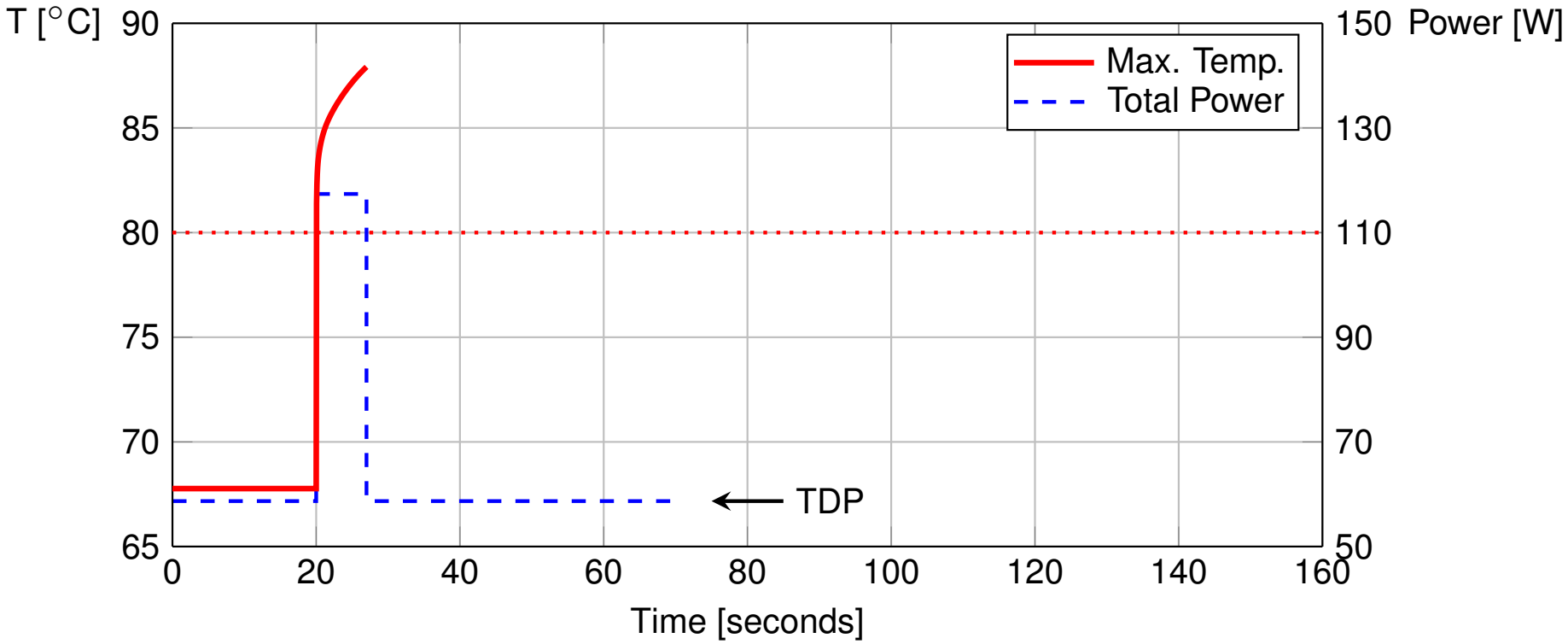

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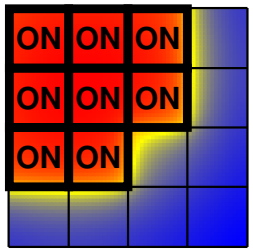

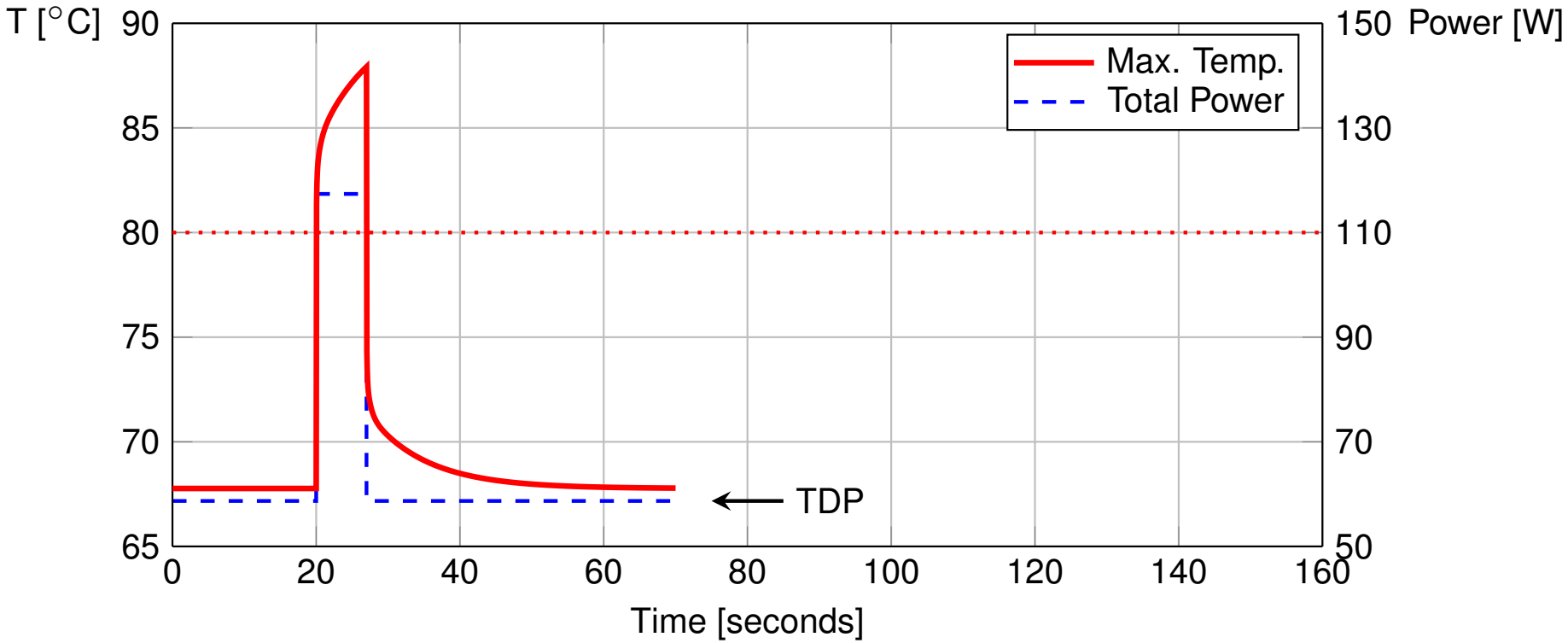

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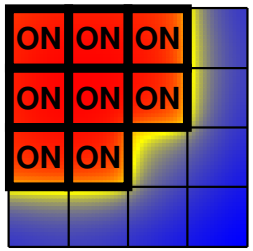

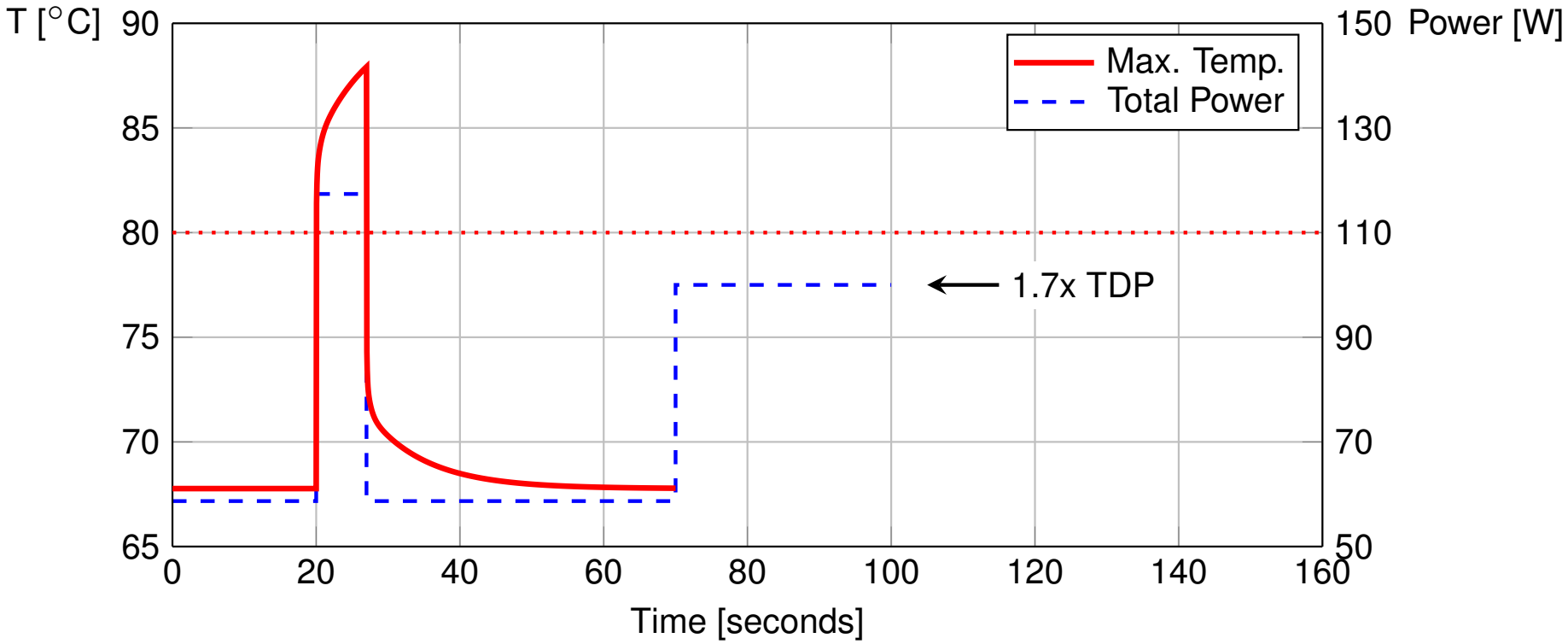

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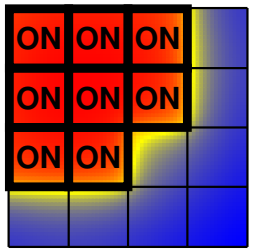

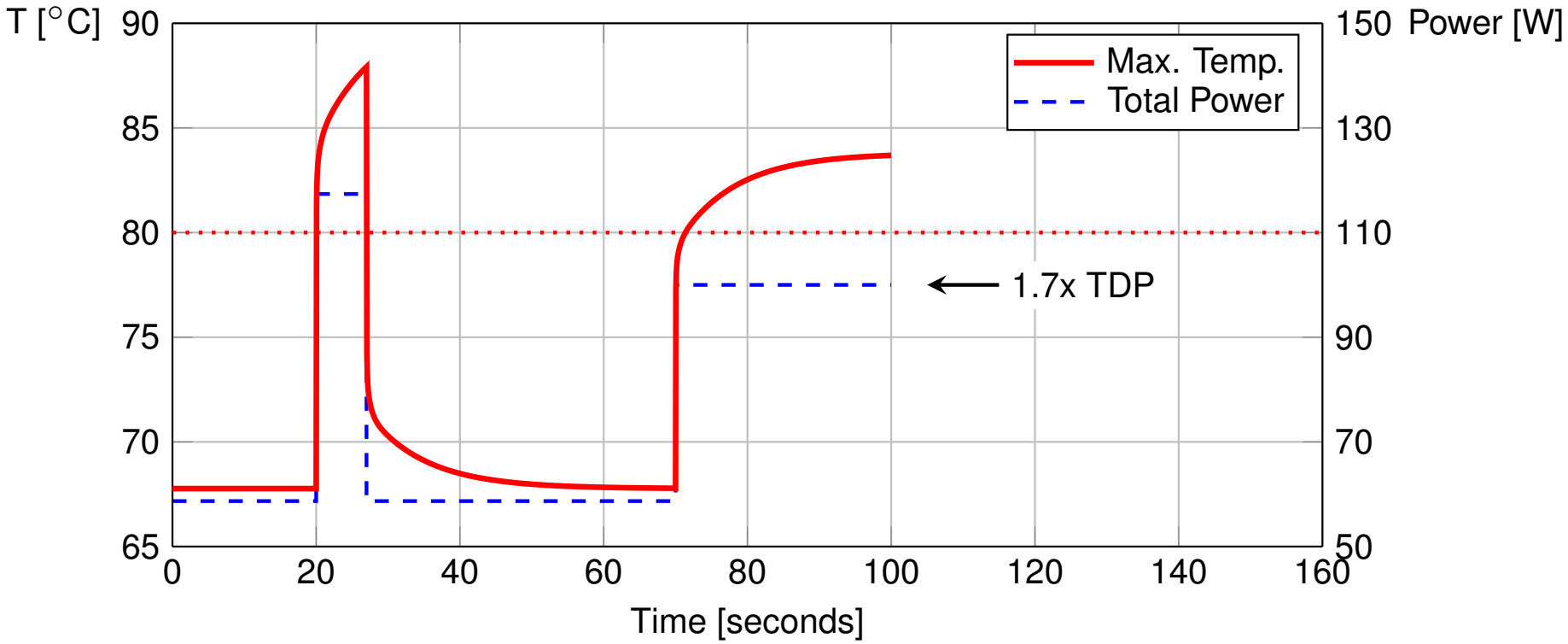

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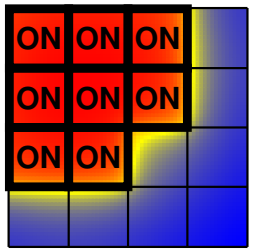

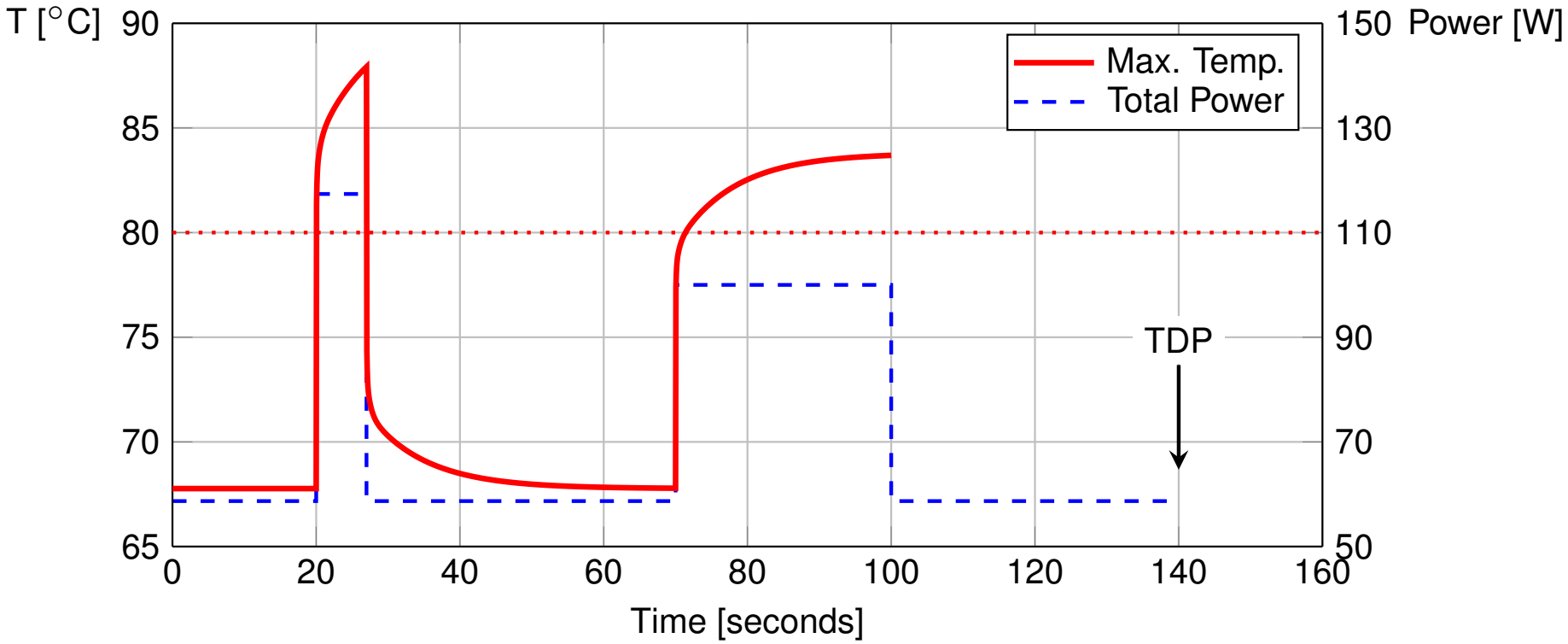

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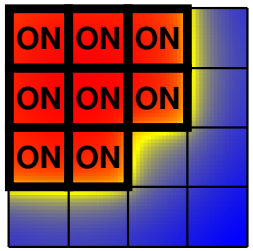

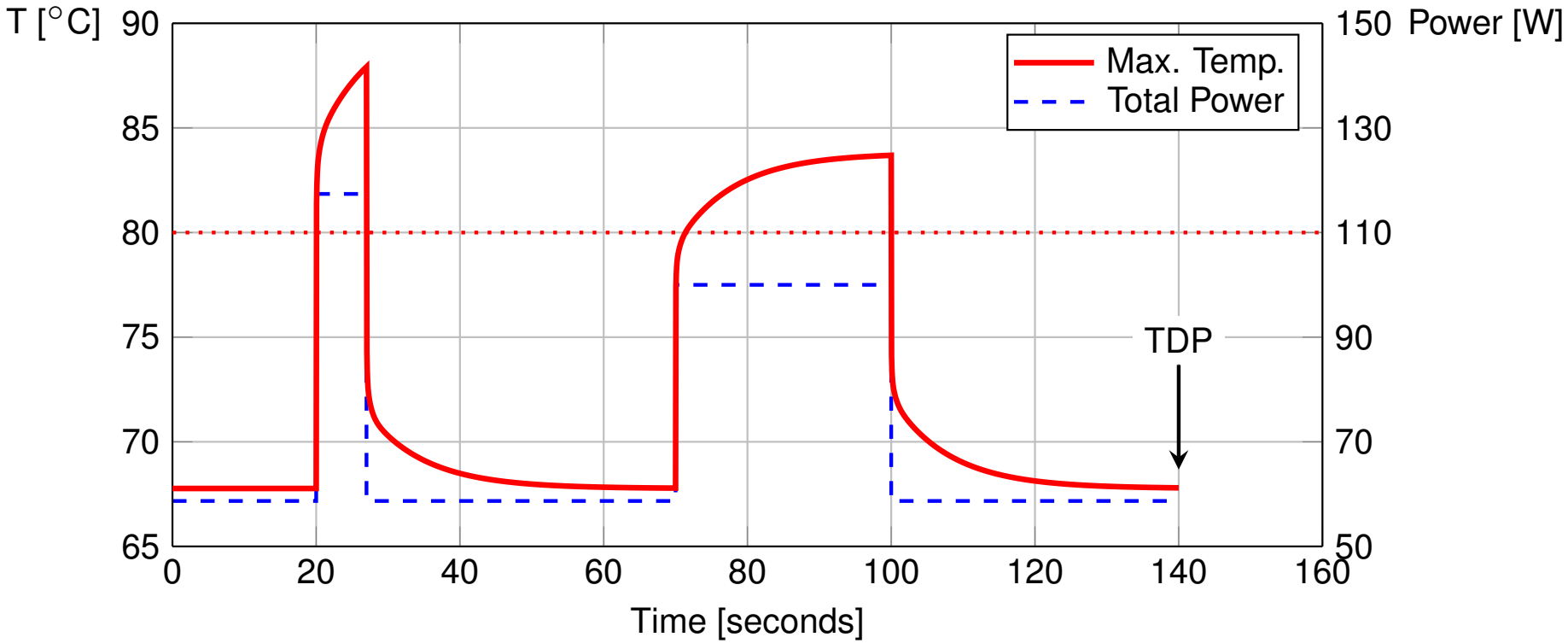

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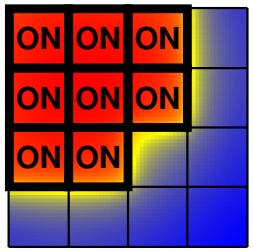

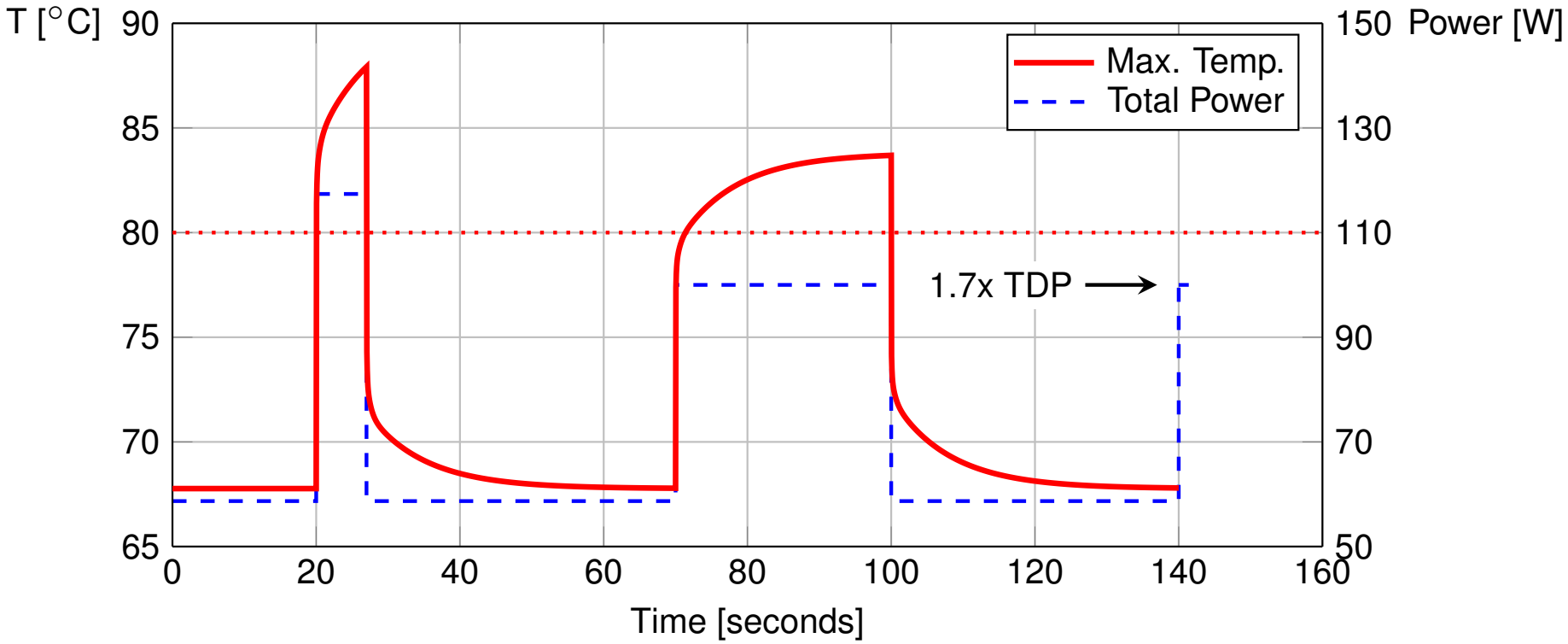

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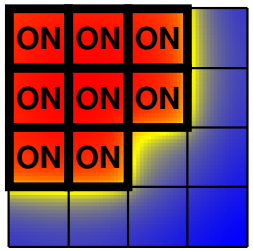

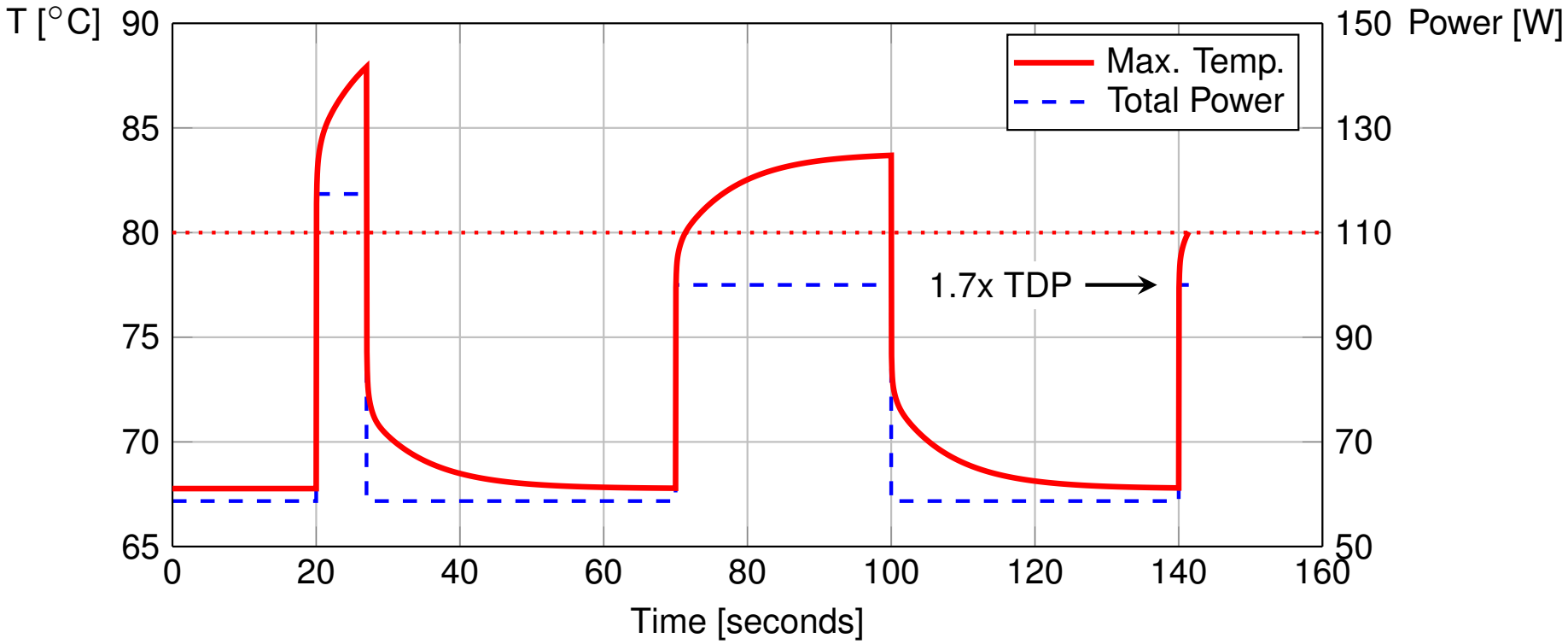

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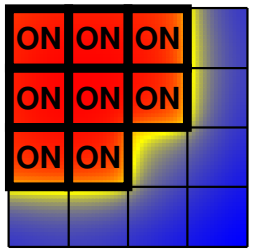

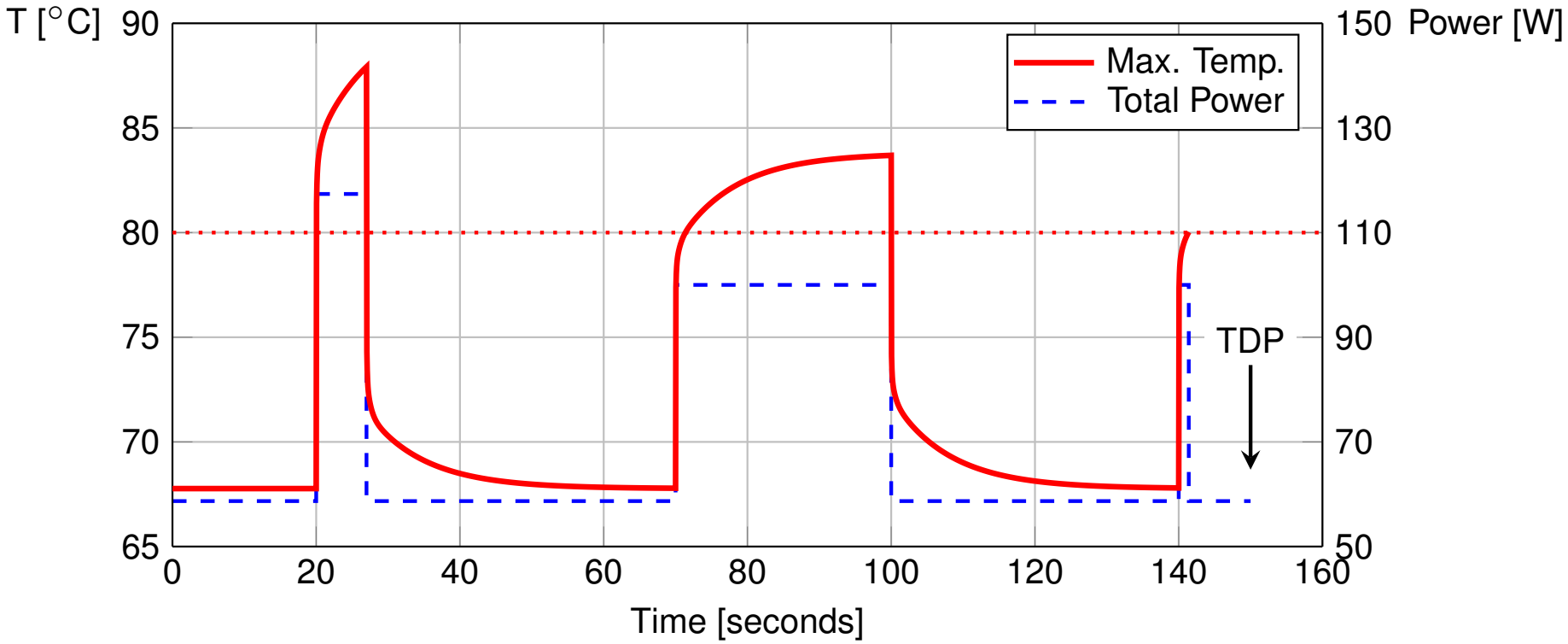

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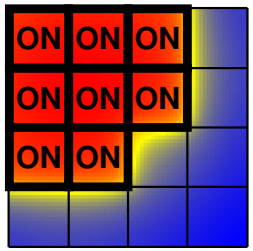

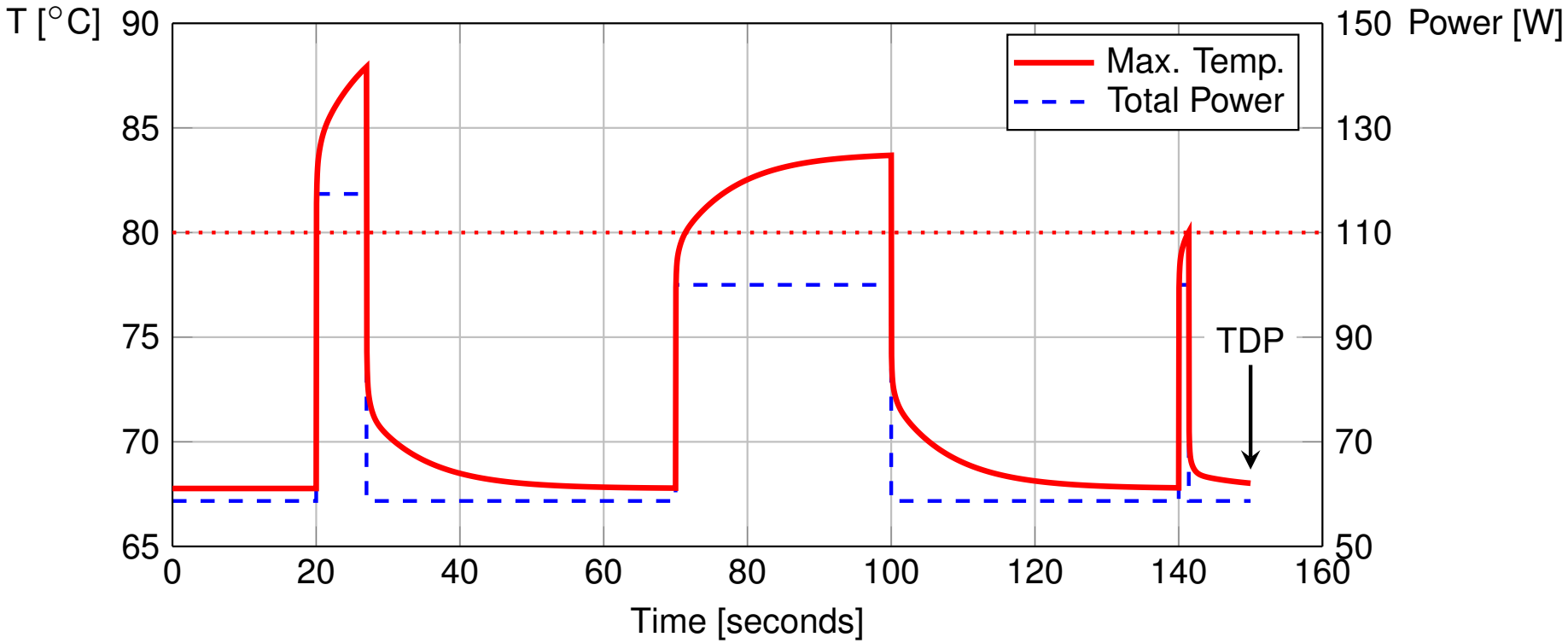

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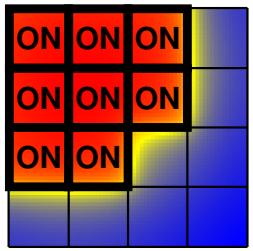

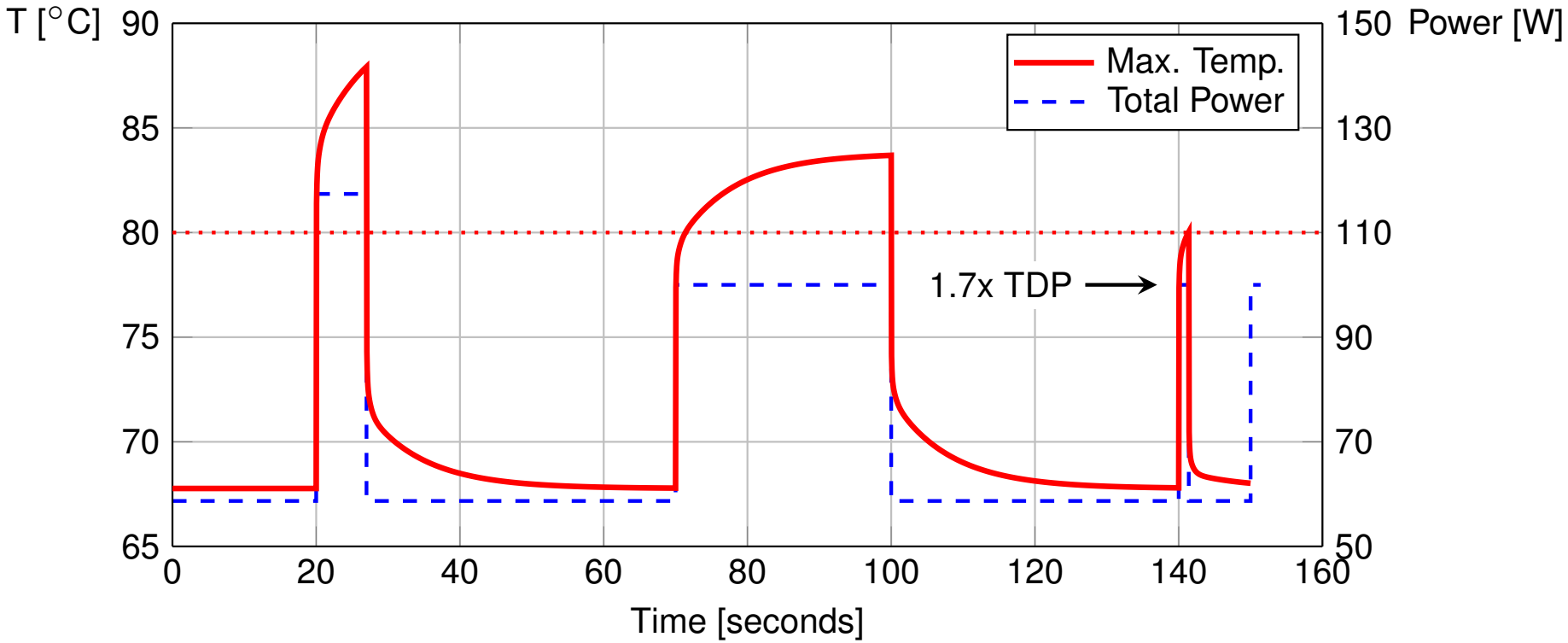

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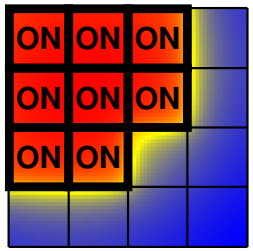

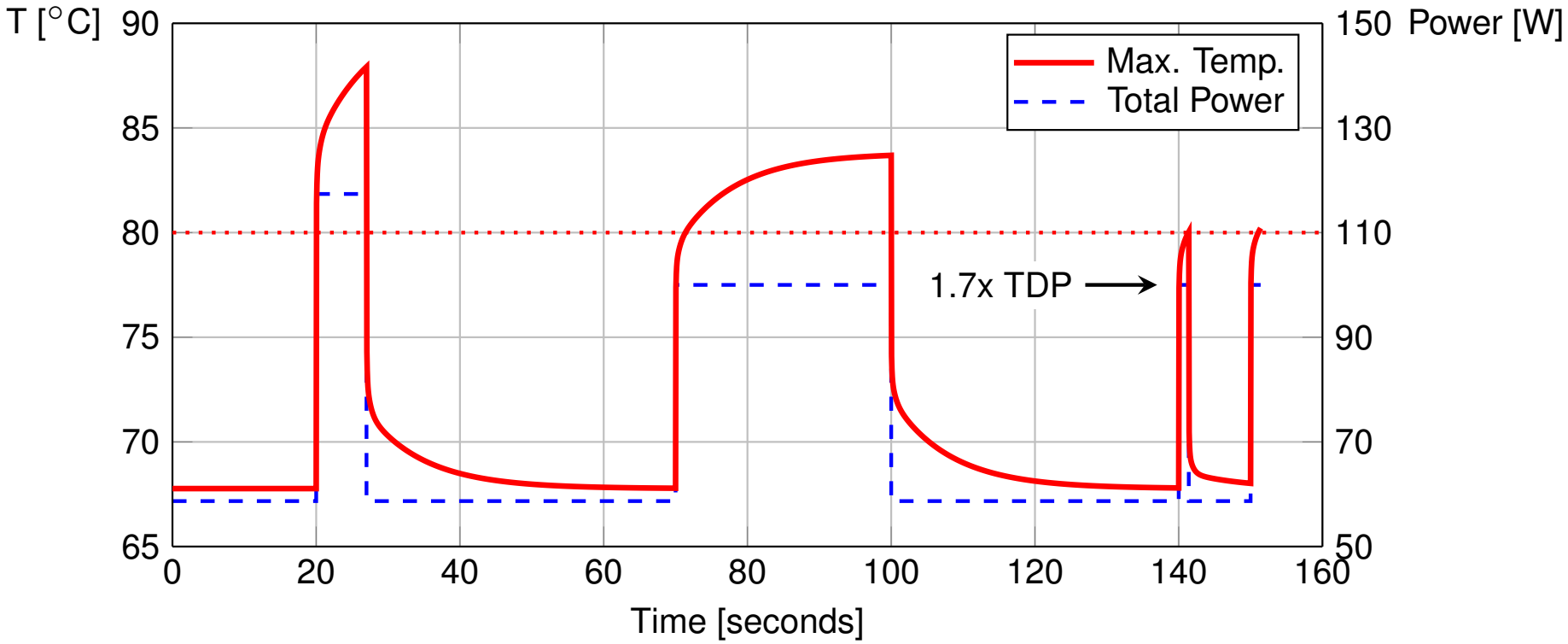

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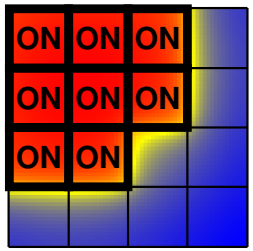

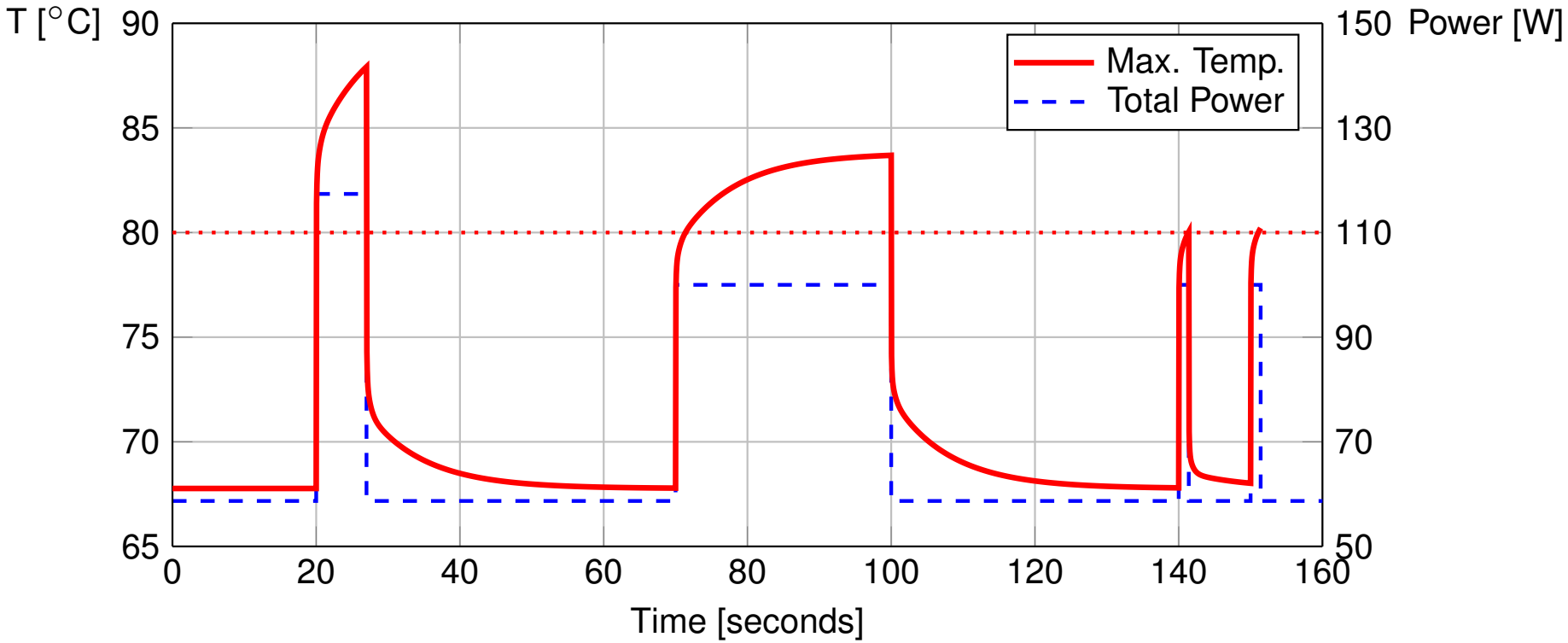

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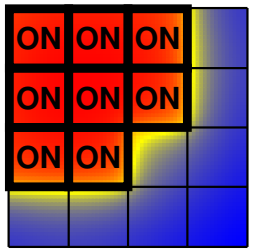

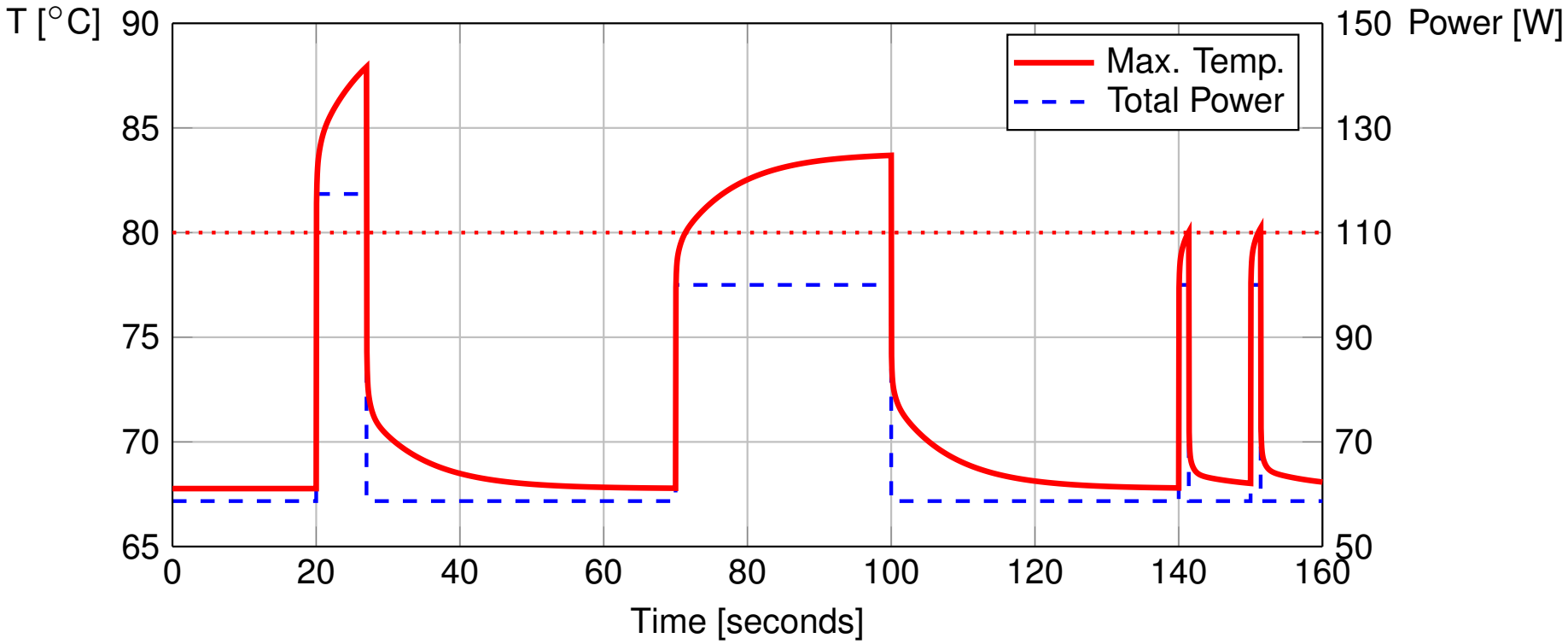

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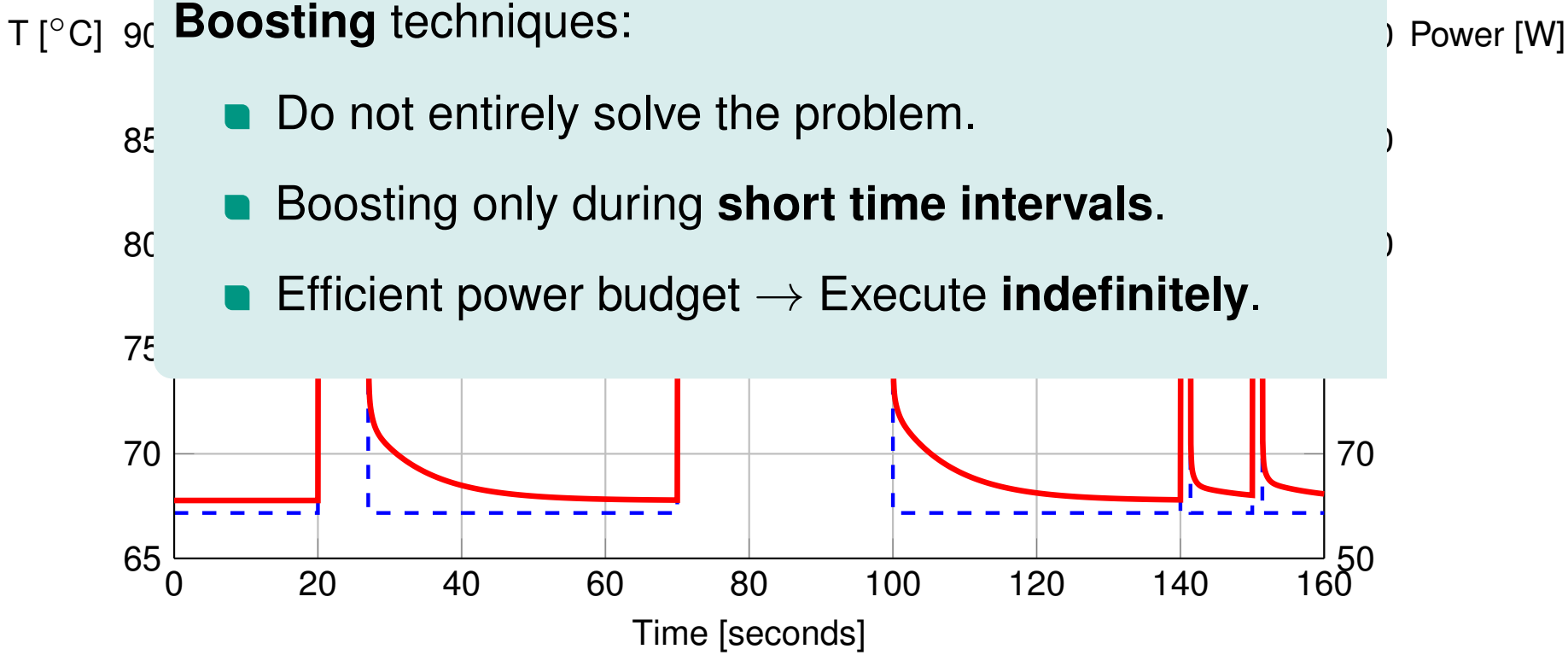
Example Conclusions:

Boosting techniques:

- Do not entirely solve the problem.
- Boosting only during **short time intervals**.
- Efficient power budget $\rightarrow$ Execute **indefinitely**.



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- Achieve **higher system performance**.
- Efficient power budget:
  - **Thermally safe**: TSP does no trigger DTM.
  - **Not pessimistic**: Allows power values that result in highest temperatures near T_{DTM}.

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$\Rightarrow$ **Thermal Safe Power (TSP)**

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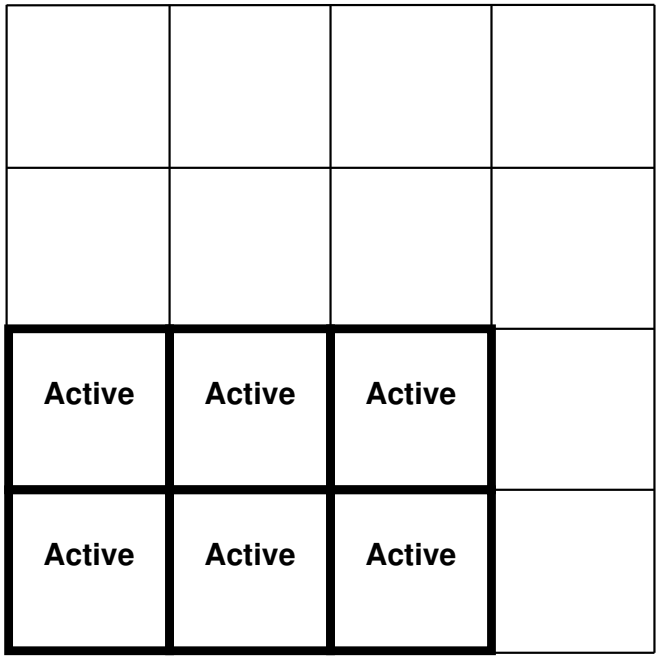

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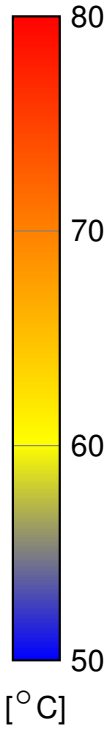

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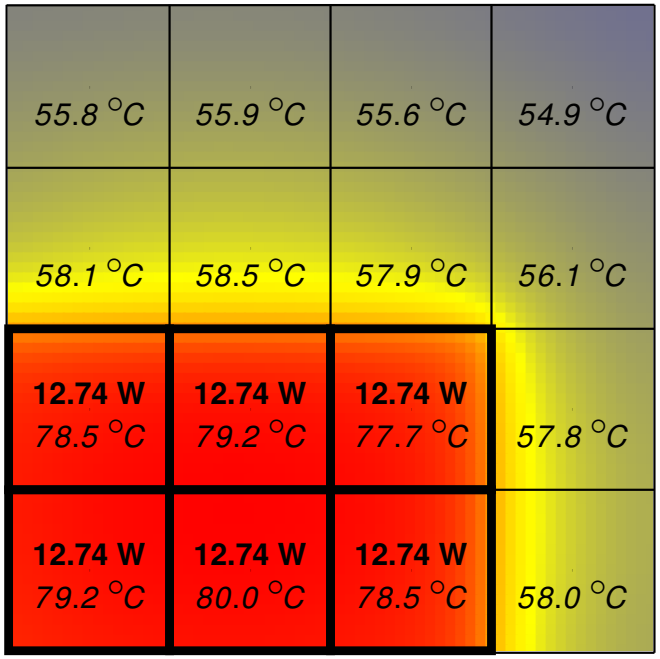

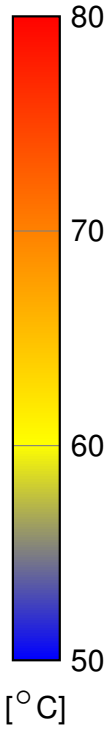

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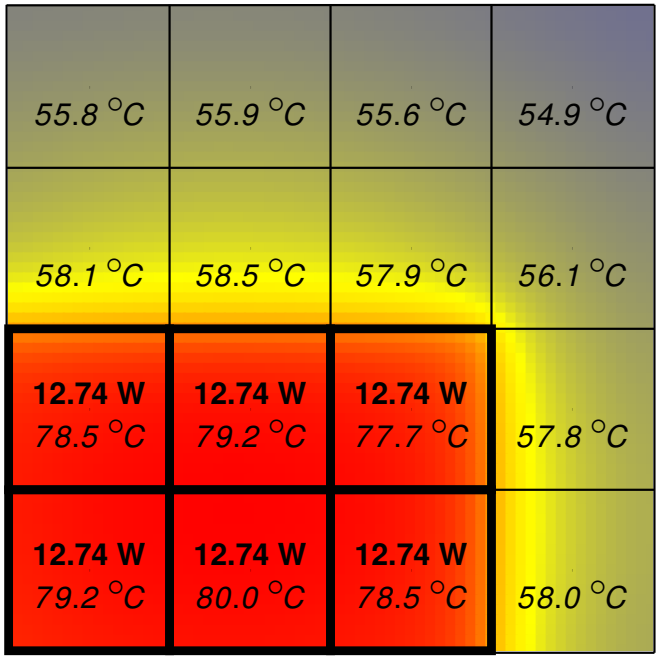

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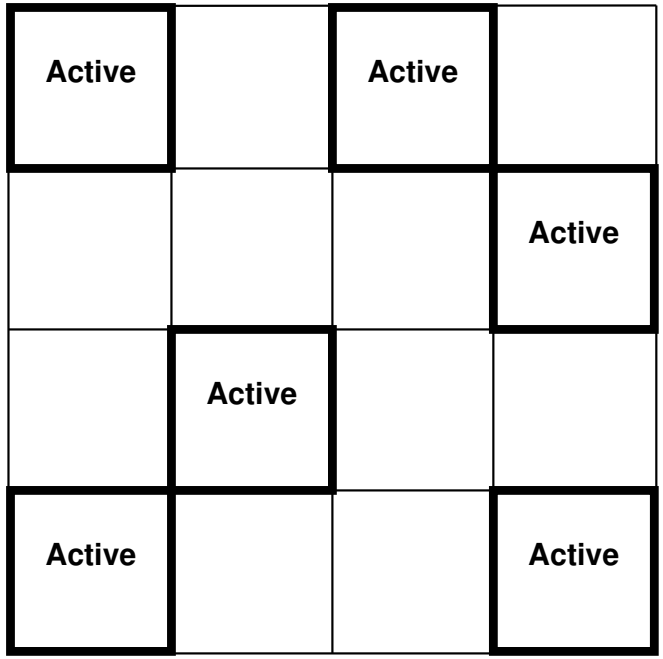

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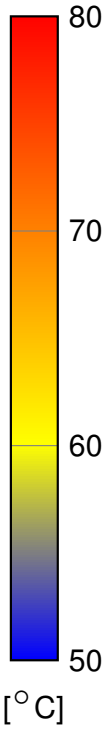

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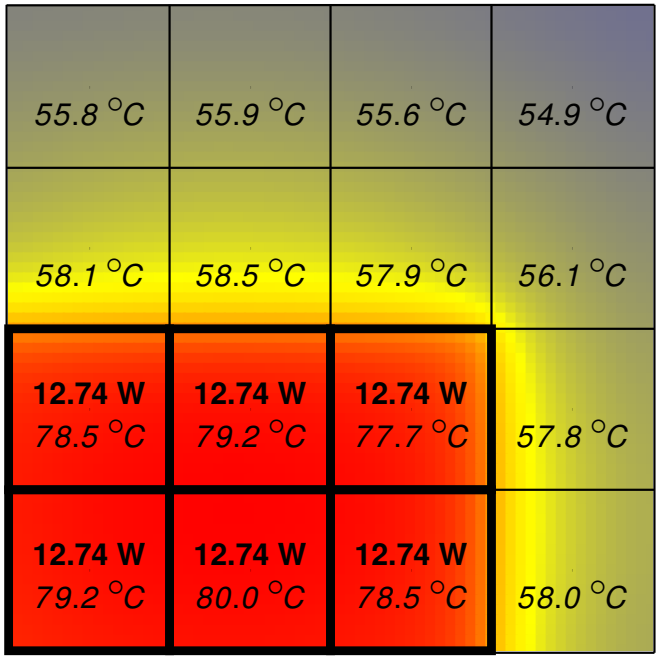

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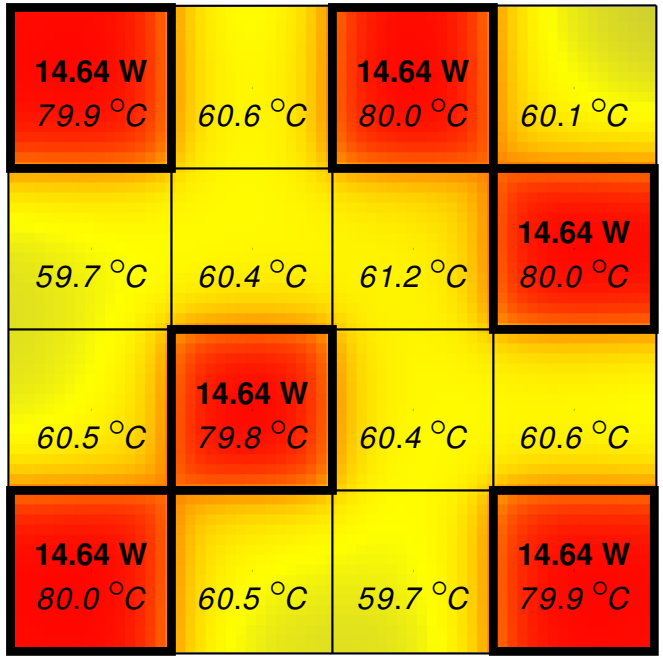

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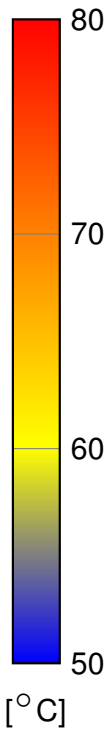

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TSP table built at design time:

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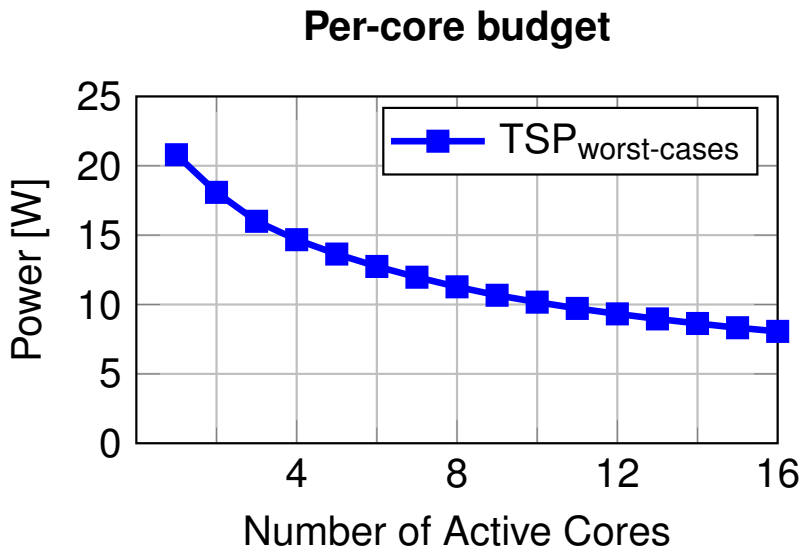
TSP per-core [W]	20.79	18.08	16.00	14.67	13.64	12.74	11.97	11.27	10.67	10.17	9.72	9.33	8.96	8.63	8.33	8.06



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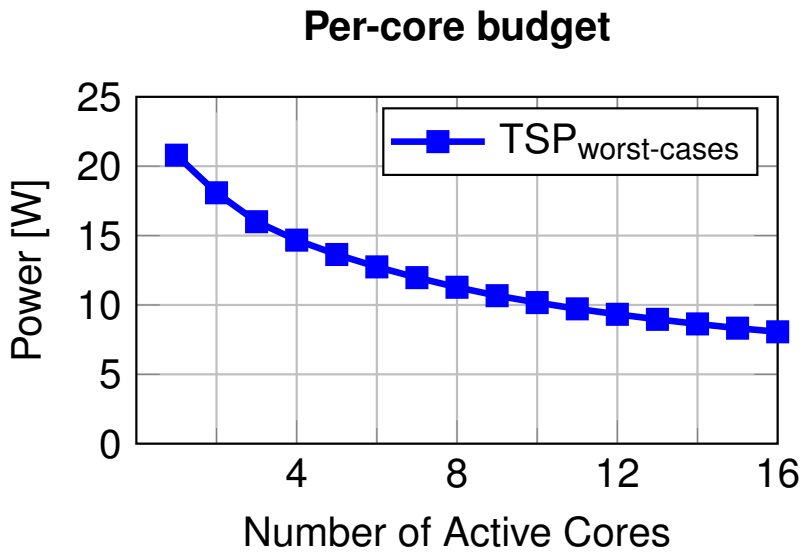

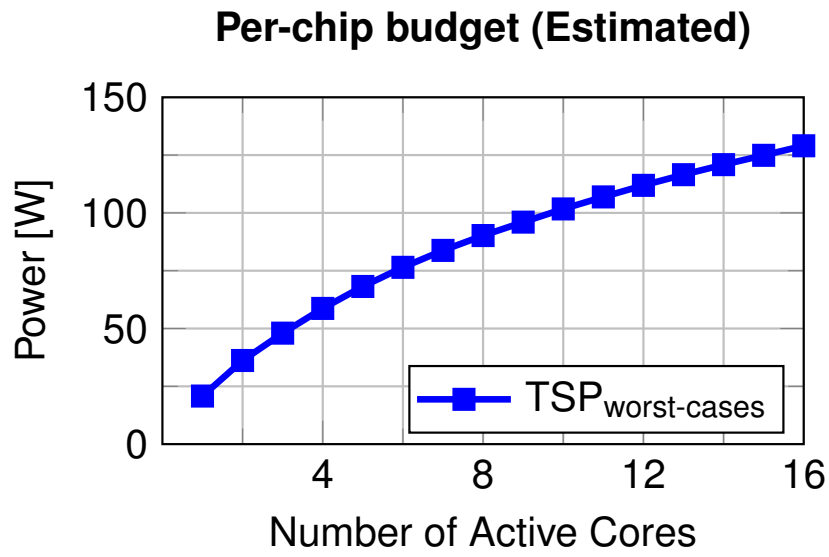

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For a given mapping **Q**:

- All active cores consume $P_{\text{TSP}}(\mathbf{Q}) \rightarrow$ **Highest** temperatures.
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$$T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b^{-1}{}_{i,j} \cdot q_j + P_{\text{inact}}^{\text{core}} \cdot \sum_{\forall j \in \mathbf{K}'} b^{-1}{}_{i,j} \left(1 - q_j\right) + \sum_{j=1}^{N} b^{-1}{}_{i,j} \left(p_j^{\text{blocks}} + T_{\text{amb}} \cdot g_j\right)$$

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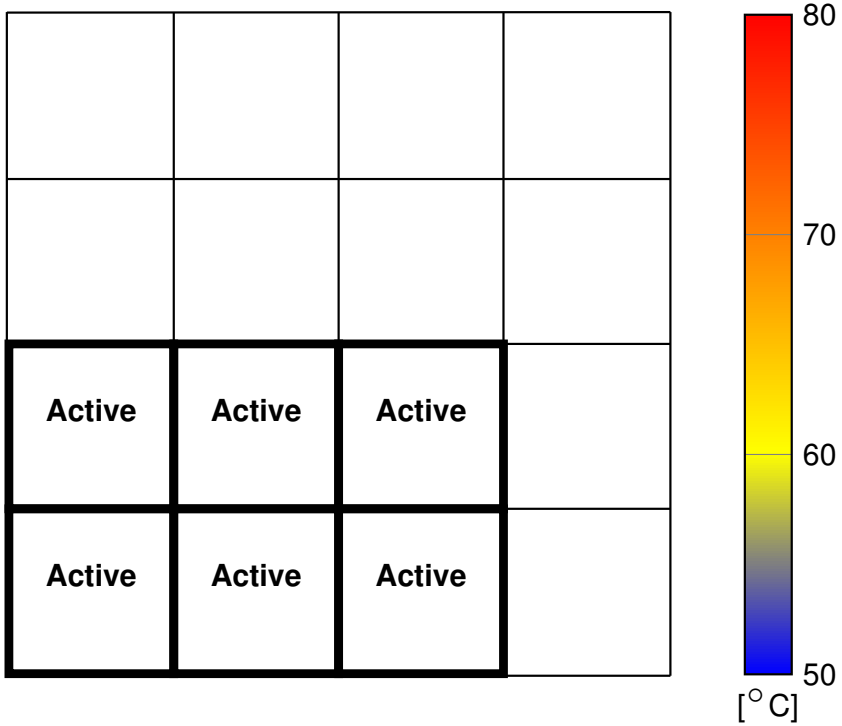
$$T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b^{-1}{}_{i,j} \cdot q_j + P^{\text{cor}}_{\text{ina}} \quad \textbf{Constant for node } i \quad \left(p_j^{\text{blocks}} + T_{\text{amb}} \cdot g_j \right)$$

- Our algorithm: For every node i
  - Set $T_i = T_{\text{DTM}}$.
  - Compute P_{equal}.
  - $P_{\text{TSP}}(\mathbf{Q}) \leftarrow$ Minimum P_{equal}.

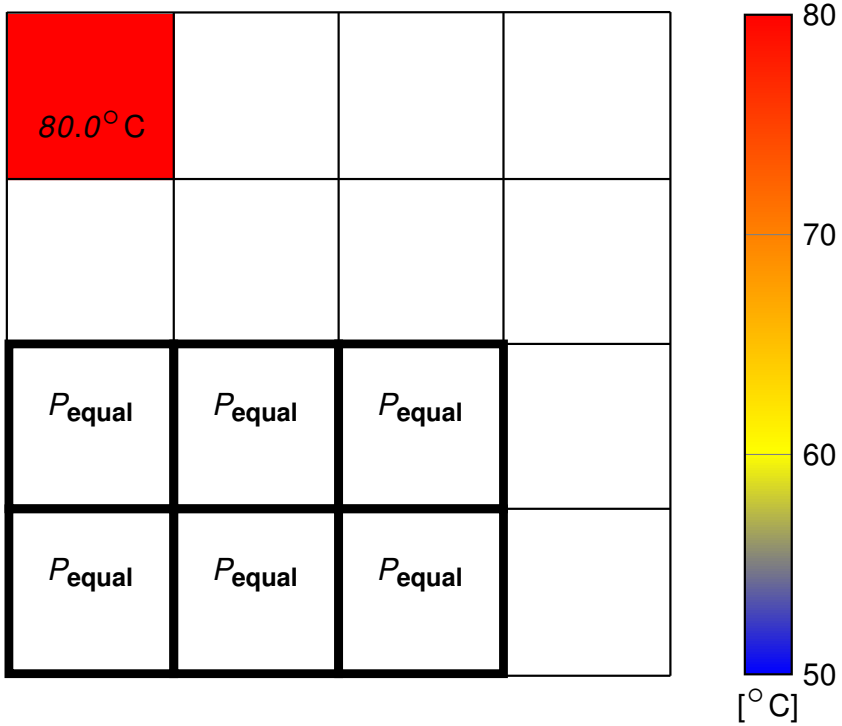
TSP for Given Mappings

Example for a given mapping **Q**:



TSP for Given Mappings

Example for a given mapping **Q**:

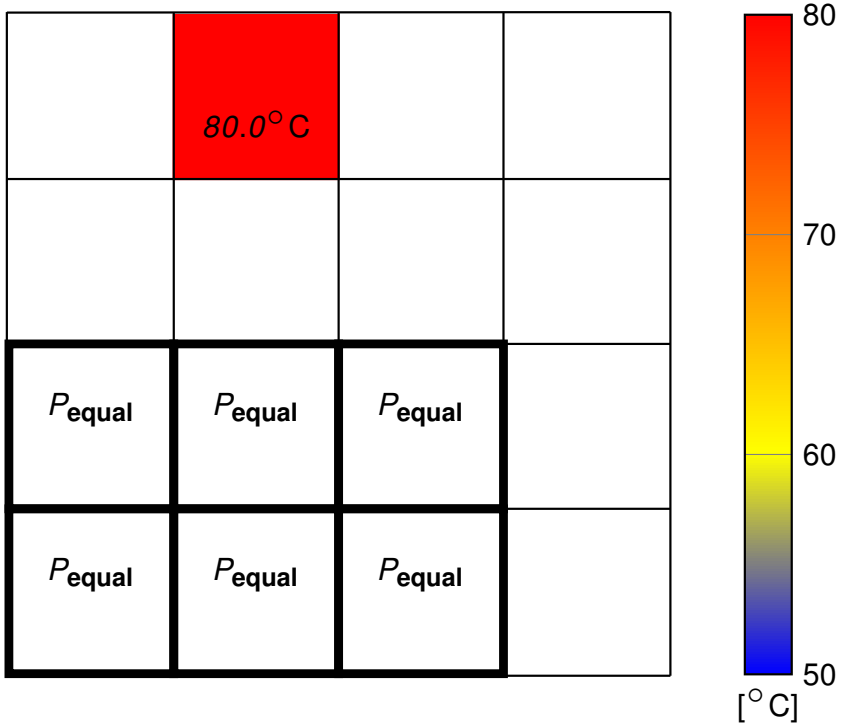


$$T_1 = 80.0^\circ C \rightarrow P_{\text{equal}} = 41.30W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 41.30W$$

TSP for Given Mappings

Example for a given mapping **Q**:

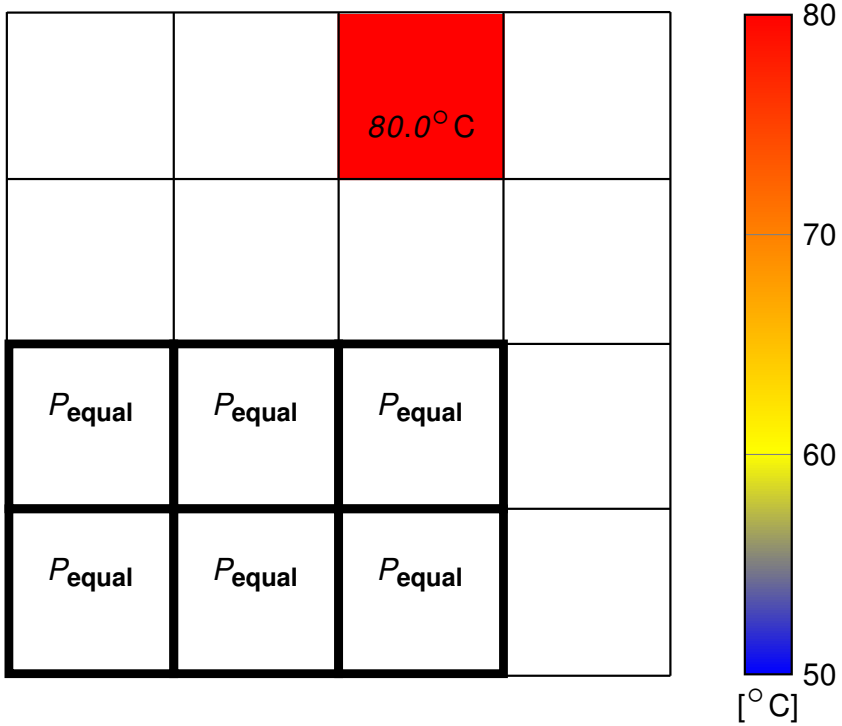


$$T_2 = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 40.92W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 40.92W$$

TSP for Given Mappings

Example for a given mapping **Q**:

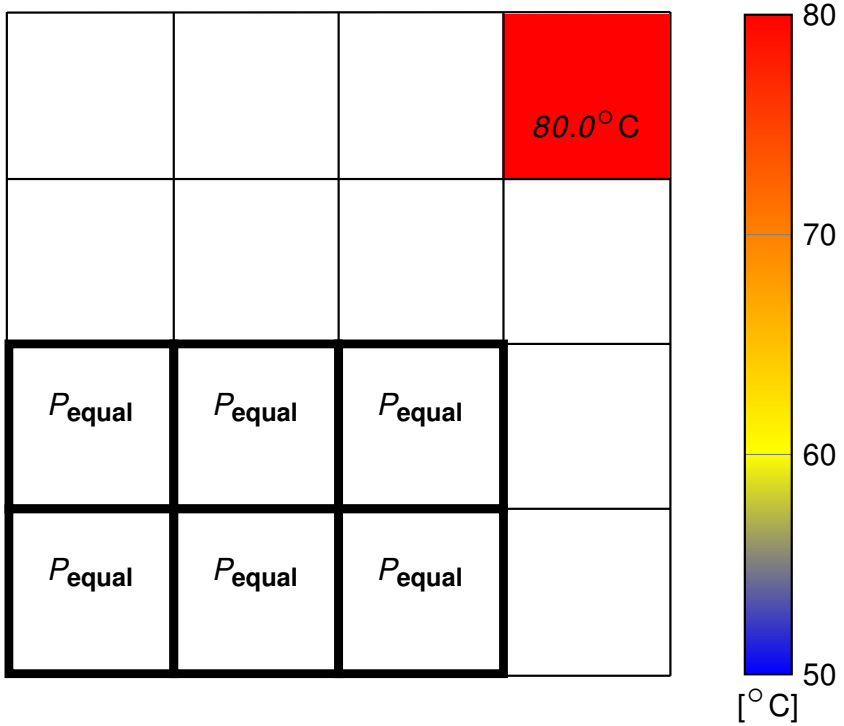


$$T_3 = 80.0^\circ C \rightarrow P_{\text{equal}} = 42.08 W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 40.92 W$$

TSP for Given Mappings

Example for a given mapping **Q**:

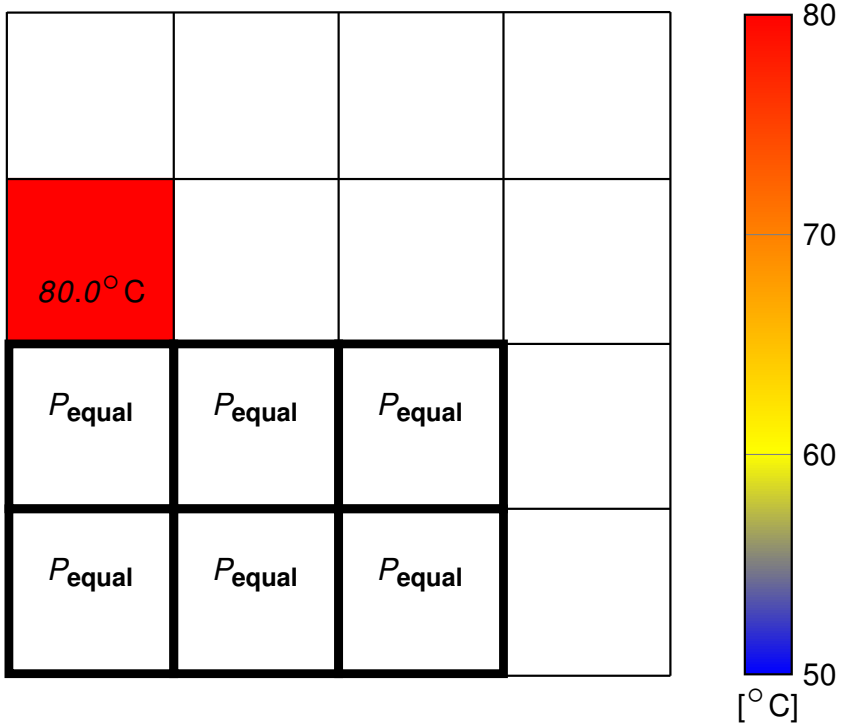


$$T_4 = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 44.83W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 40.92W$$

TSP for Given Mappings

Example for a given mapping **Q**:

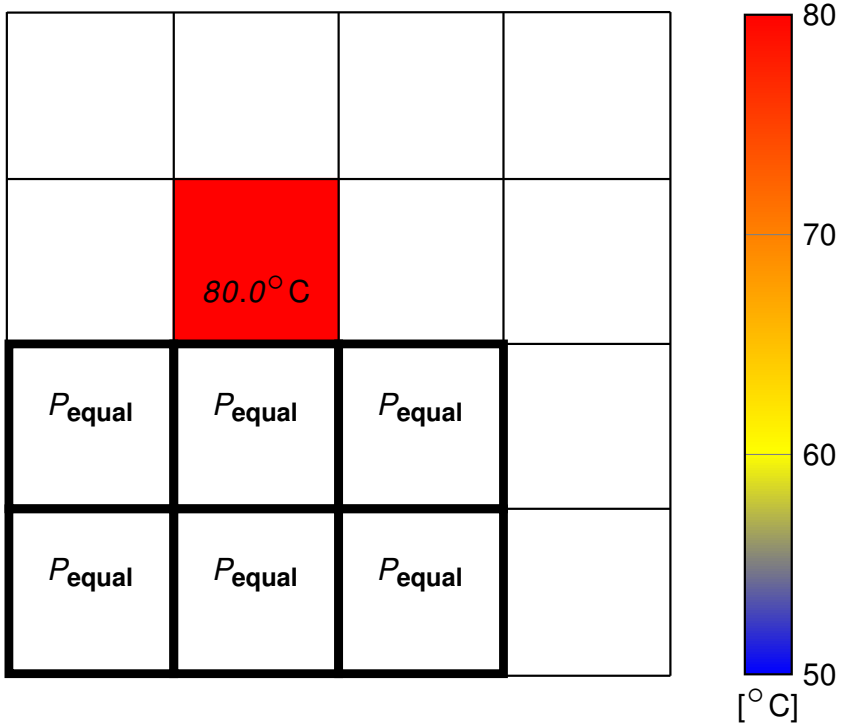


$$T_5 = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 33.99W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 33.99W$$

TSP for Given Mappings

Example for a given mapping **Q**:

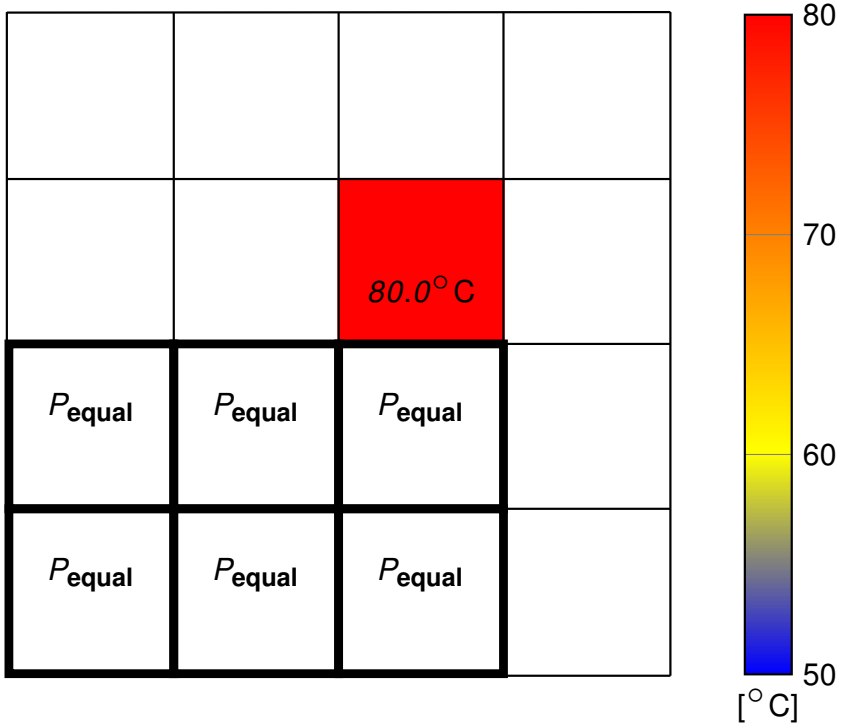


$$T_6 = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 33.11W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 33.11W$$

TSP for Given Mappings

Example for a given mapping **Q**:

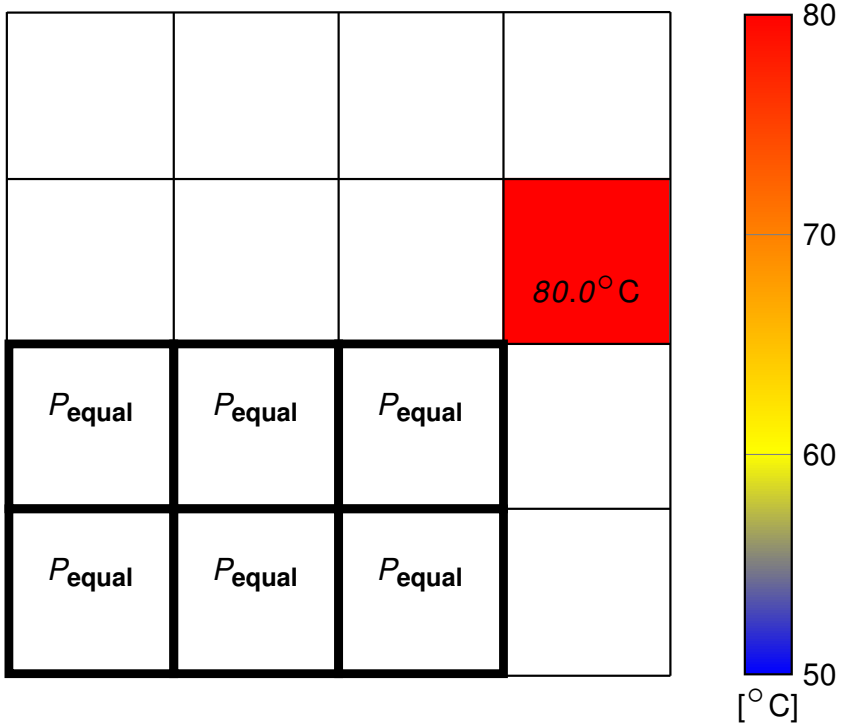


$$T_7 = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 34.60W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 33.11W$$

TSP for Given Mappings

Example for a given mapping **Q**:

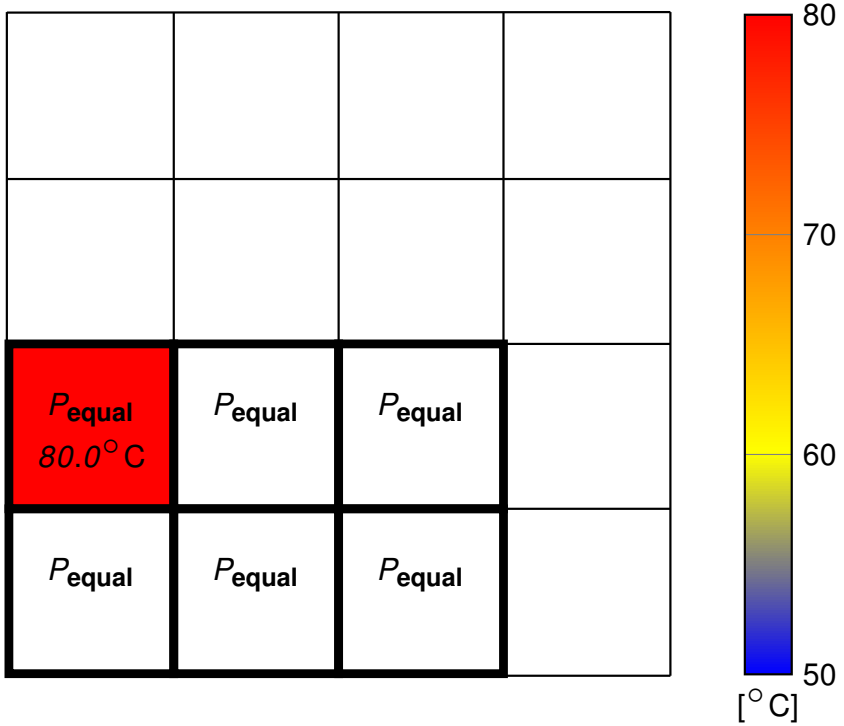


$$T_8 = 80.0^\circ C \rightarrow P_{\text{equal}} = 40.30 W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 33.11 W$$

TSP for Given Mappings

Example for a given mapping **Q**:

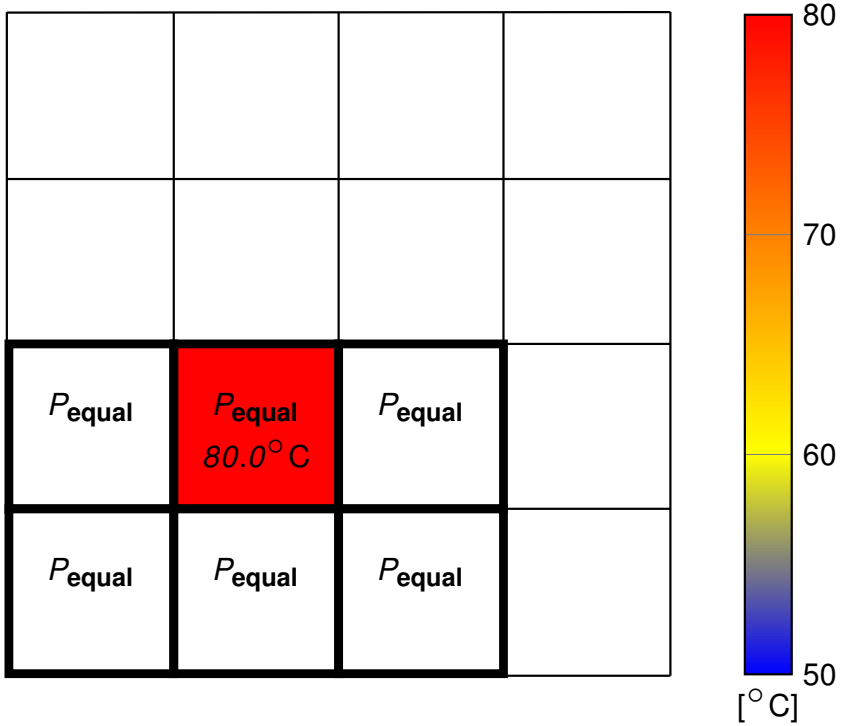


$$T_9 = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 13.32W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 13.32W$$

TSP for Given Mappings

Example for a given mapping **Q**:

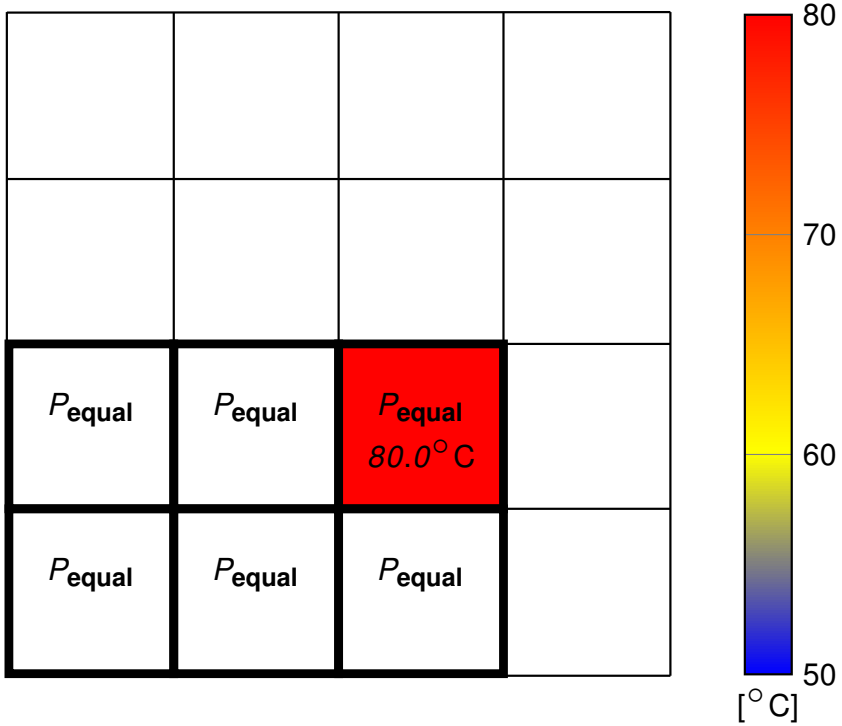


$$T_{10} = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 13.04W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 13.04W$$

TSP for Given Mappings

Example for a given mapping **Q**:

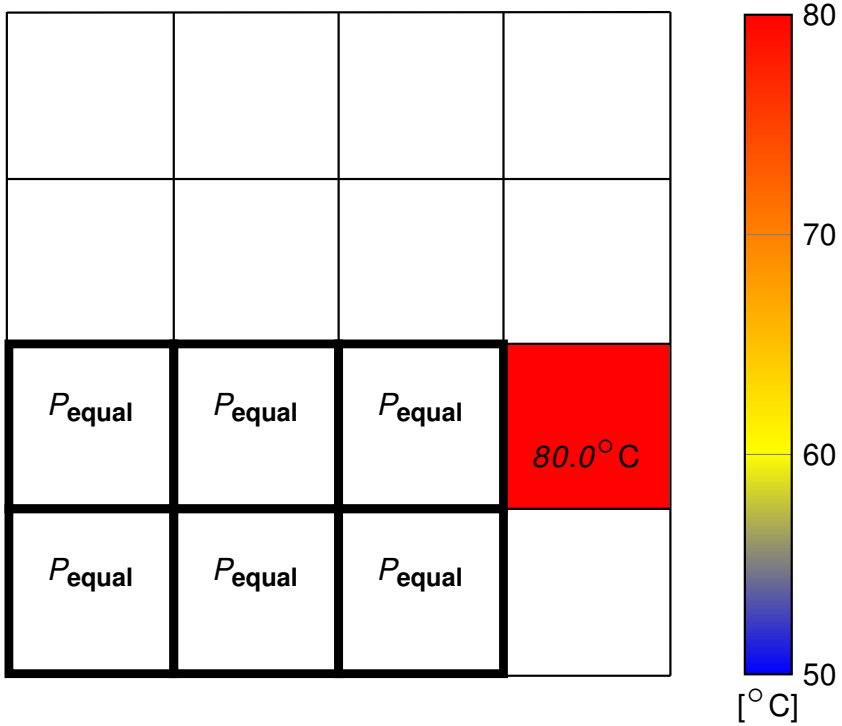


$$T_{11} = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 13.62W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 13.04W$$

TSP for Given Mappings

Example for a given mapping **Q**:

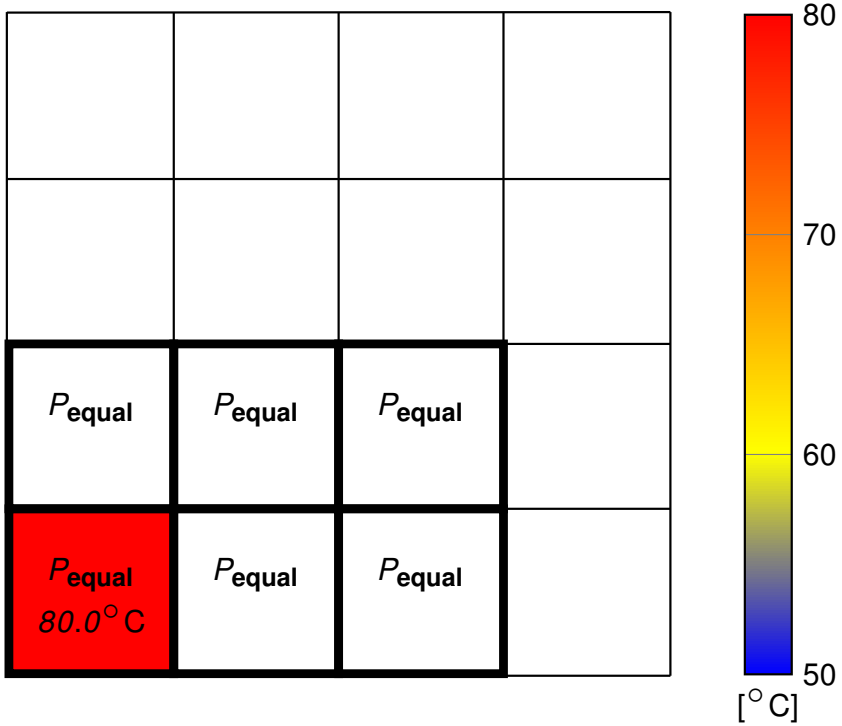


$$T_{12} = 80.0^{\circ}C \rightarrow P_{equal} = 34.93W$$

$$P_{TSP}(\mathbf{Q}) = 13.04W$$

TSP for Given Mappings

Example for a given mapping **Q**:

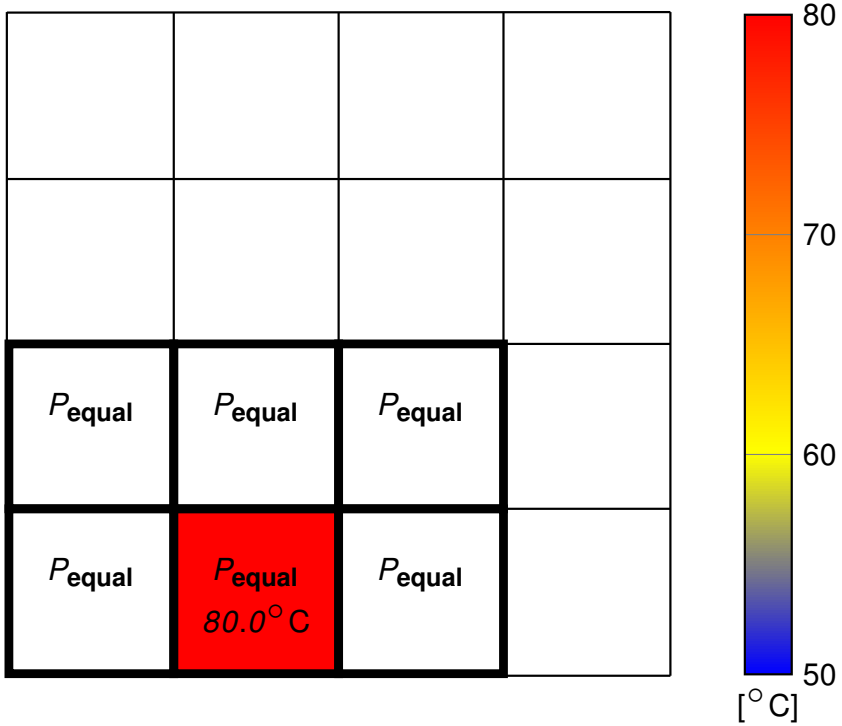


$$T_{13} = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 13.03W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 13.03W$$

TSP for Given Mappings

Example for a given mapping **Q**:

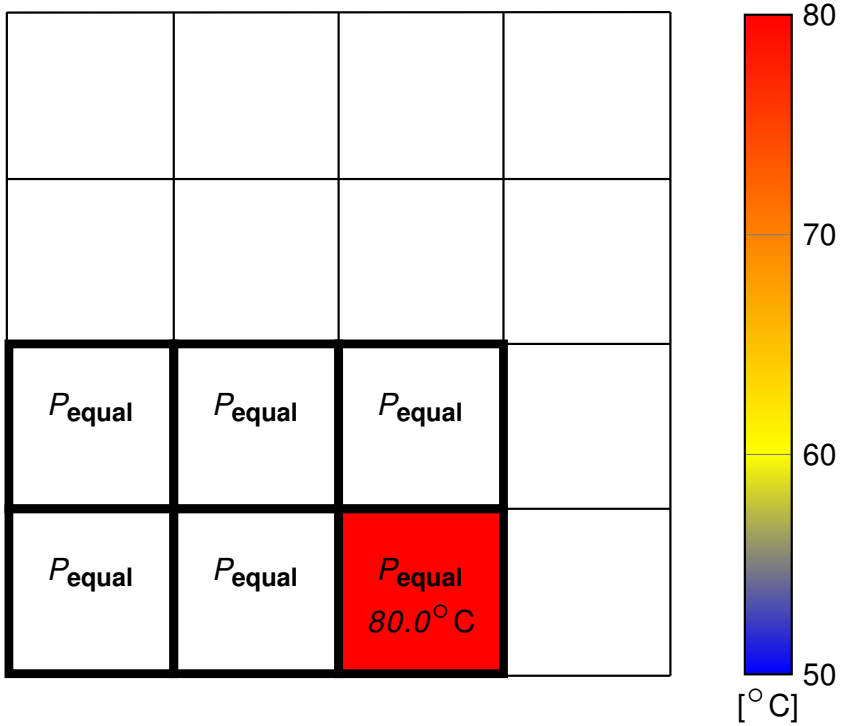


$$T_{14} = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 12.74W$$

$$P_{\text{TSP}}(\mathbf{Q}) = 12.74W$$

TSP for Given Mappings

Example for a given mapping **Q**:

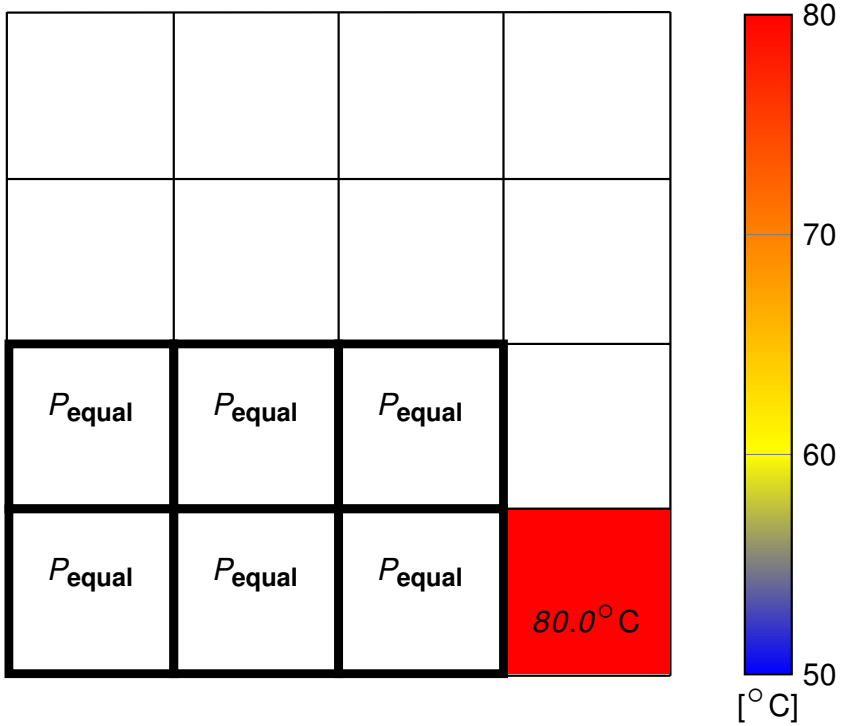


$$T_{15} = 80.0^{\circ}C \rightarrow P_{equal} = 13.31W$$

$$P_{TSP}(\mathbf{Q}) = 12.74W$$

TSP for Given Mappings

Example for a given mapping **Q**:

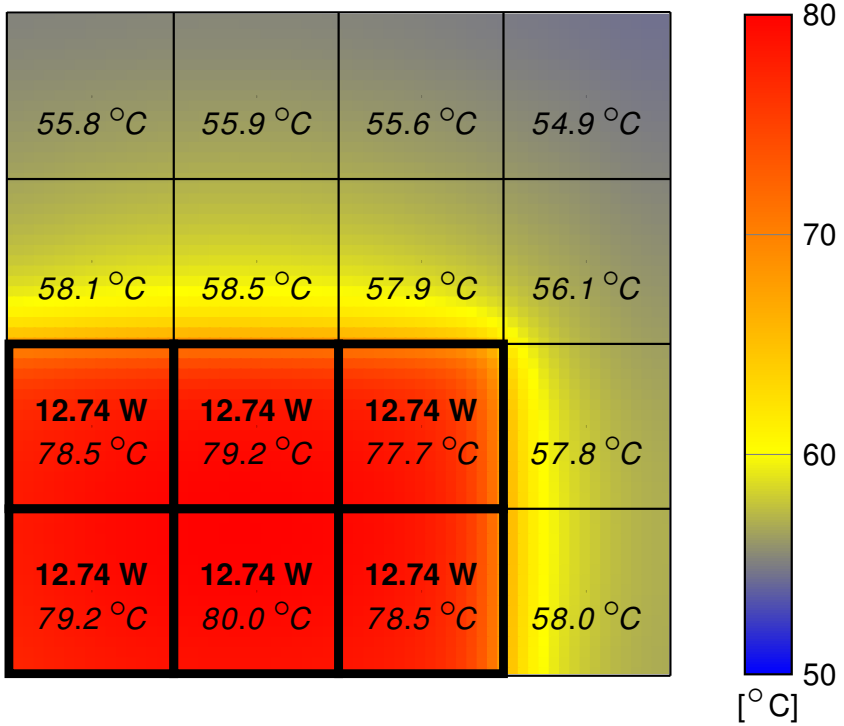


$$T_{16} = 80.0^{\circ}C \rightarrow P_{equal} = 34.22W$$

$$P_{TSP}(\mathbf{Q}) = 12.74W$$

TSP for Given Mappings

Example for a given mapping **Q**:



$$P_{\text{TSP}}(\mathbf{Q}) = 12.74W$$

Polynomial time complexity

Outline

- Introduction and State-of-the-art
- Motivation
- Objective and Contributions
- System Model
- Thermal Safe Power (TSP)
  - For Given Mappings
  - For the Worst-Case Mappings
- Evaluations
- Conclusions

TSP for the Worst-Case Mappings

- Most pessimistic (lowest) TSP value for m active cores.
- **Any** m cores can **safely** consume up to $P_{\text{TSP}}^{\text{worst}}(m)$.

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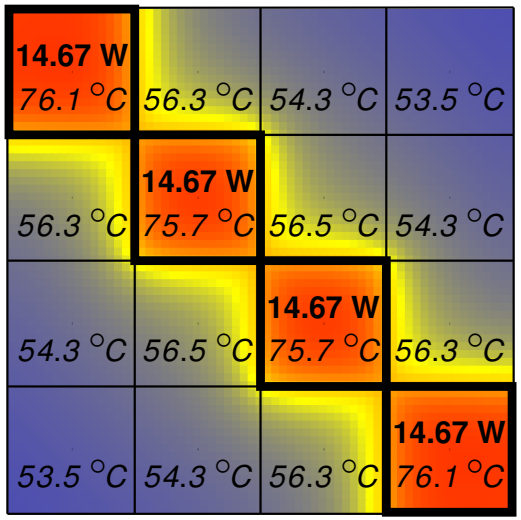
For example, with $P_{\text{TSP}}^{\text{worst}}(4) = 14.67$ W:



Highest Temperature: 76.1 °C

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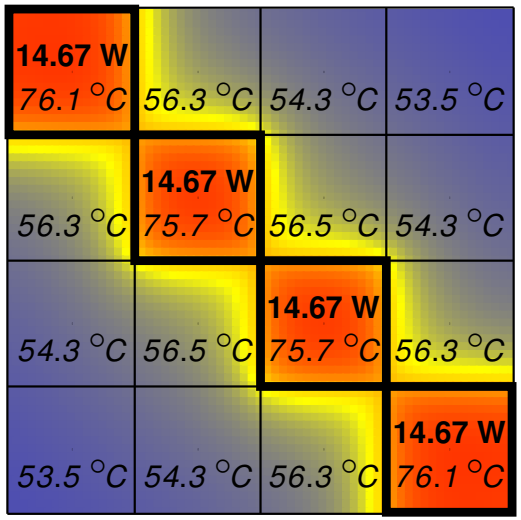
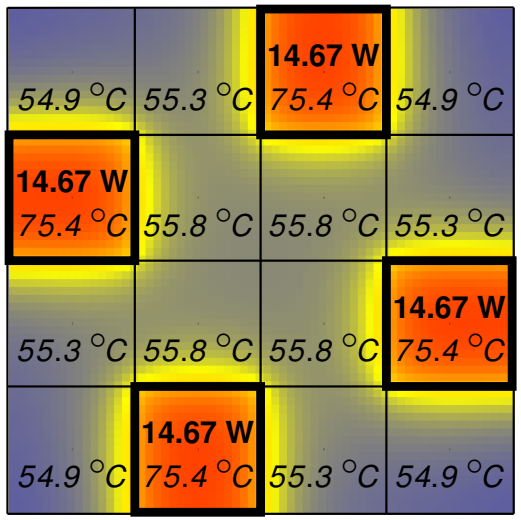
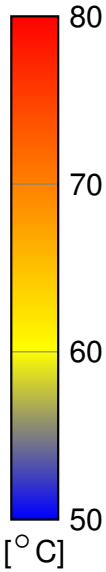


Highest Temperature: 76.1°C



Highest Temperature: 75.4°C



TSP for the Worst-Case Mappings

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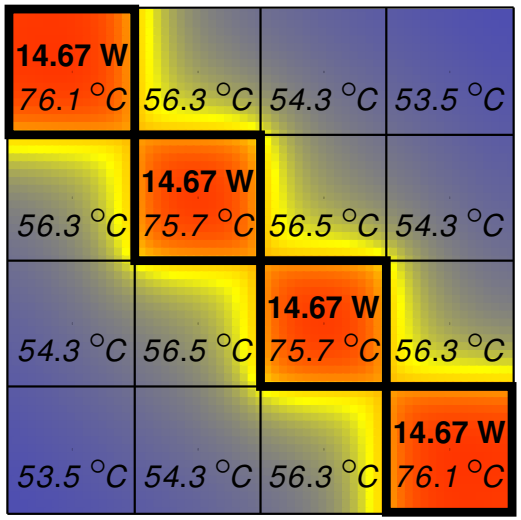
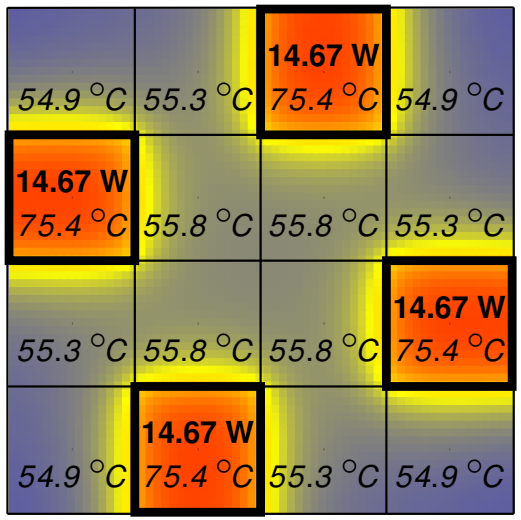
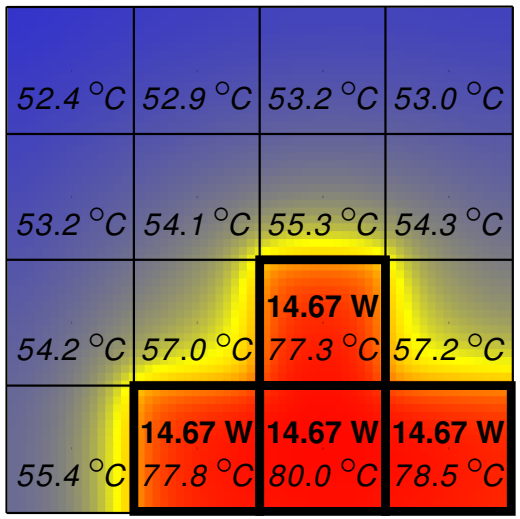


Highest Temperature: 76.1°C



Highest Temperature: 75.4°C



Highest Temperature: 80.0°C

TSP for the Worst-Case Mappings

For m active cores:

- All active cores consume $P_{\text{TSP}}^{\text{worst}}(m) \rightarrow$ **Highest** temperatures.
- The temperature on node i is:

$$T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b^{-1}{}_{i,j} \cdot q_j + P_{\text{inact}}^{\text{core}} \cdot \sum_{\forall j \in \mathbf{K}'} b^{-1}{}_{i,j} \, (1 - q_j) + \sum_{j=1}^{N} b^{-1}{}_{i,j} \left(p_j^{\text{blocks}} + T_{\text{amb}} \cdot g_j \right)$$

TSP for the Worst-Case Mappings

For m active cores:

- All active cores consume $P_{\text{TSP}}^{\text{worst}}(m) \rightarrow$ **Highest** temperatures.
- The temperature on node i is:

$$T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} \textbf{Depends on the mapping} + \sum_{j=1}^{N} \textbf{Constant for node } i$$

TSP for the Worst-Case Mappings

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- Naive algorithm: Brute force.

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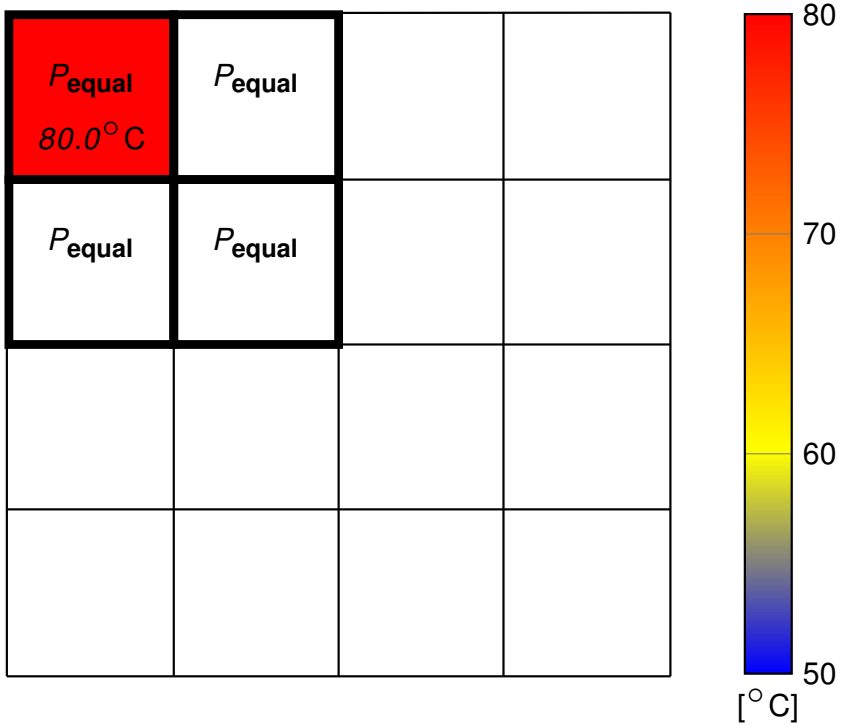
- Naive algorithm: Brute force.
- Our algorithm: **Polynomial Time** $\rightarrow$ For every node i
  - Set $T_i = T_{\text{DTM}}$.
  - Worst-case mapping for node $i \rightarrow$ Compute P_{equal} .
  - $P_{\text{TSP}}^{\text{worst}}(m) \leftarrow$ Minimum P_{equal}.

TSP for the Worst-Case Mappings

Example for 4 active cores:

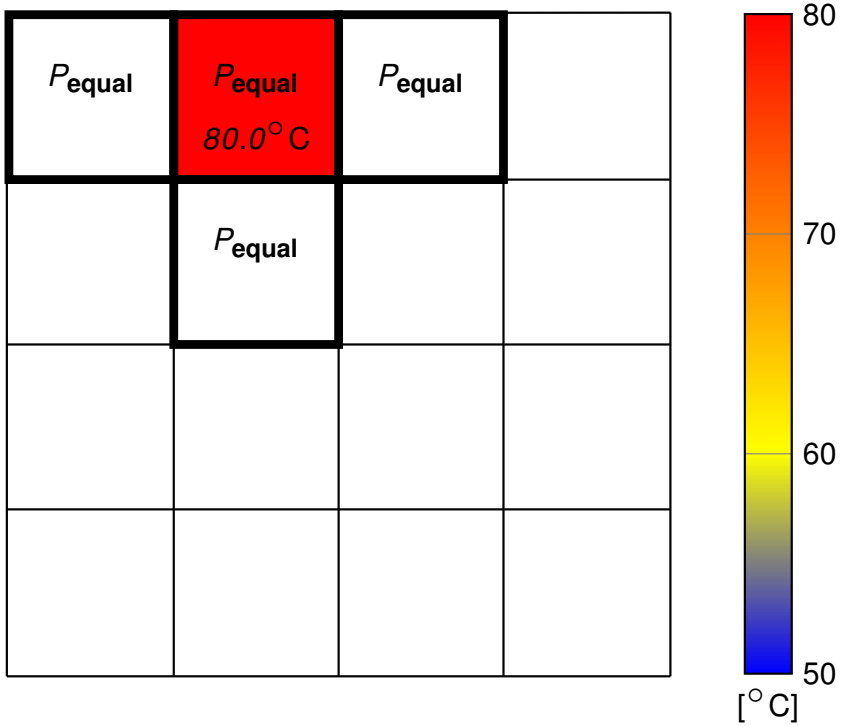


$$T_1 = 80.0^\circ C \rightarrow P_{equal} = 14.77W$$

$$P_{TSP}^{worst}(4) = 14.77W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

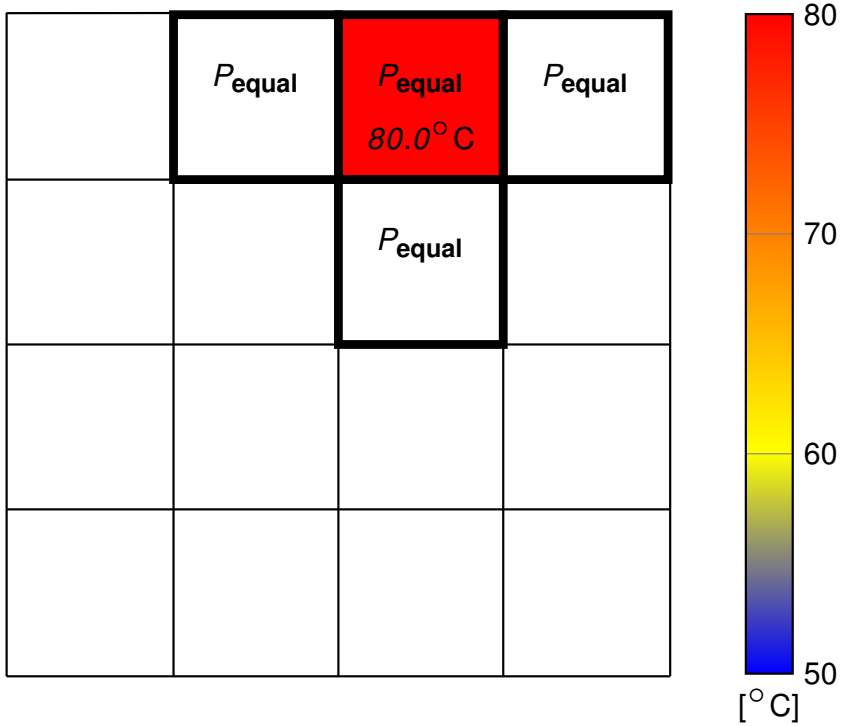


$$T_2 = 80.0^\circ C \rightarrow P_{equal} = 14.67W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

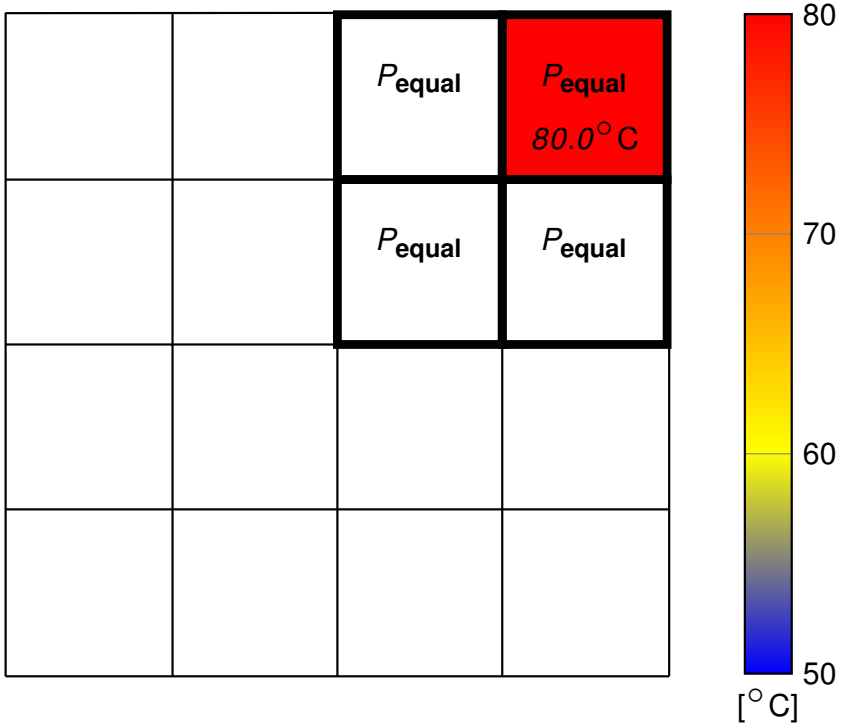


$$T_3 = 80.0^{\circ}C \rightarrow P_{equal} = 14.67W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

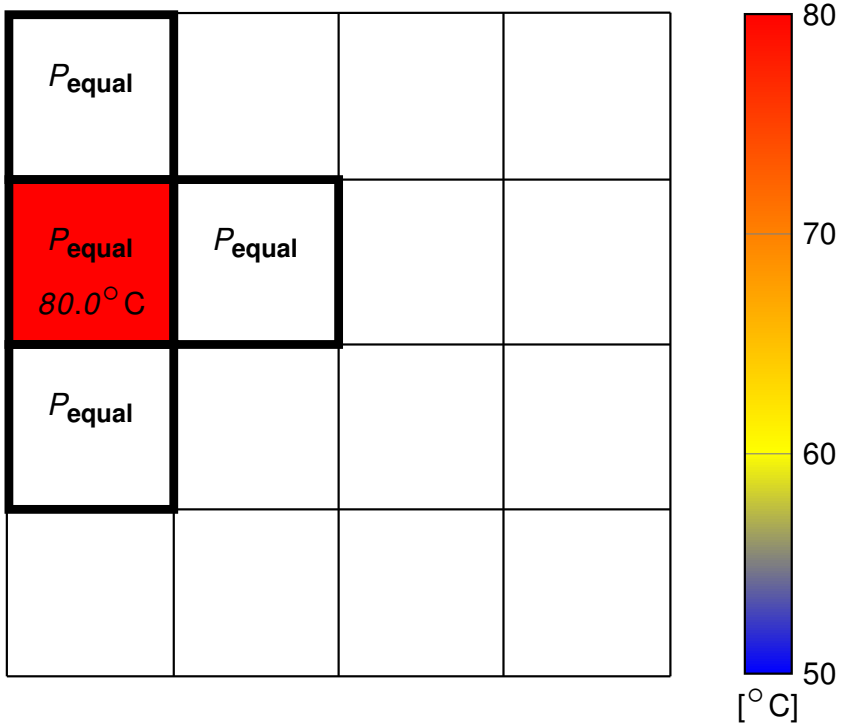


$$T_4 = 80.0^{\circ}C \rightarrow P_{equal} = 14.77W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

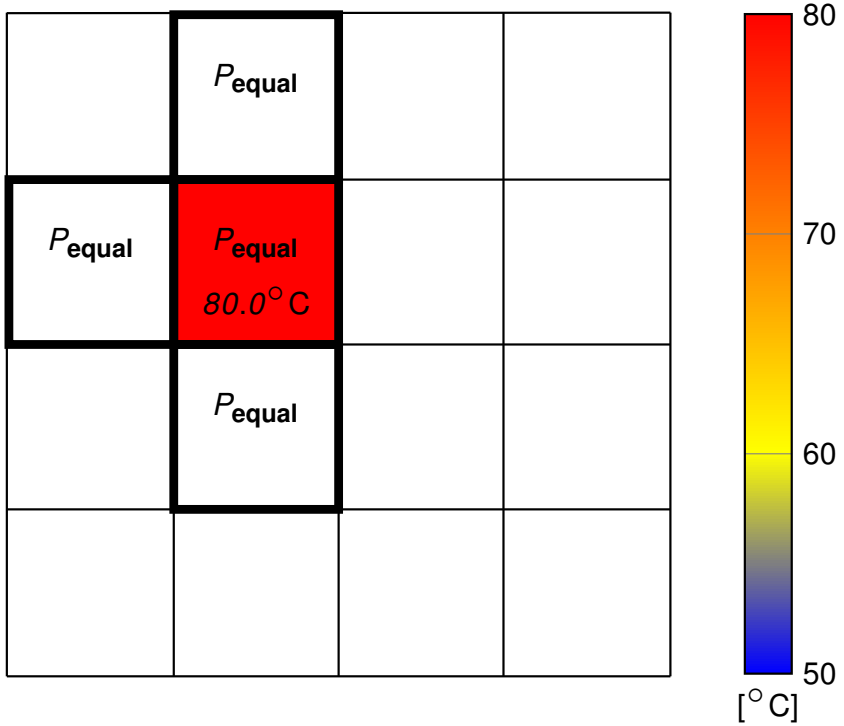


$$T_5 = 80.0^{\circ}C \rightarrow P_{equal} = 14.67W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

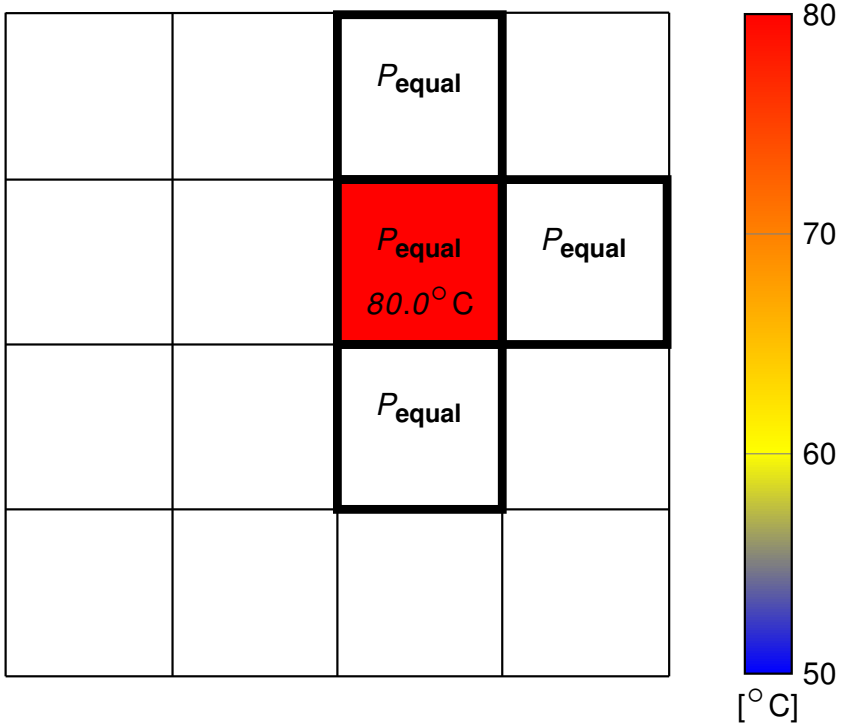


$$T_6 = 80.0^{\circ}C \rightarrow P_{equal} = 15.07W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

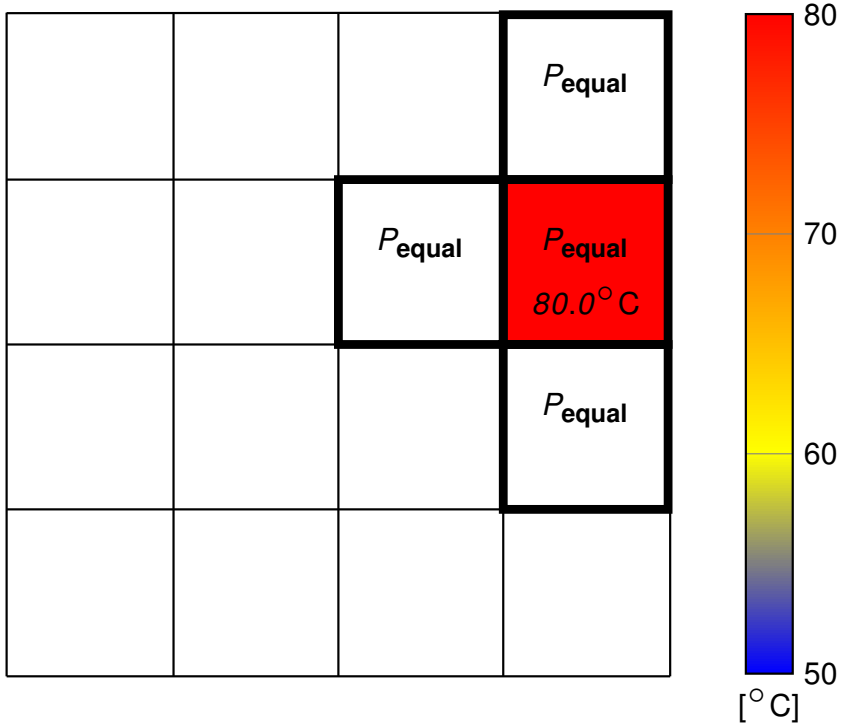


$$T_7 = 80.0^{\circ}C \rightarrow P_{\text{equal}} = 15.07W$$

$$P_{\text{TSP}}^{\text{worst}}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

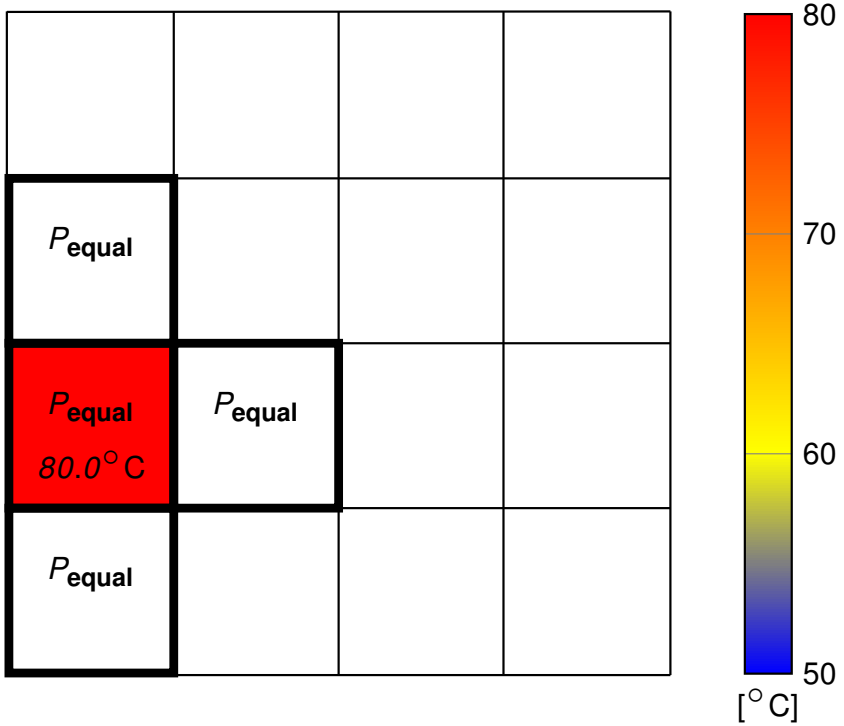


$$T_8 = 80.0^{\circ}C \rightarrow P_{equal} = 14.67W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

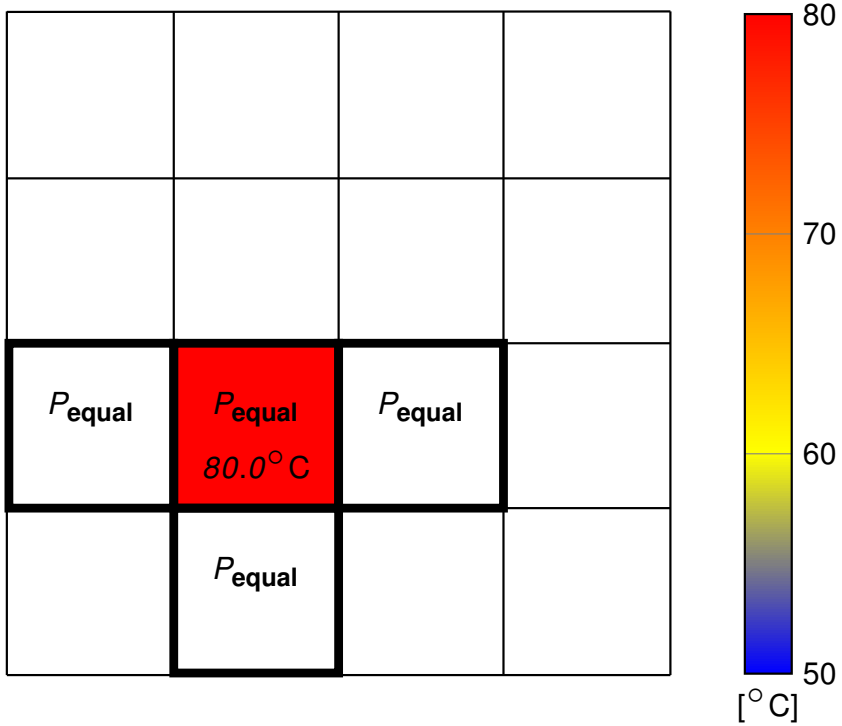


$$T_9 = 80.0^{\circ}C \rightarrow P_{equal} = 14.67W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

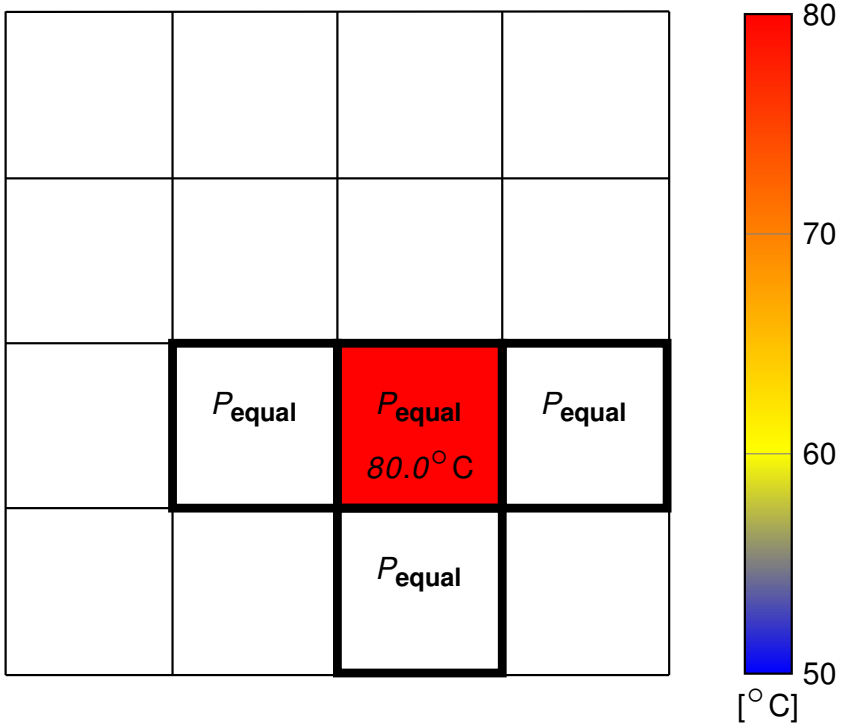


$$T_{10} = 80.0^{\circ}C \rightarrow P_{equal} = 15.07W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

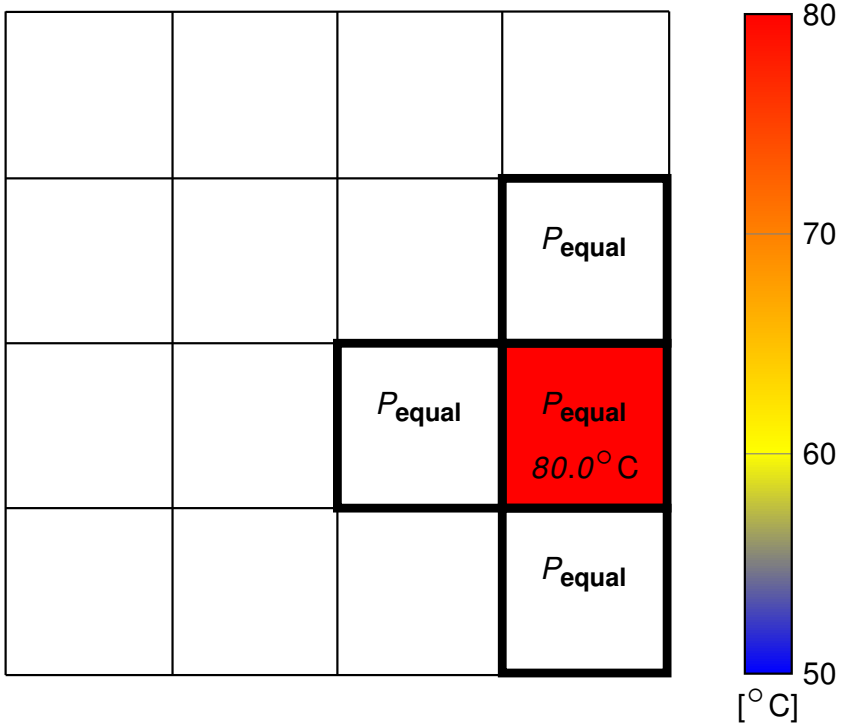


$$T_{11} = 80.0^{\circ}C \rightarrow P_{equal} = 15.07W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:

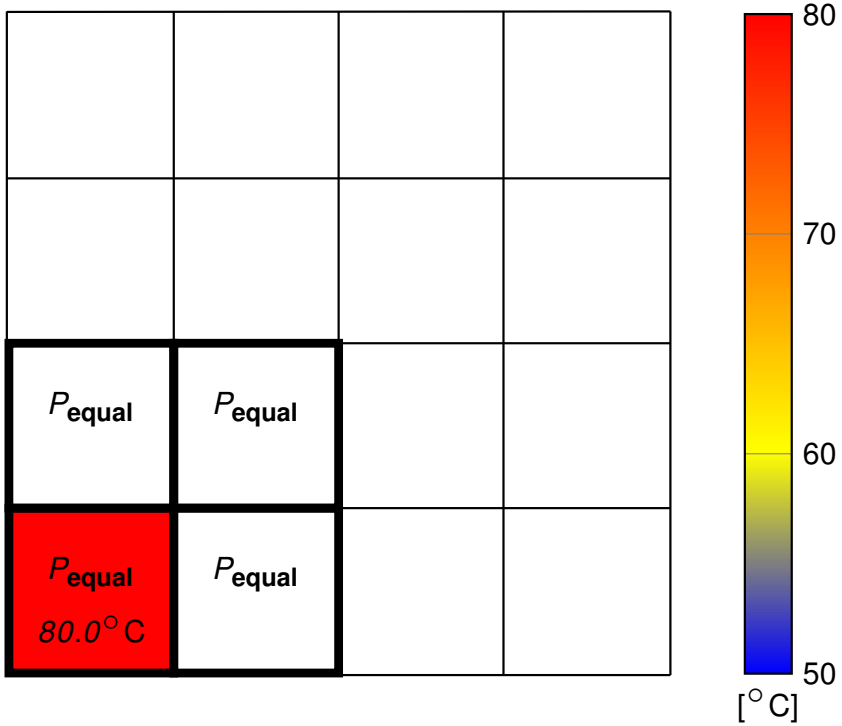


$$T_{12} = 80.0^{\circ}C \rightarrow P_{equal} = 14.67W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

TSP for the Worst-Case Mappings

Example for 4 active cores:



$$T_{13} = 80.0^{\circ}C \rightarrow P_{equal} = 14.77W$$

$$P_{TSP}^{worst}(4) = 14.67W$$

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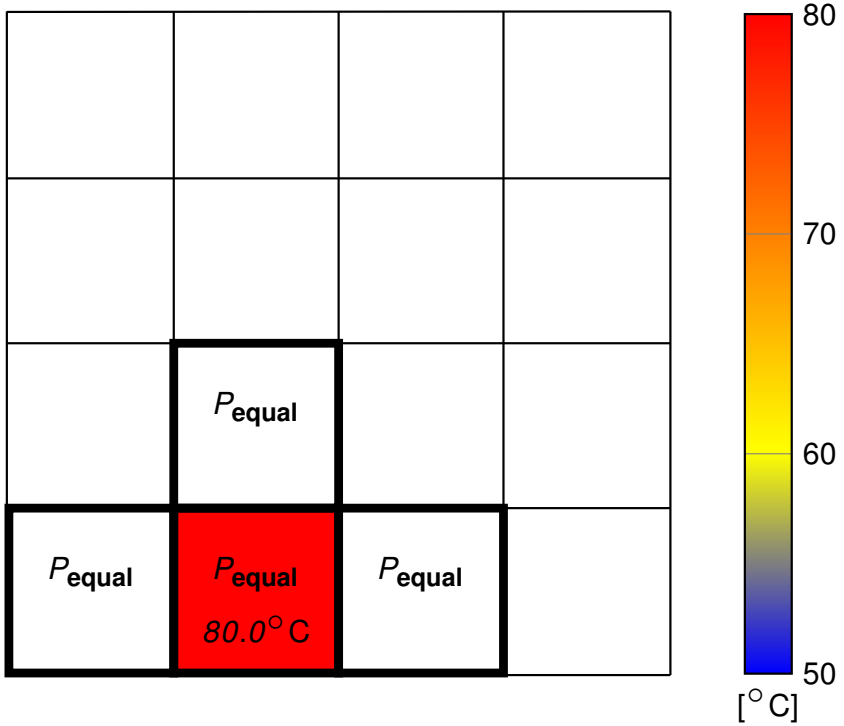

$$T_{14} = 80.0^{\circ}C \rightarrow P_{equal} = 14.67W$$

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TSP for the Worst-Case Mappings

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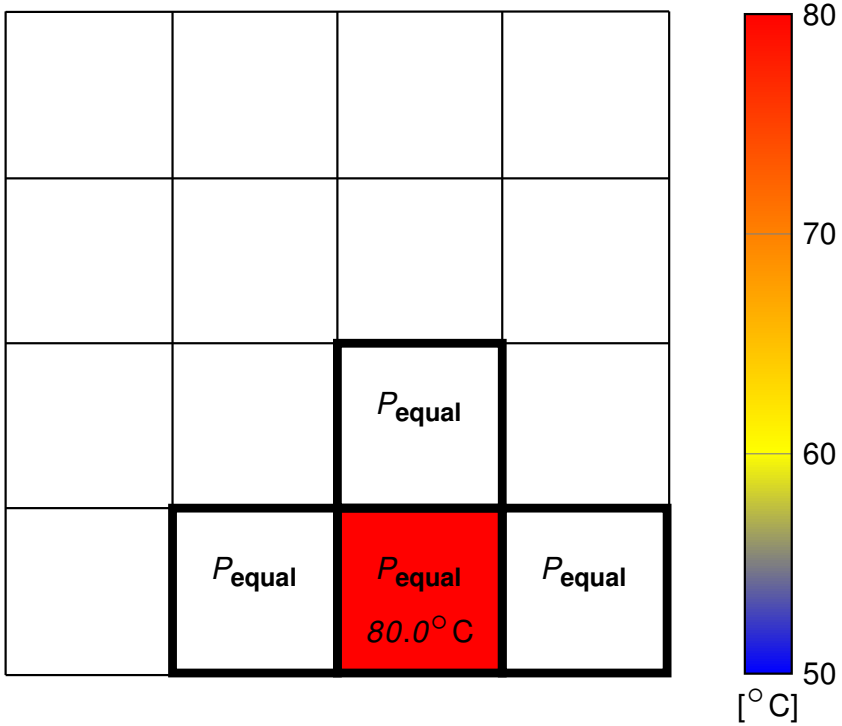

$$T_{15} = 80.0^{\circ}C \rightarrow P_{equal} = 14.67W$$

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TSP for the Worst-Case Mappings

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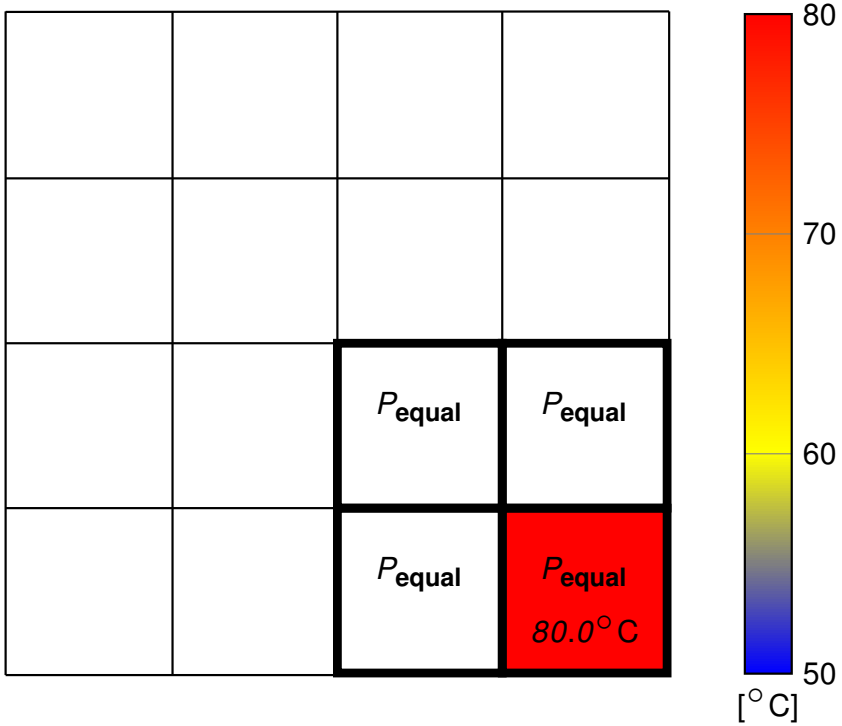

$$T_{16} = 80.0^{\circ}C \rightarrow P_{equal} = 14.77W$$

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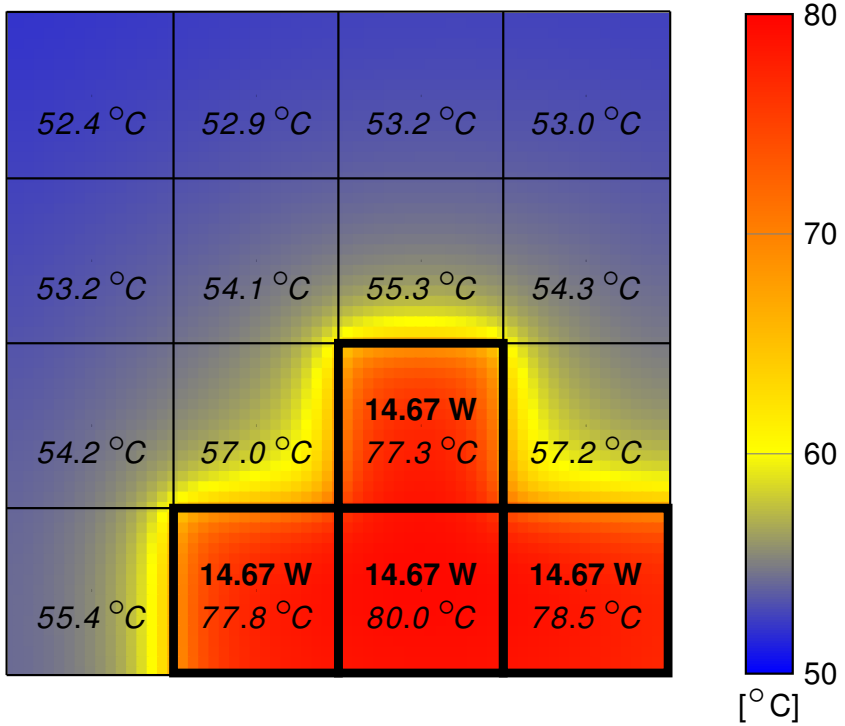

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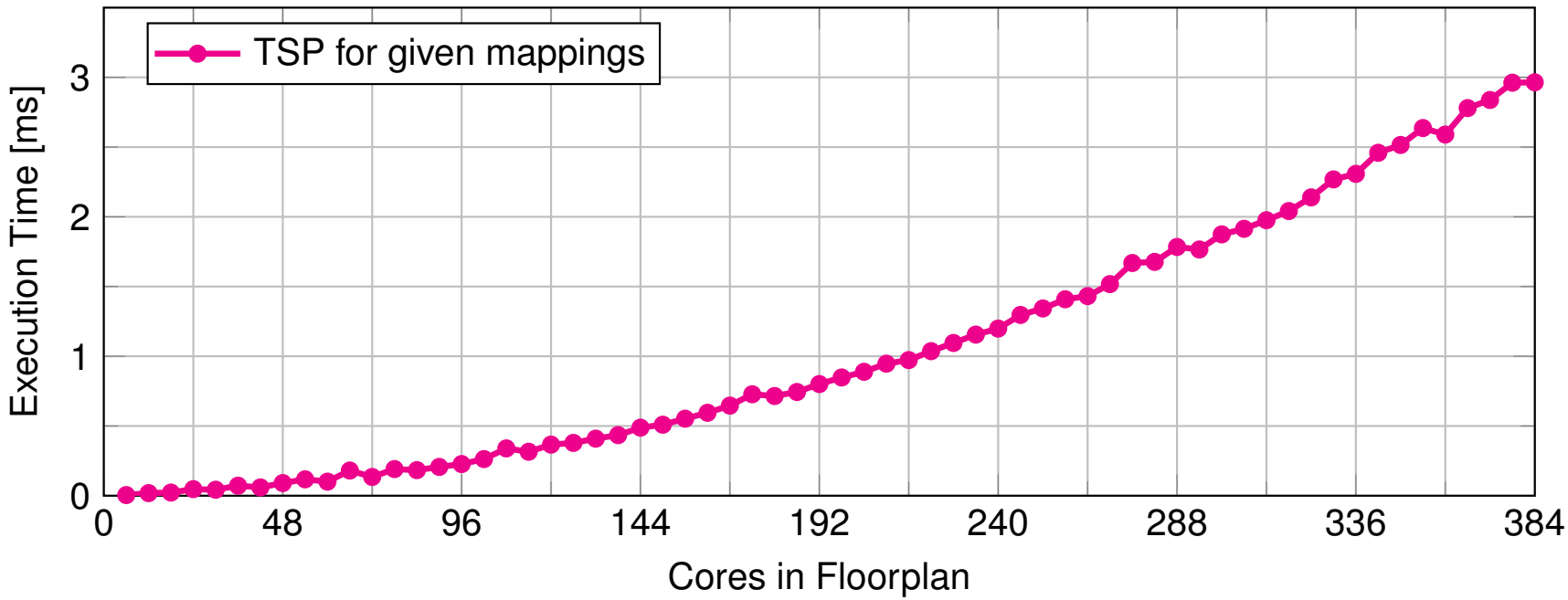
Polynomial time complexity

Outline

- Introduction and State-of-the-art
- Motivation
- Objective and Contributions
- System Model
- Thermal Safe Power (TSP)
  - For Given Mappings
  - For the Worst-Case Mappings
- Evaluations
- Conclusions

Evaluations: Algorithm Execution Time

- TSP for given mappings algorithm.
- On a desktop computer running at 3.10GHz.
- Different numbers of cores.
- 25000 random mappings for every case.



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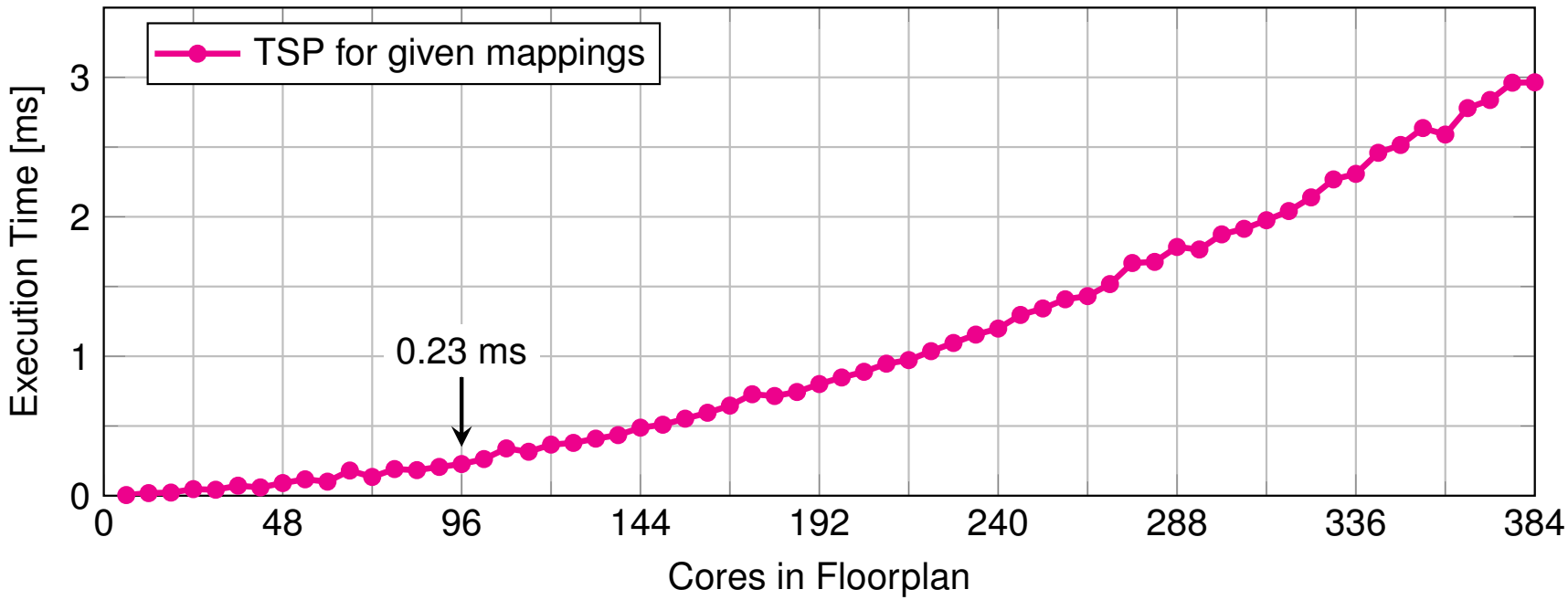

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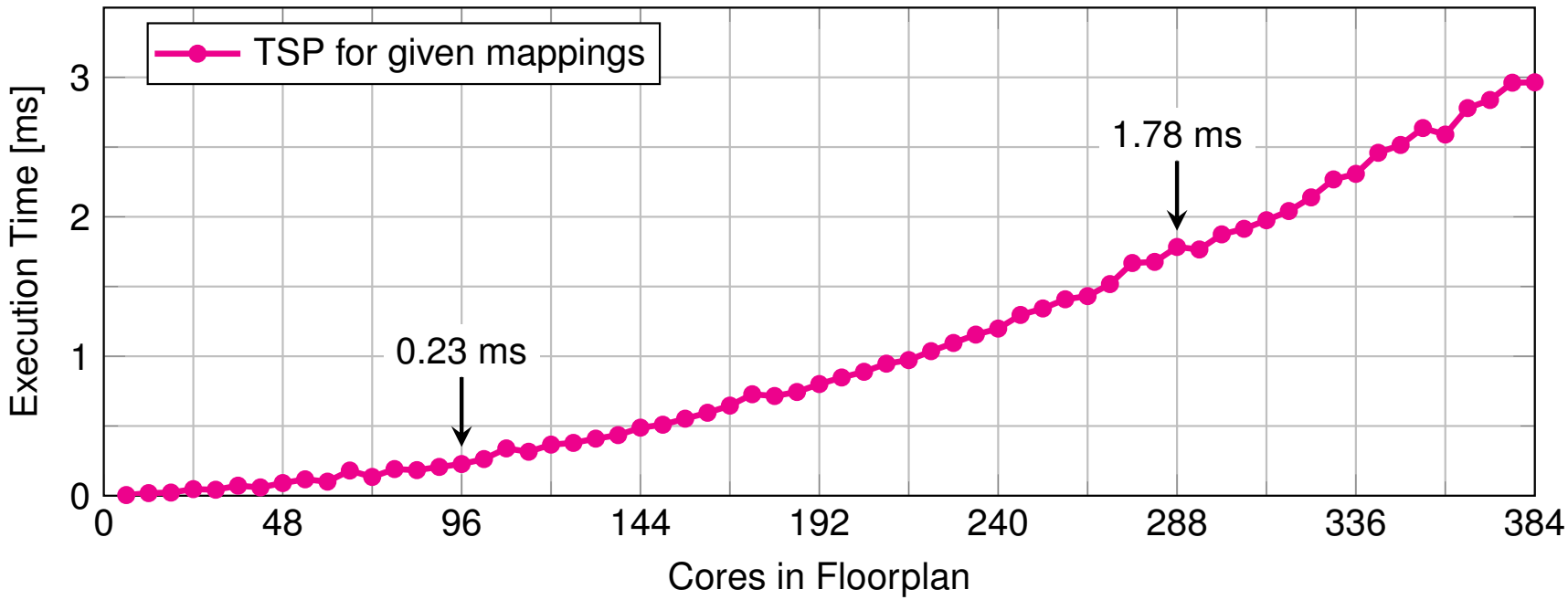

Evaluations: Setup

- 64 core system:
  - *Out-of-order* Alpha 21264 cores in 22 nm.
  - Area of 9.6mm^2 $\rightarrow$ From simulations on **gem5** and **McPAT**.
- Every 4 cores $\rightarrow$ Shared L2 cache and memory controller:
  - Combined area of 4.7mm^2.
- Available frequencies: 0.1 GHz, 0.2 GHz, . . . , 4.0 GHz.
- RC thermal network: $\mathbf{B}^{-1}$ and $\mathbf{G}$ $\rightarrow$ From **HotSpot**.
- **DTM:**
  - Similar to a mode of Intel Xeon 5100 and Intel Xeon 7500.
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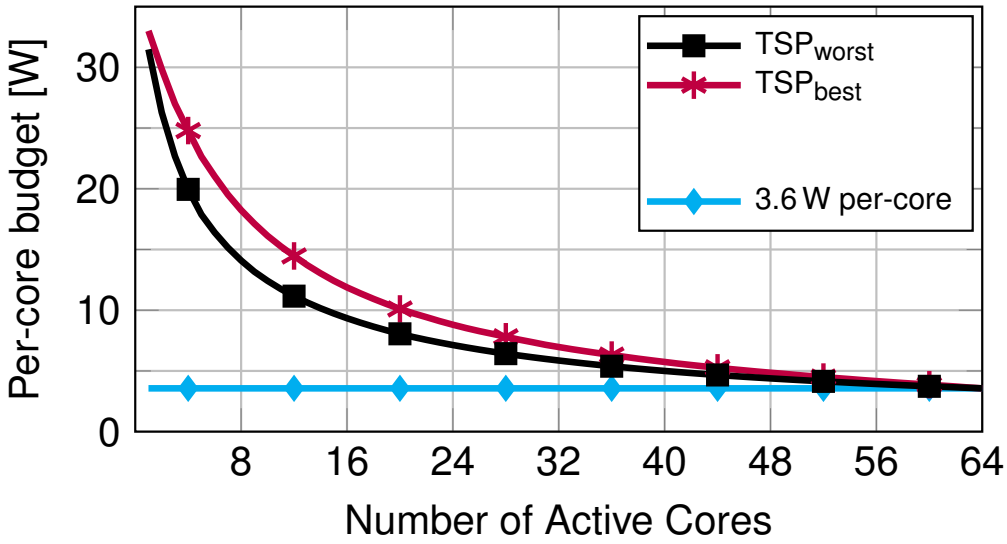
Evaluations: Hotspot Configuration

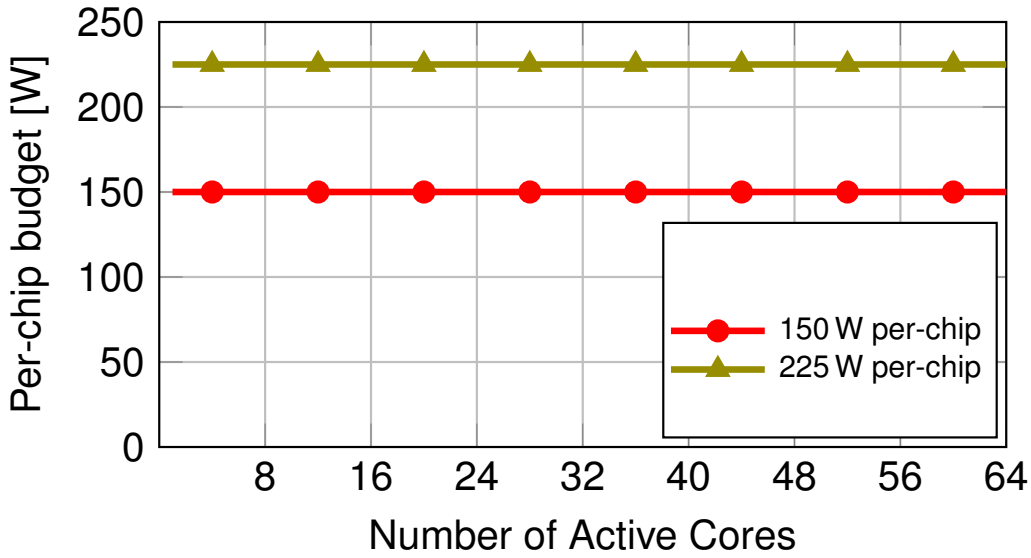
- Chip thickness: 0.15 *mm*
- Silicon thermal conductivity: $100 \frac{W}{m \cdot K}$
- Silicon specific heat: $1.75 \cdot 10^6 \frac{J}{m^3 \cdot K}$
- Heat spreader: 3 *cm* $\times$ 3 *cm*, and 1 *mm* thick
- Heat sink: 6 *cm* $\times$ 6 *cm*, and 6.9 *mm* thick
- Heat sink convection capacitance: $140.4 \frac{J}{K}$
- Heat sink convection resistance: $0.1 \frac{K}{W}$
- Heat sink and heat spreader thermal conductivity: $400 \frac{W}{m \cdot K}$
- Heat sink and heat spreader specific heat: $3.55 \cdot 10^6 \frac{J}{m^3 \cdot K}$
- Interface material thickness: 20 *um*
- Interface material thermal conductivity: $4 \frac{W}{m \cdot K}$
- Interface material specific heat: $4 \cdot 10^6 \frac{J}{m^3 \cdot K}$

Evaluations: Benchmarks

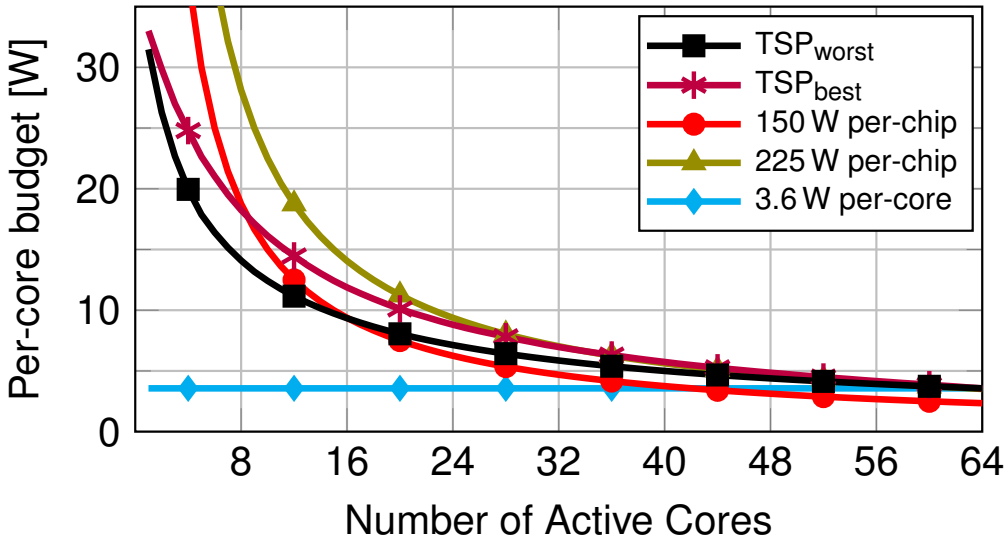
- Parsec benchmark suite:
  - H.264 video encoder.
  - Body Track.
  - Black-Scholes Partial Differential Equation option pricing.
  - Swaptions pricing.
- Threads:
  - 1, 2, 3, and 4 parallel dependent threads.

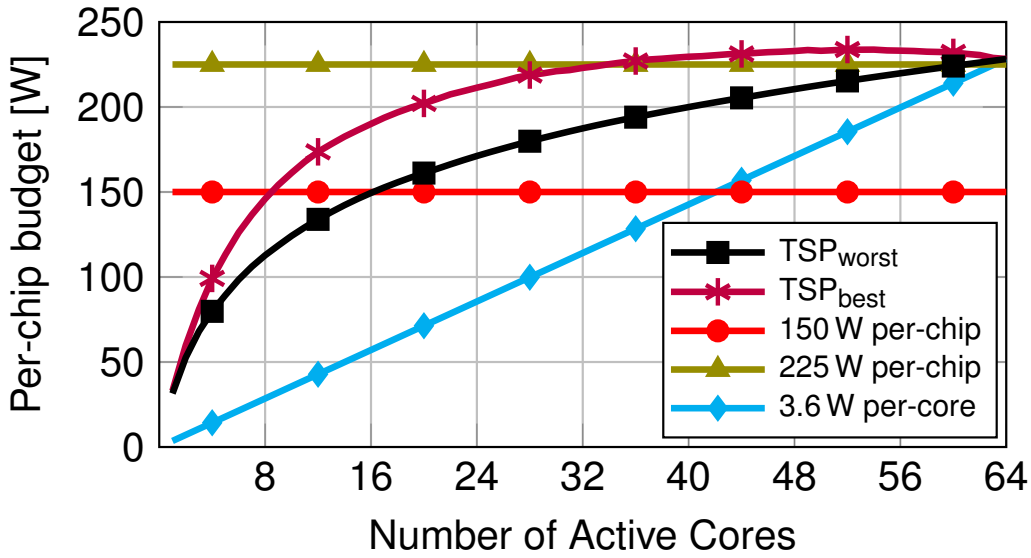
Evaluations: Power Constraints





Evaluations: Power Constraints





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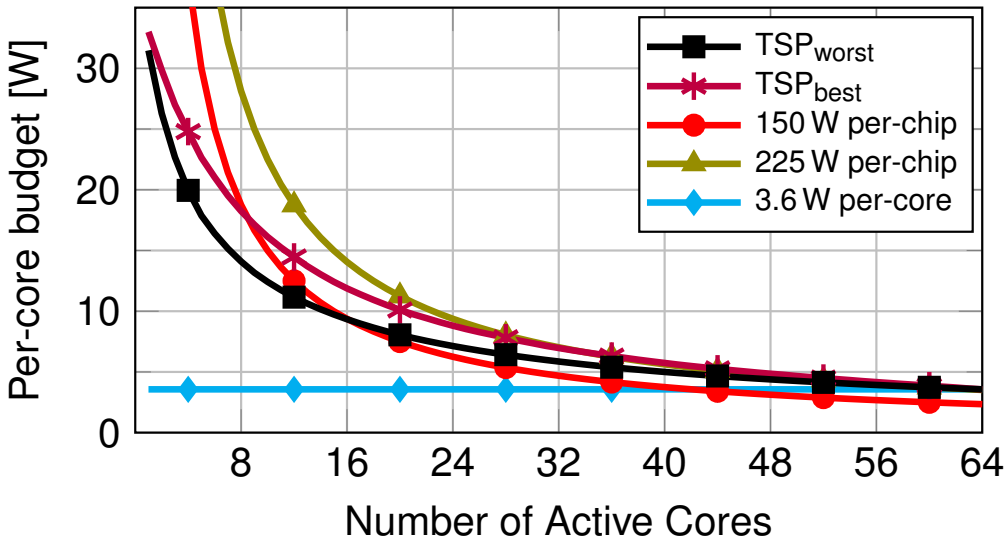
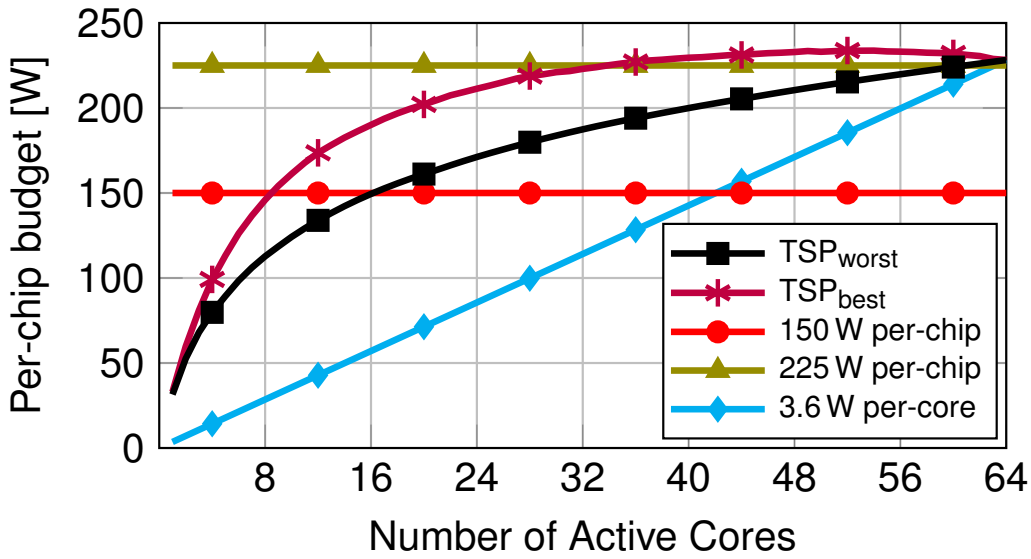
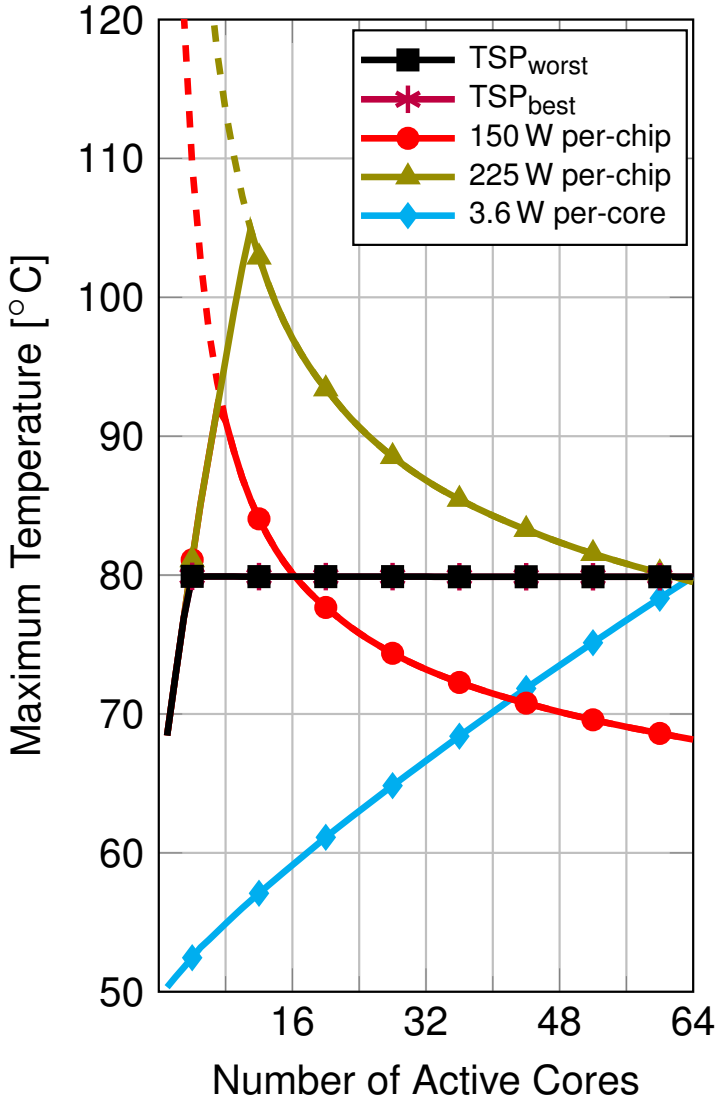


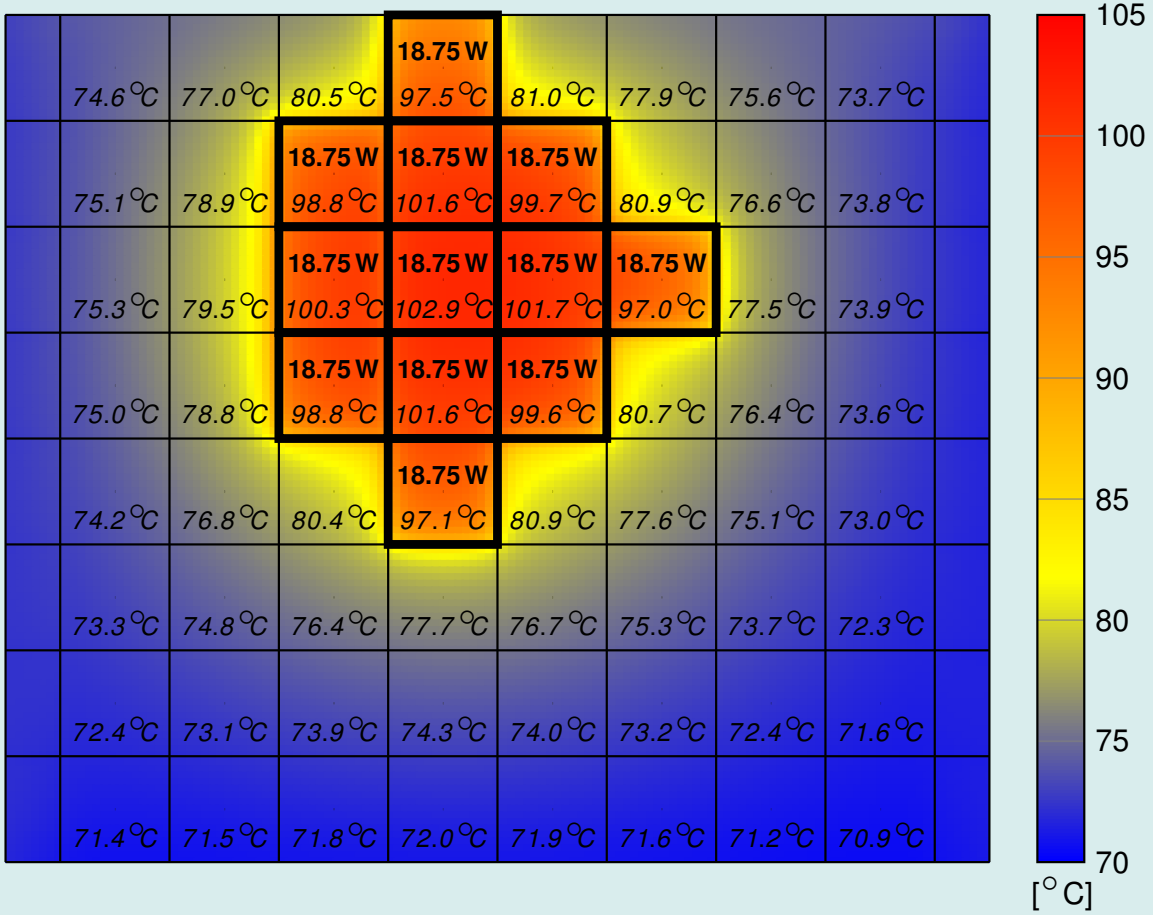


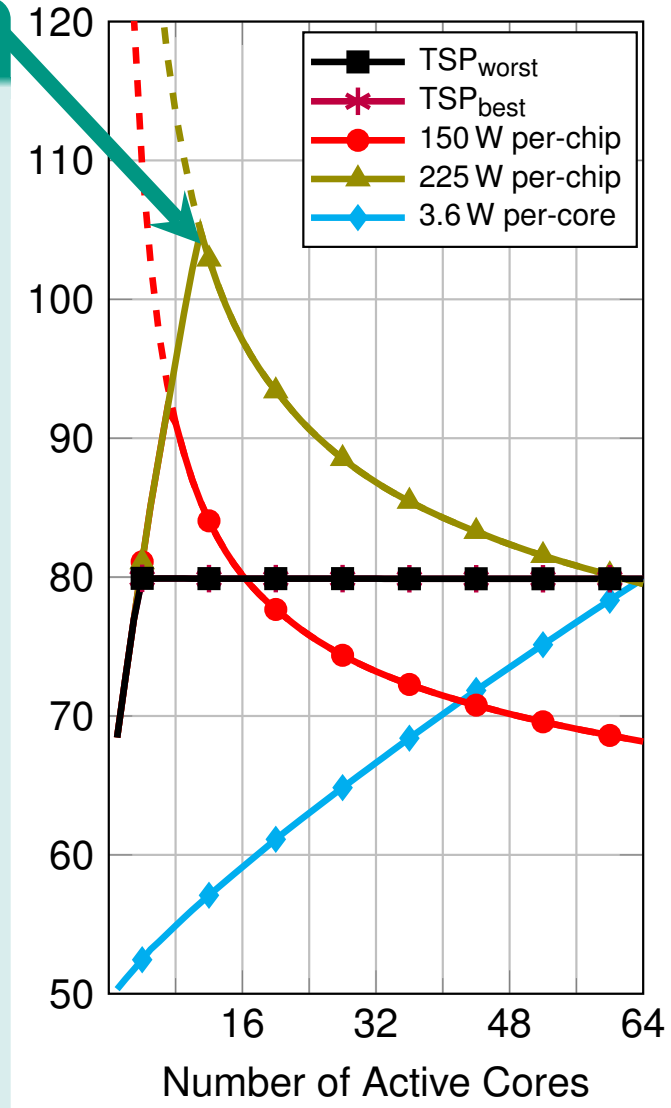


Evaluations: Power Constraints

Temperature distribution:

- 12 active cores (225 W per-chip).

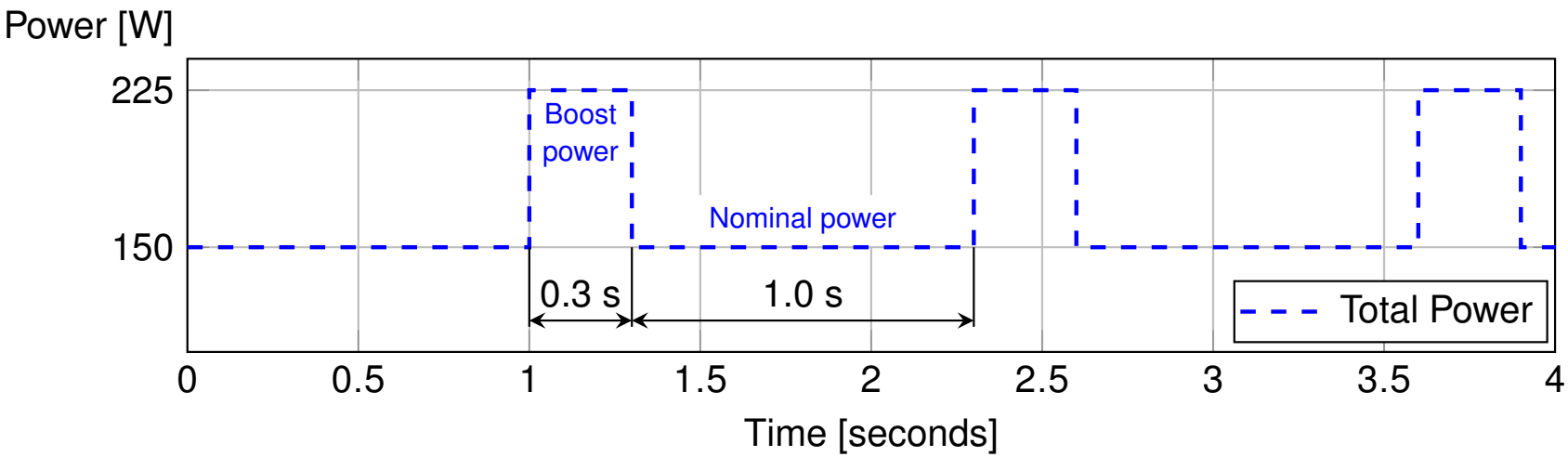




Evaluations: Power Constraints

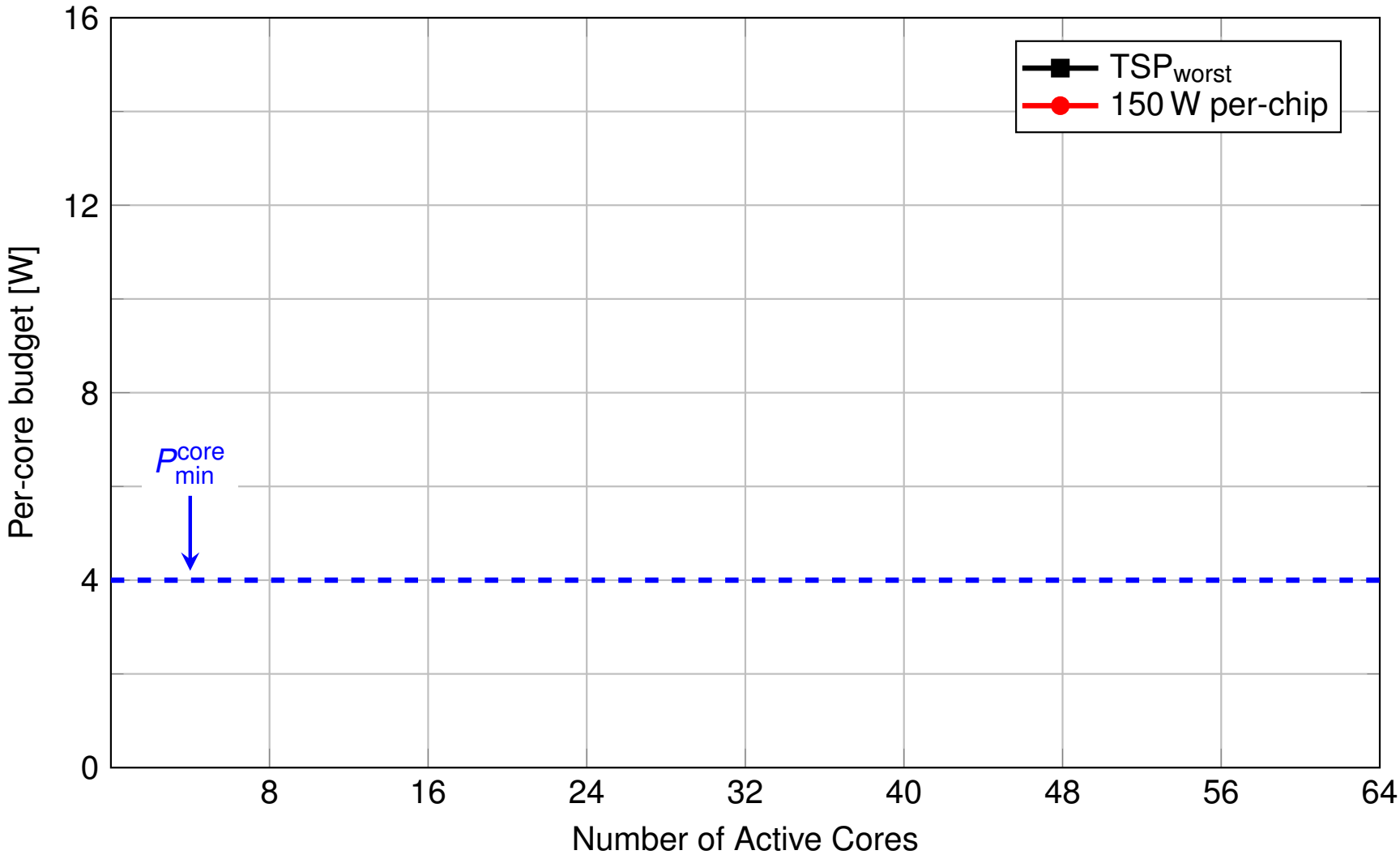
Boosting Technique (similar to a mode of Intel Xeon 5100):

- Nominal budget: 150 Watts per-chip.
- Boosting power: 225 Watts per-chip.
- Boosting interval: 0.3 seconds.
- Cool-down time: 1.0 second (at nominal power).



- If DTM is triggered at nominal power $\rightarrow$ no boosting.

Evaluations: Dark Silicon Estimations



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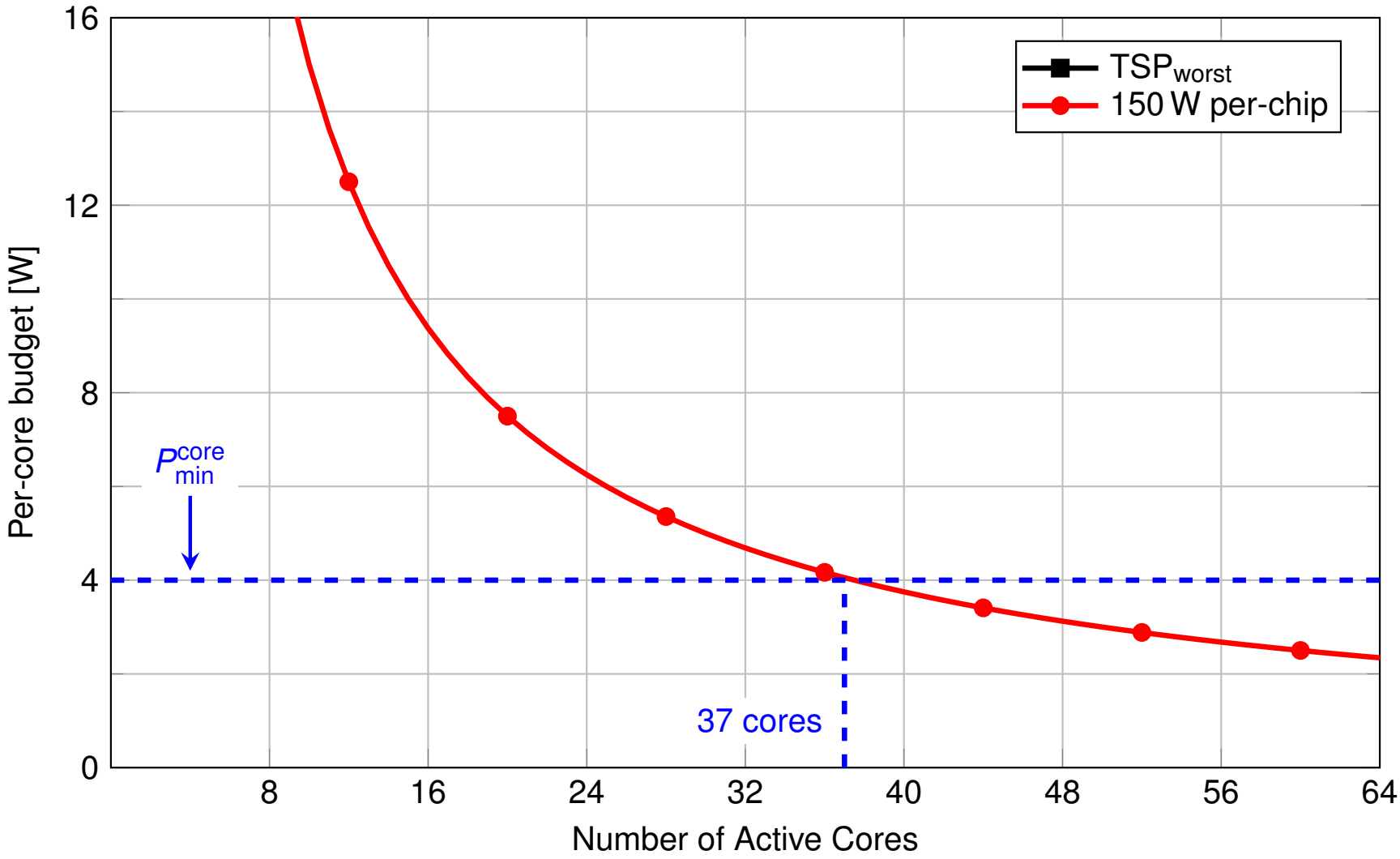

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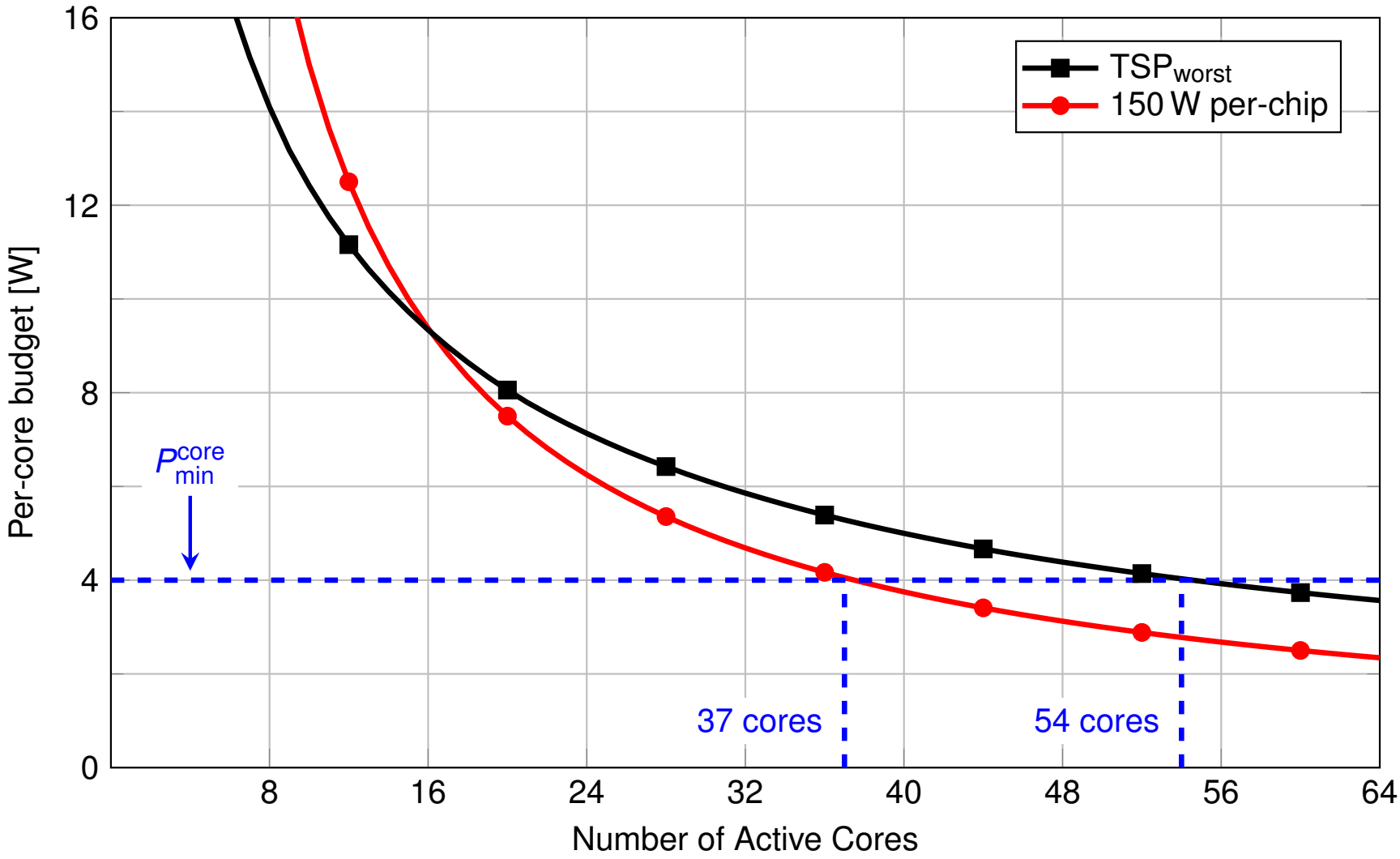

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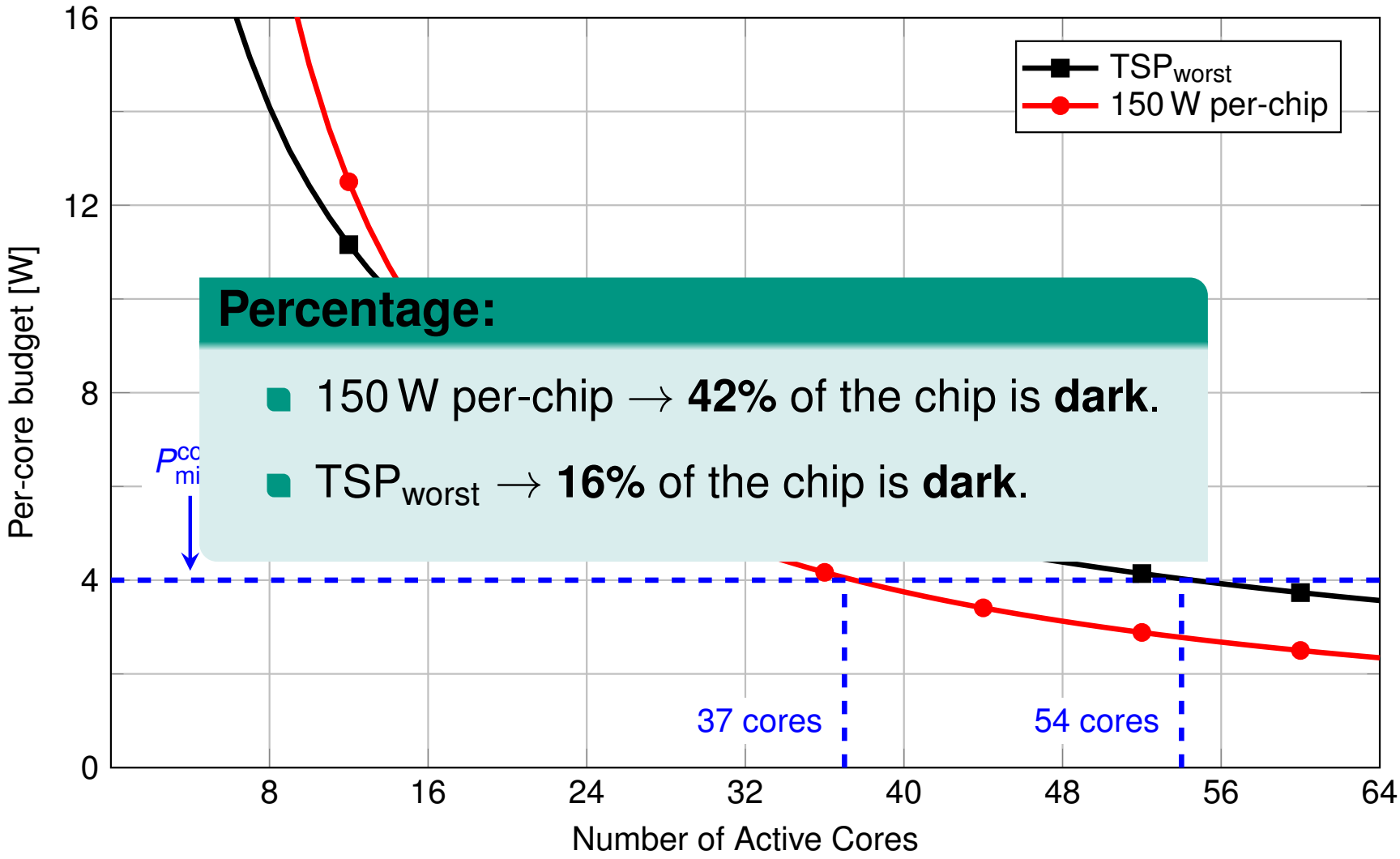
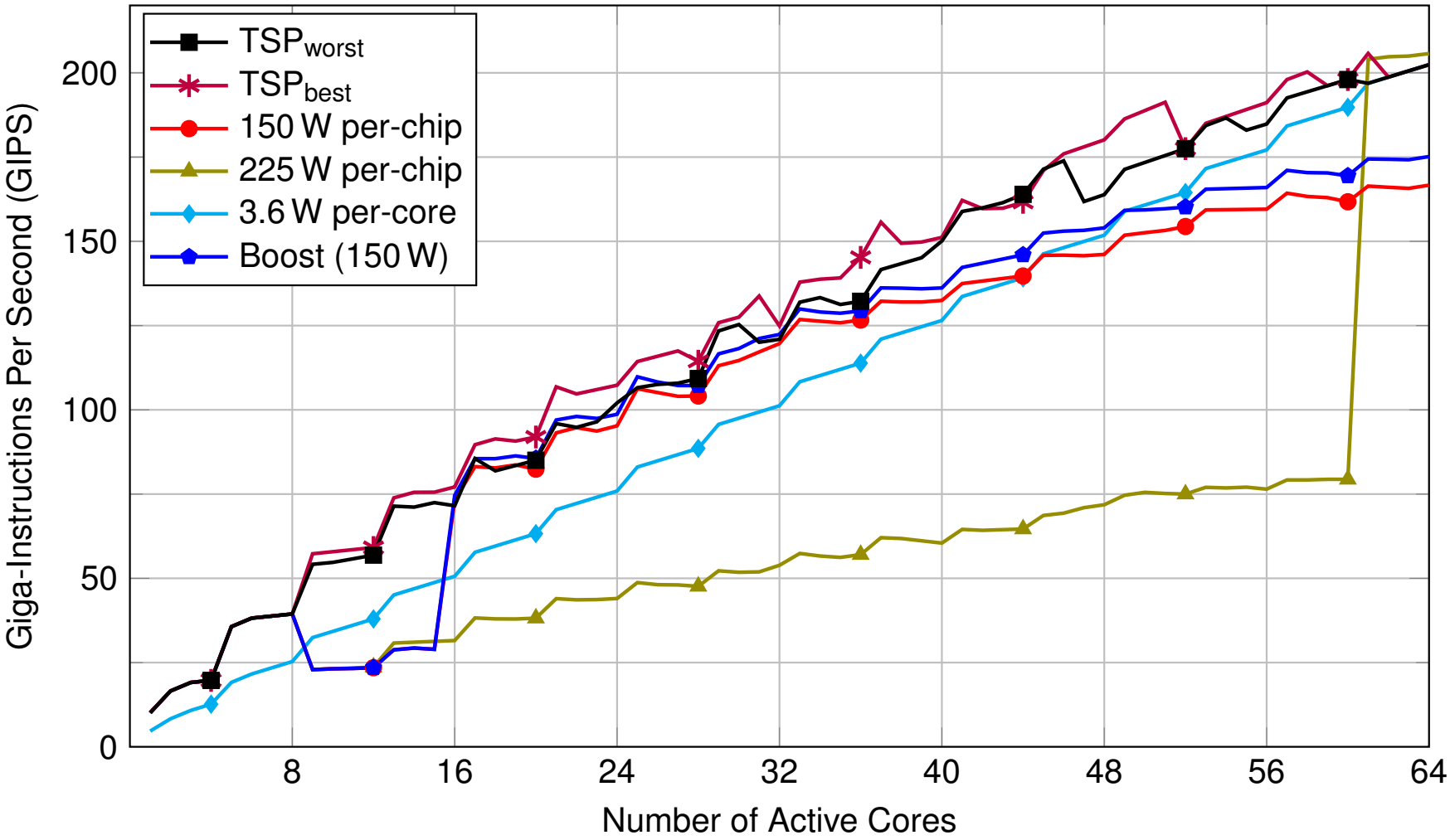


Evaluations: Performance

- H.264 video encoder:



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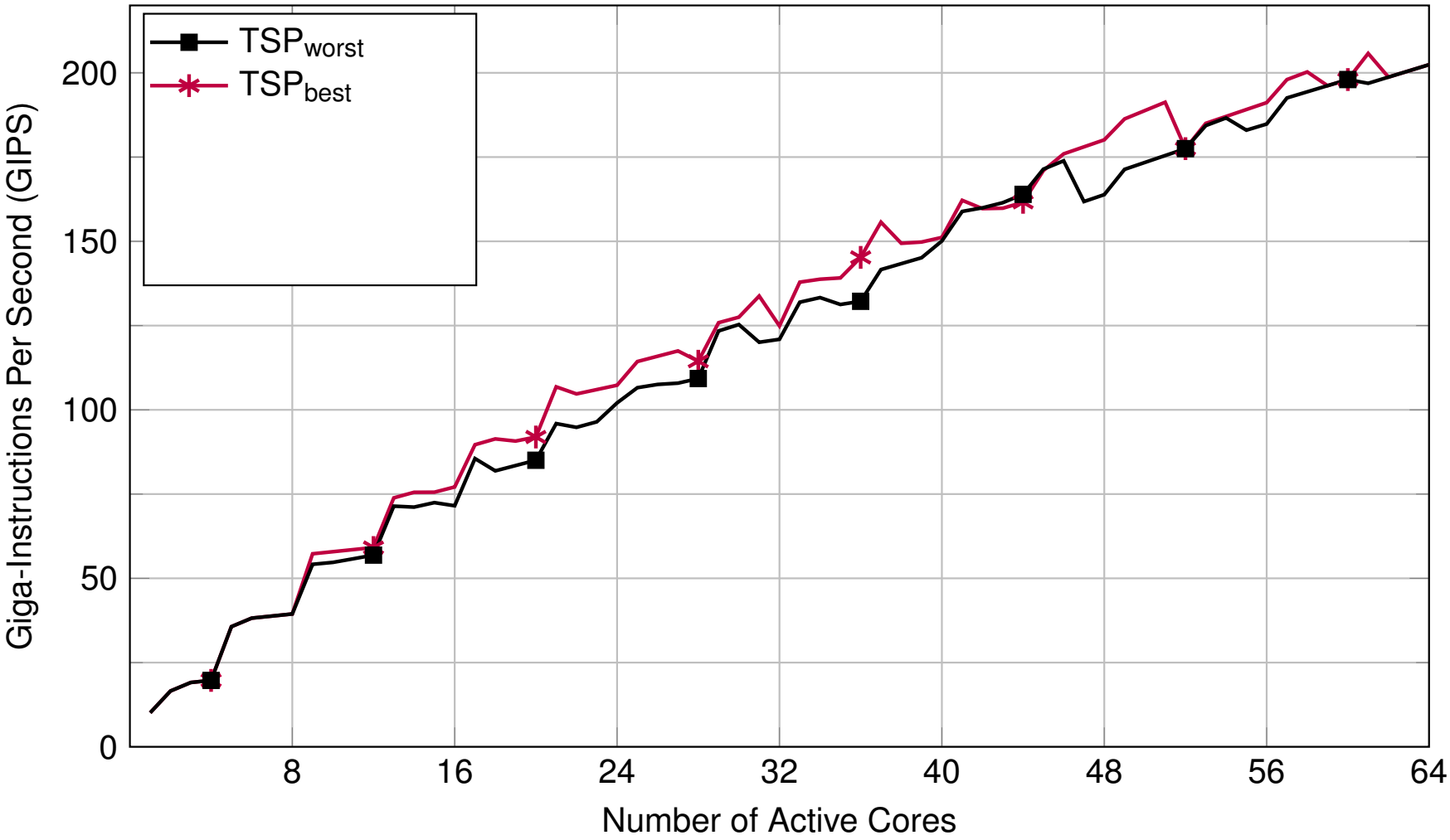

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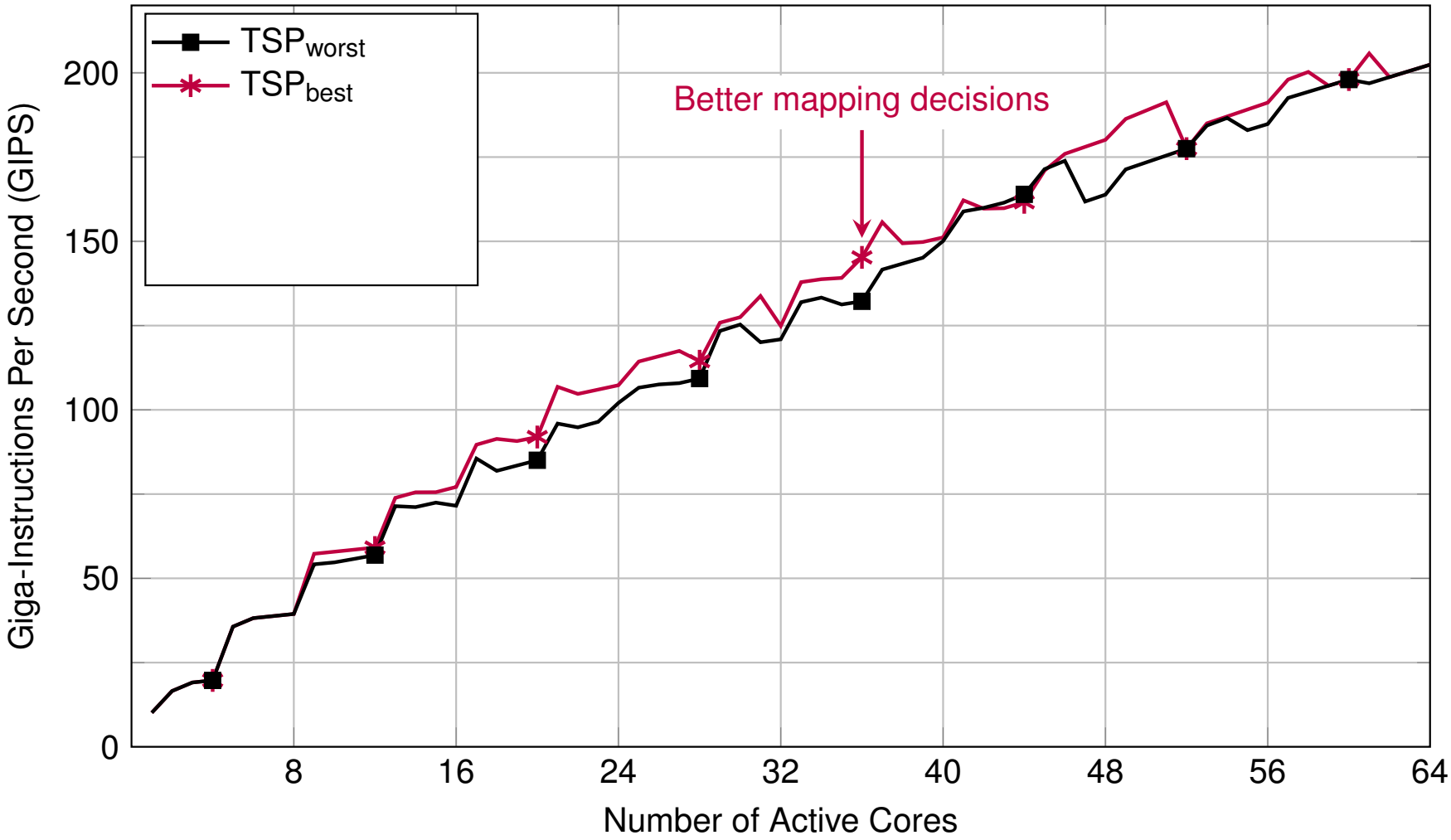

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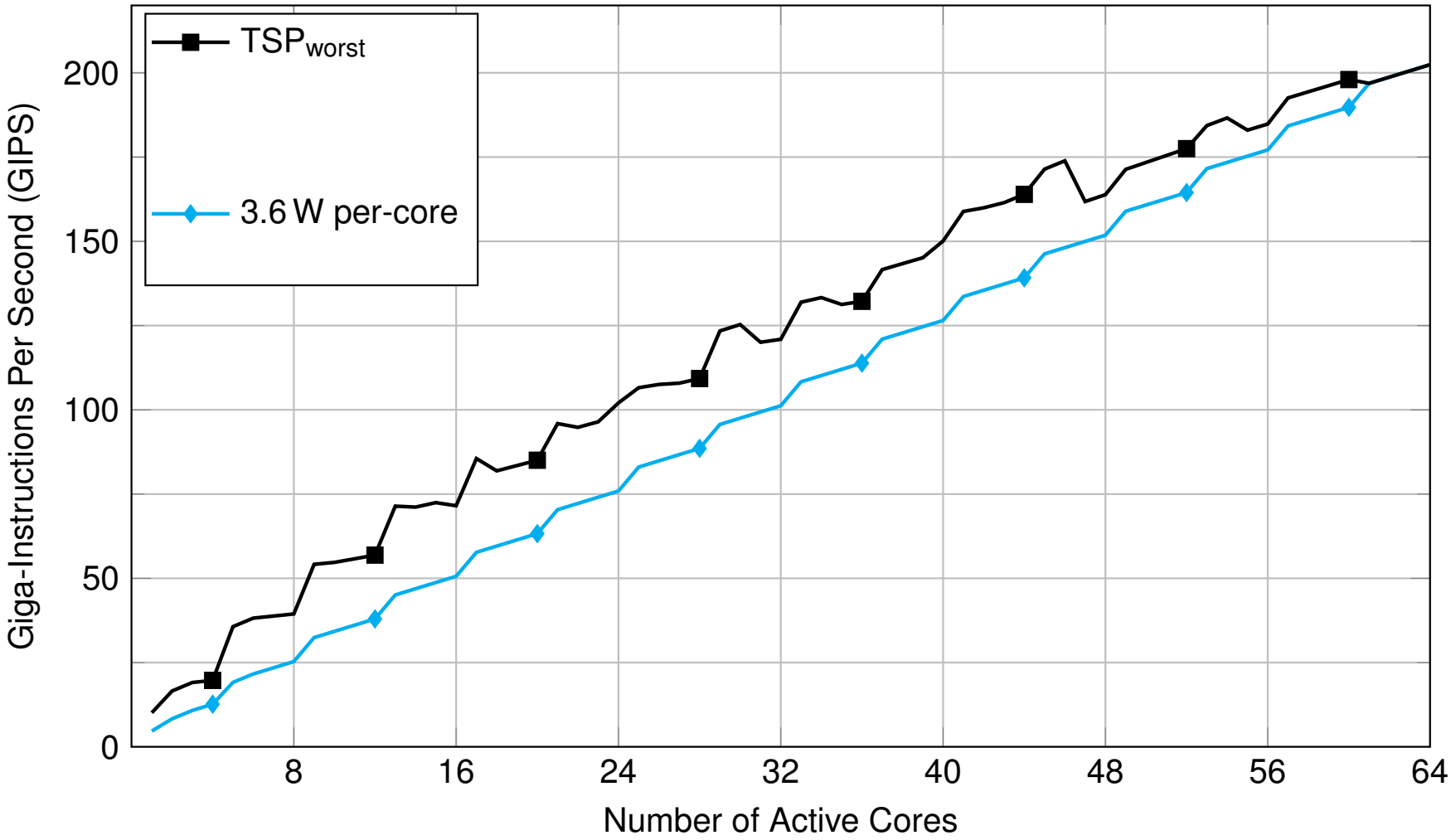

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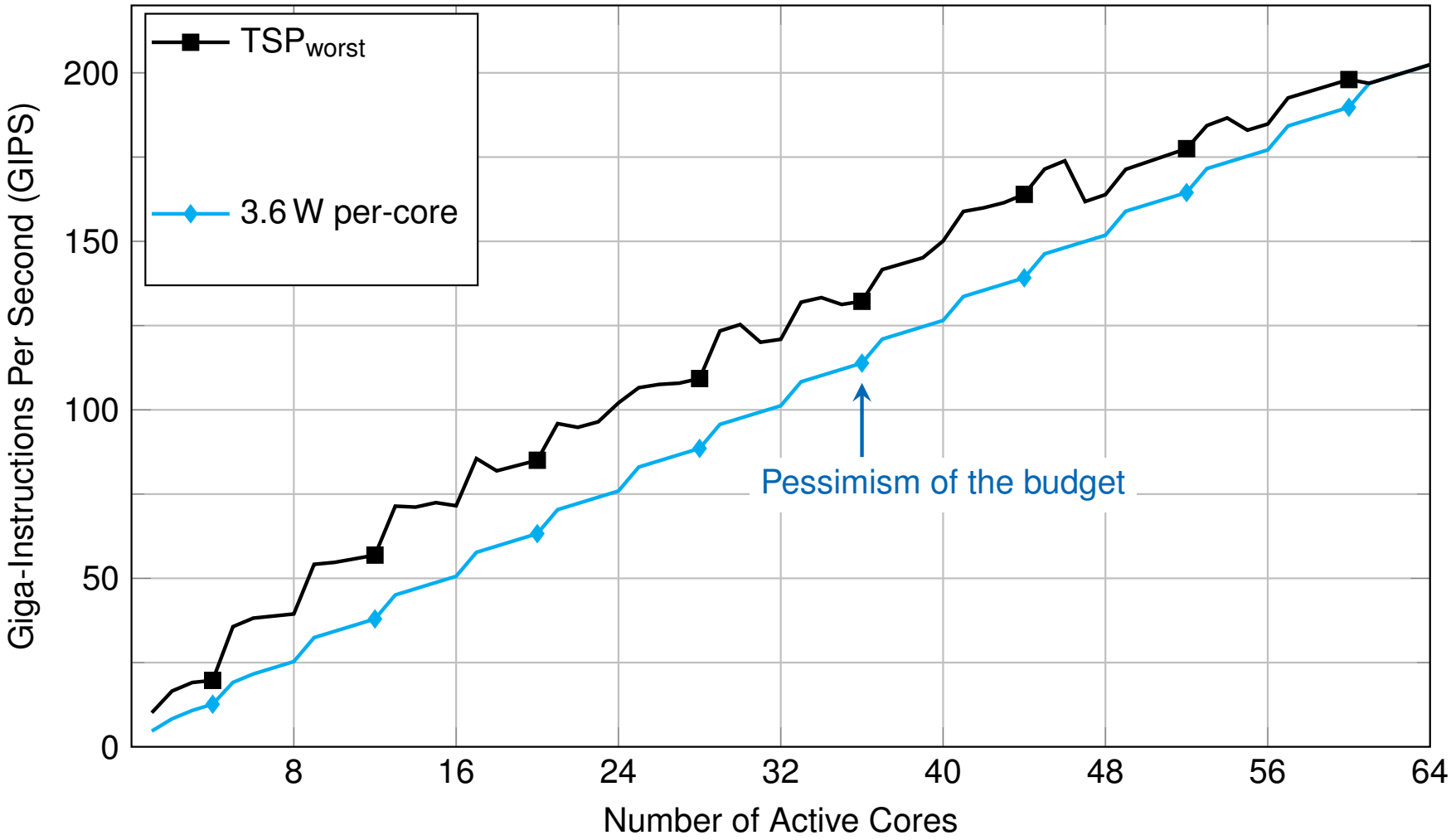

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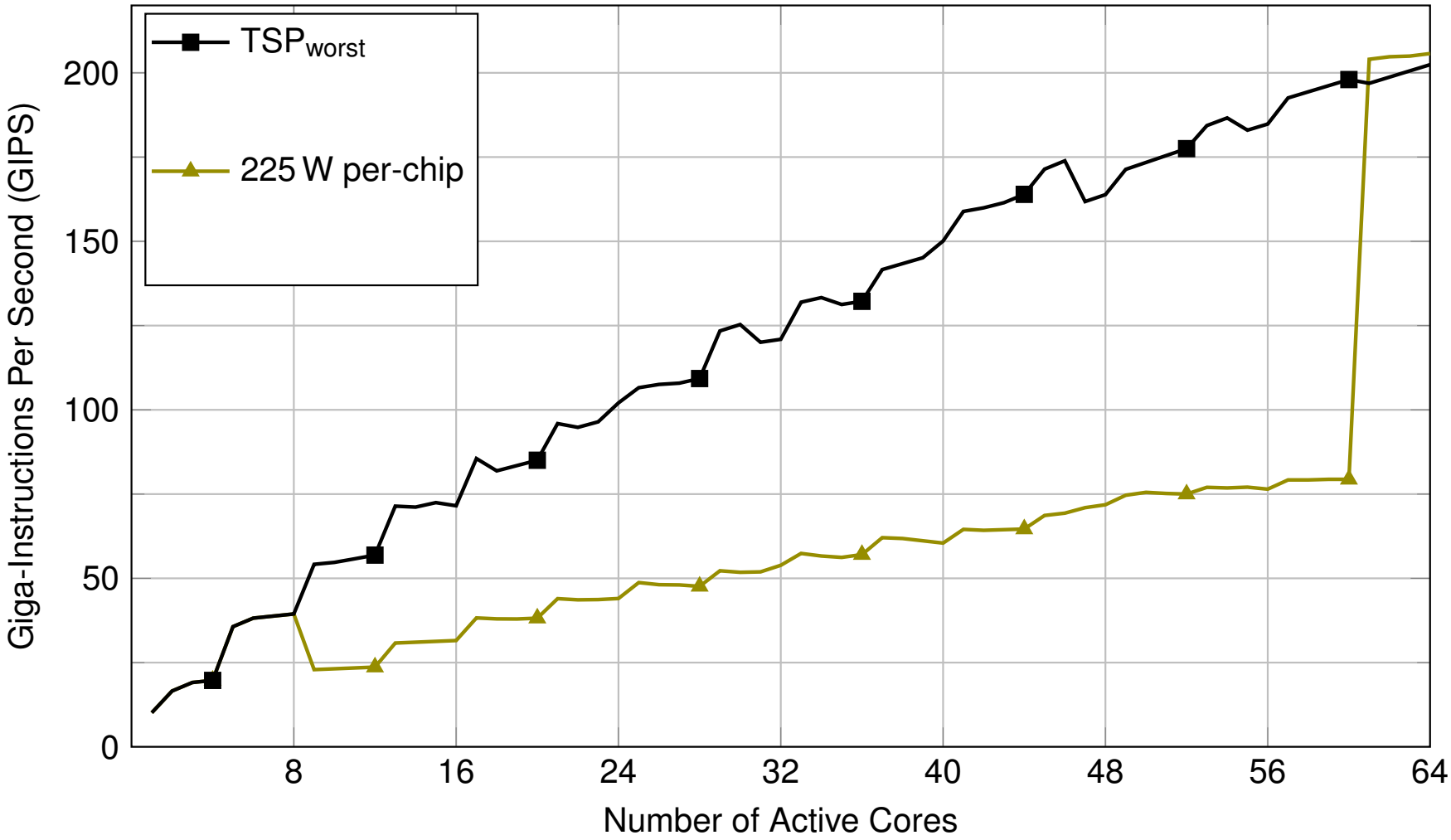

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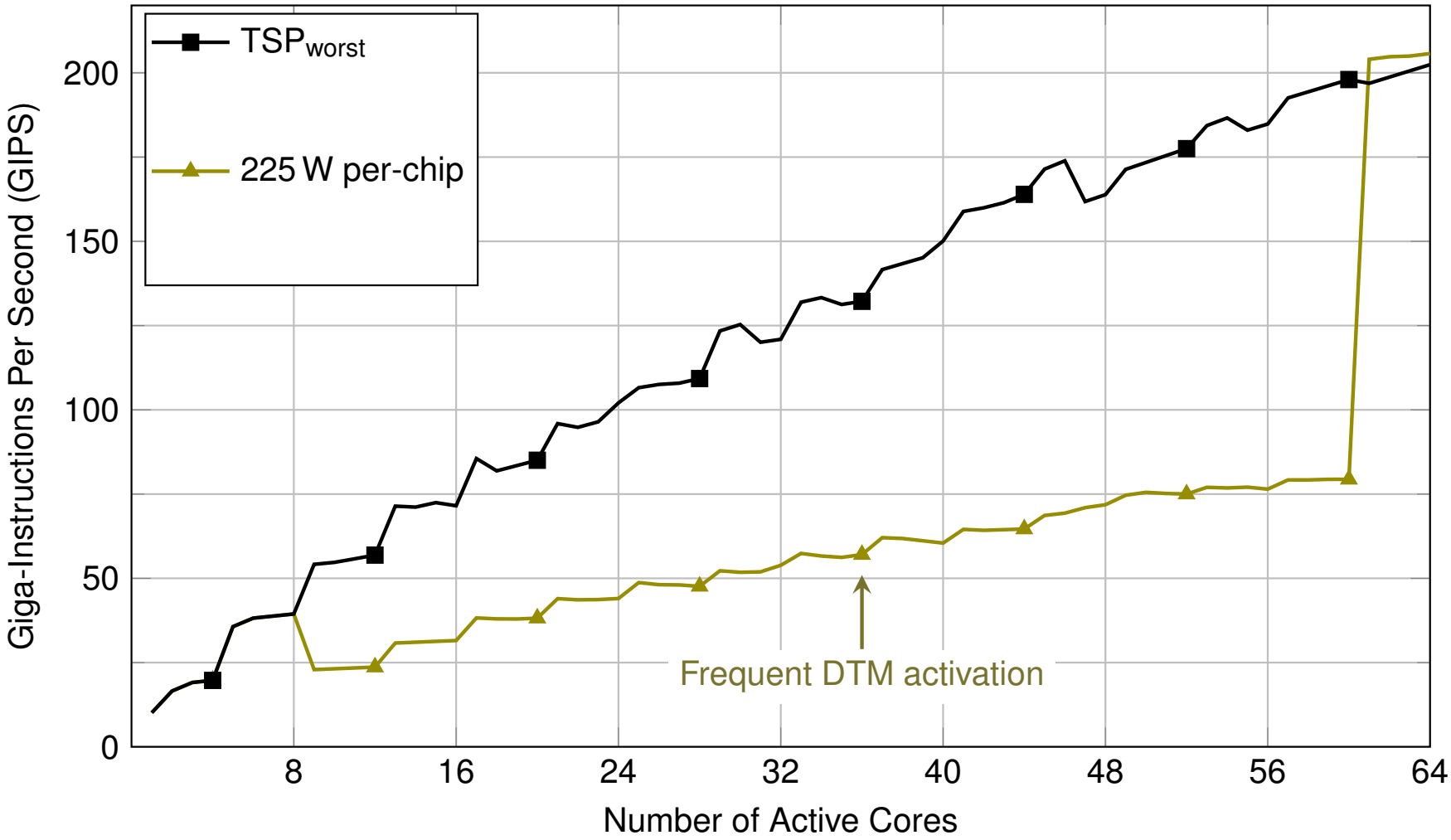

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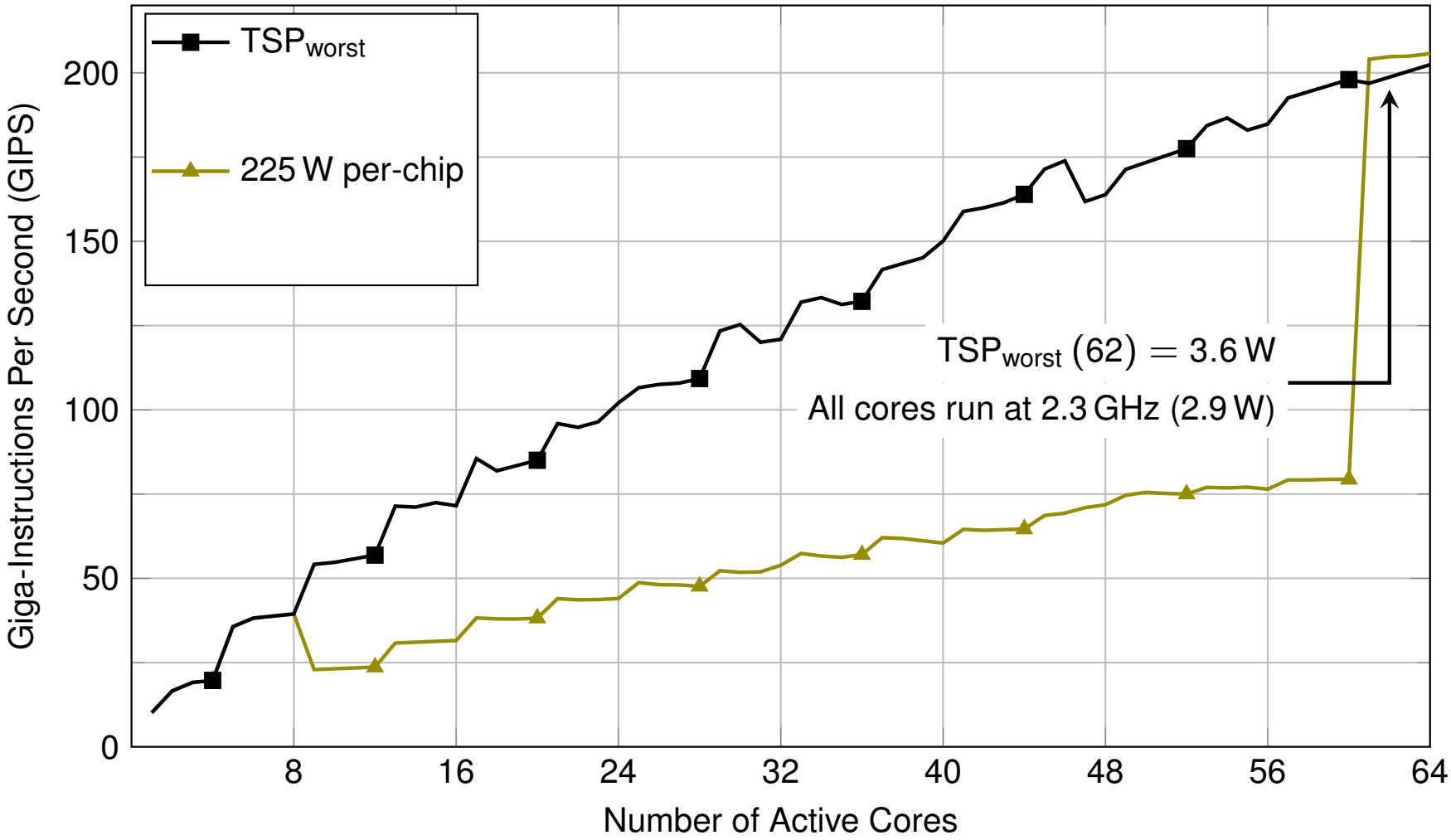

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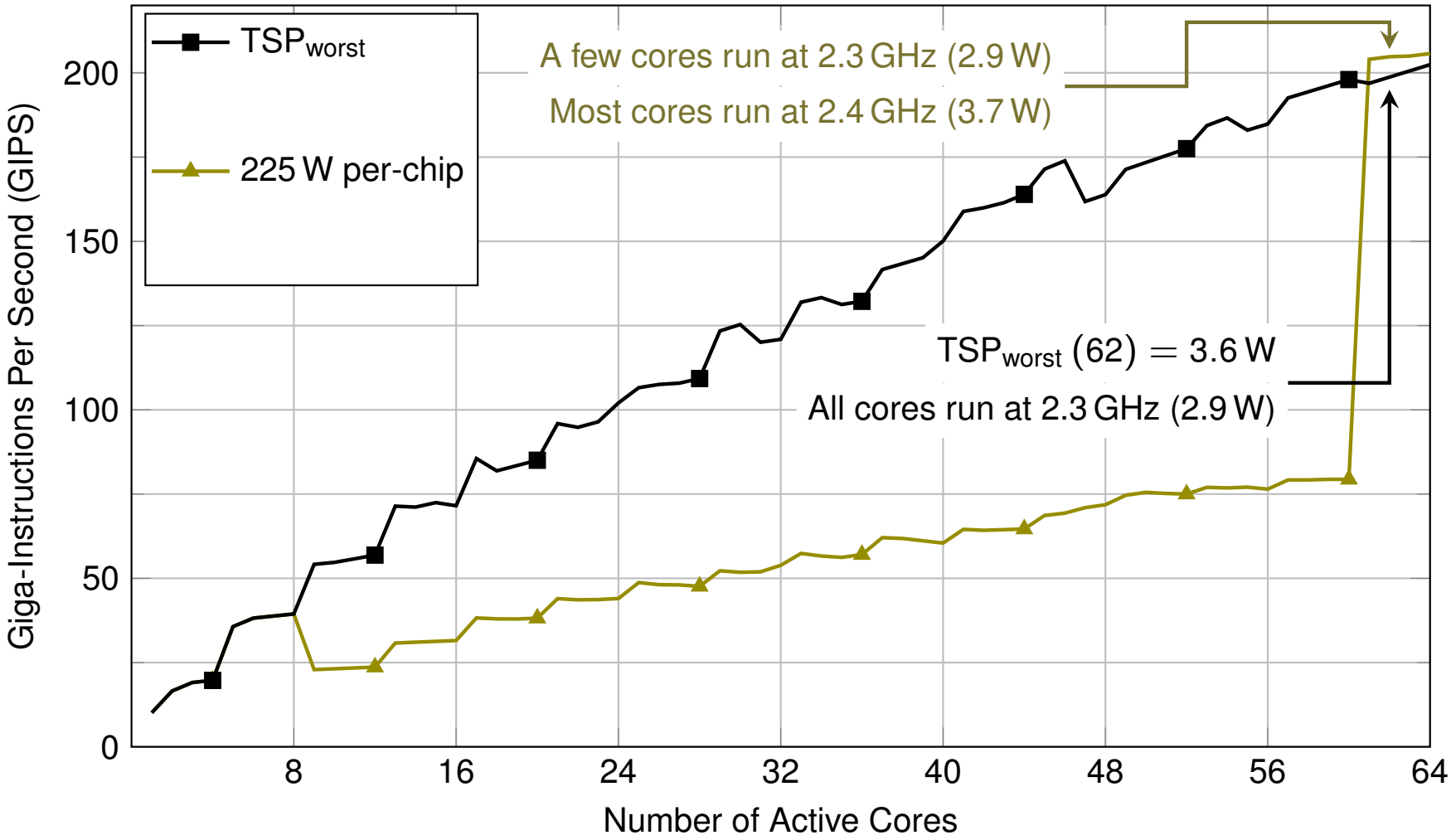

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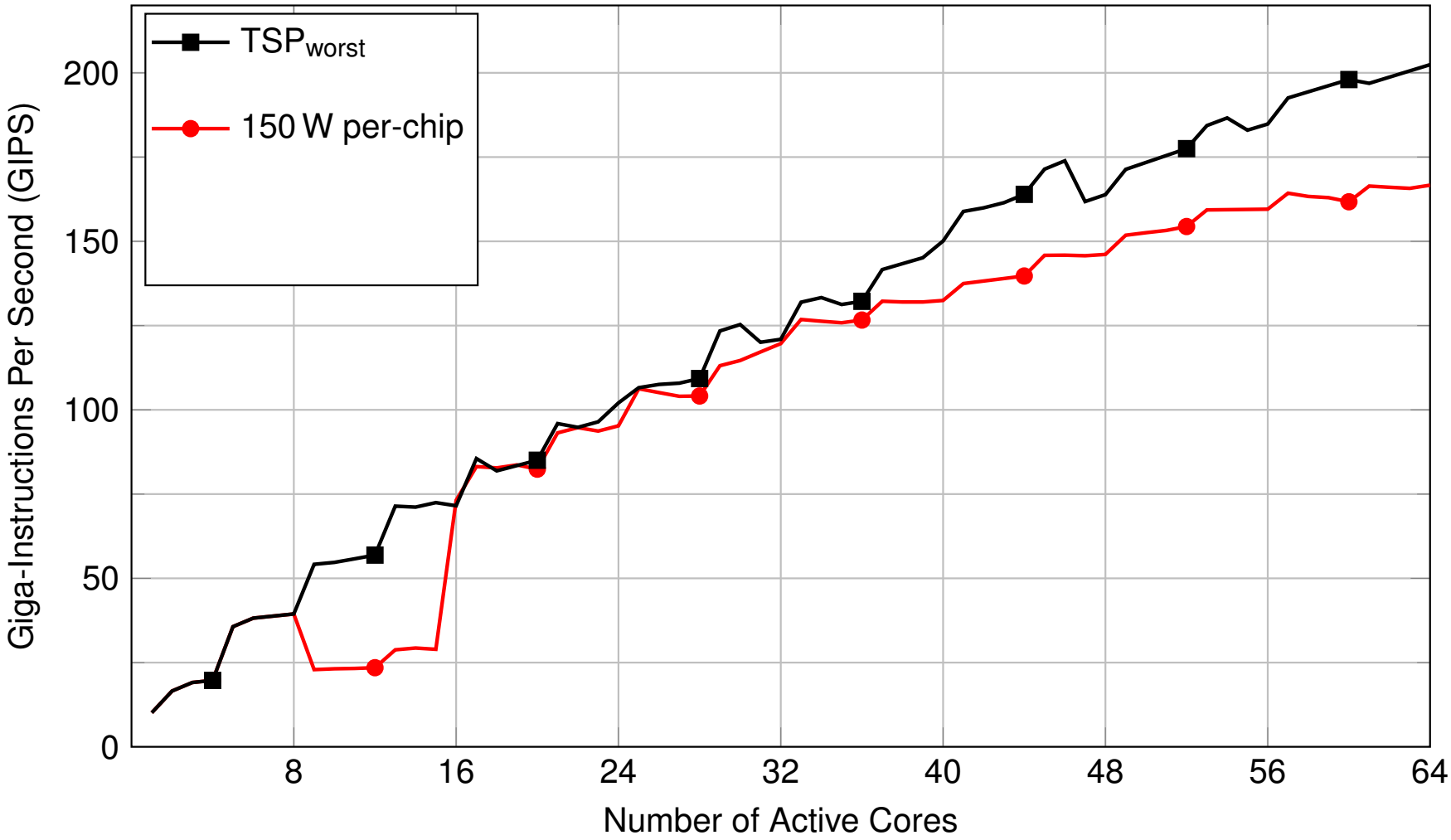

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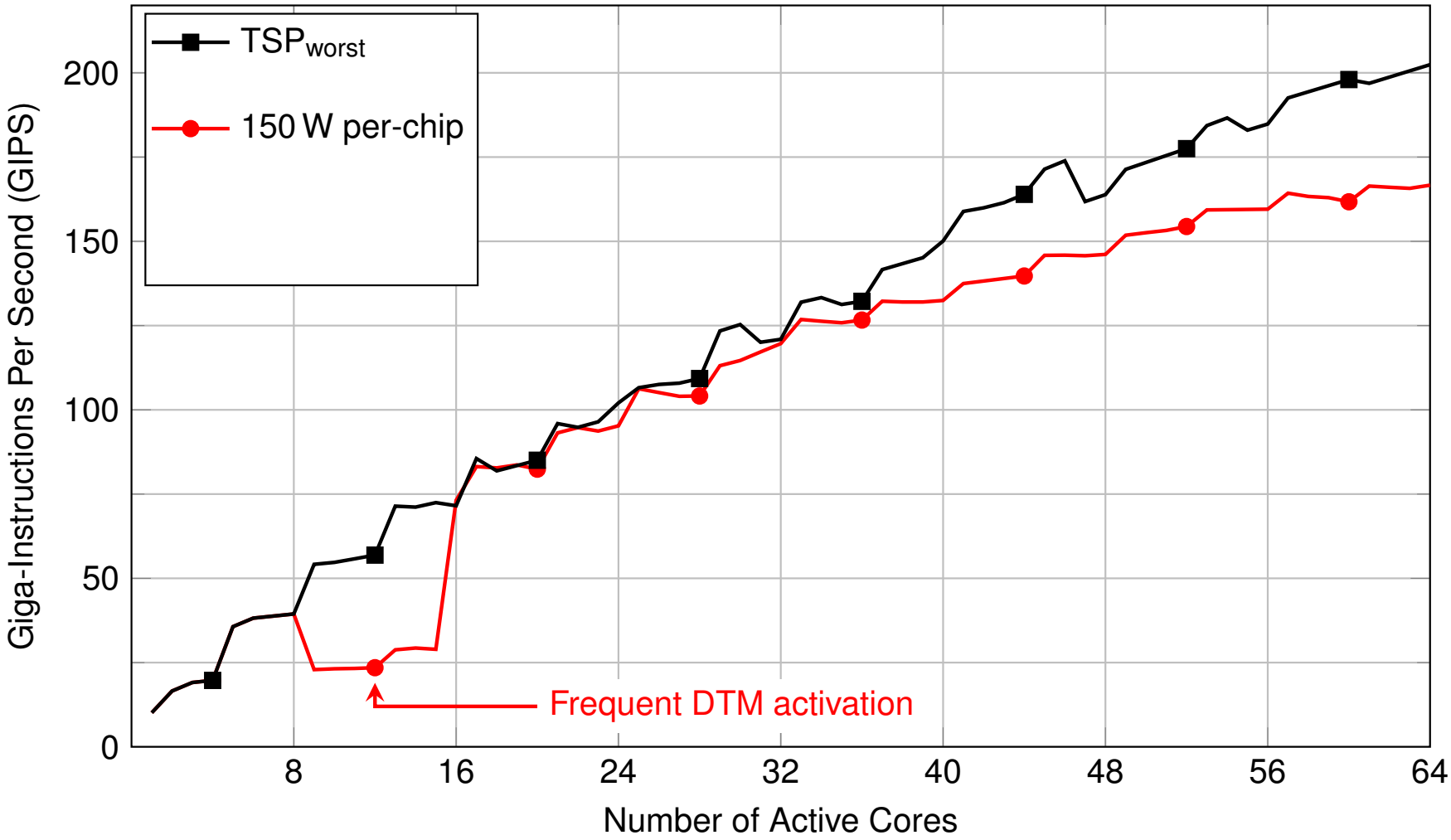

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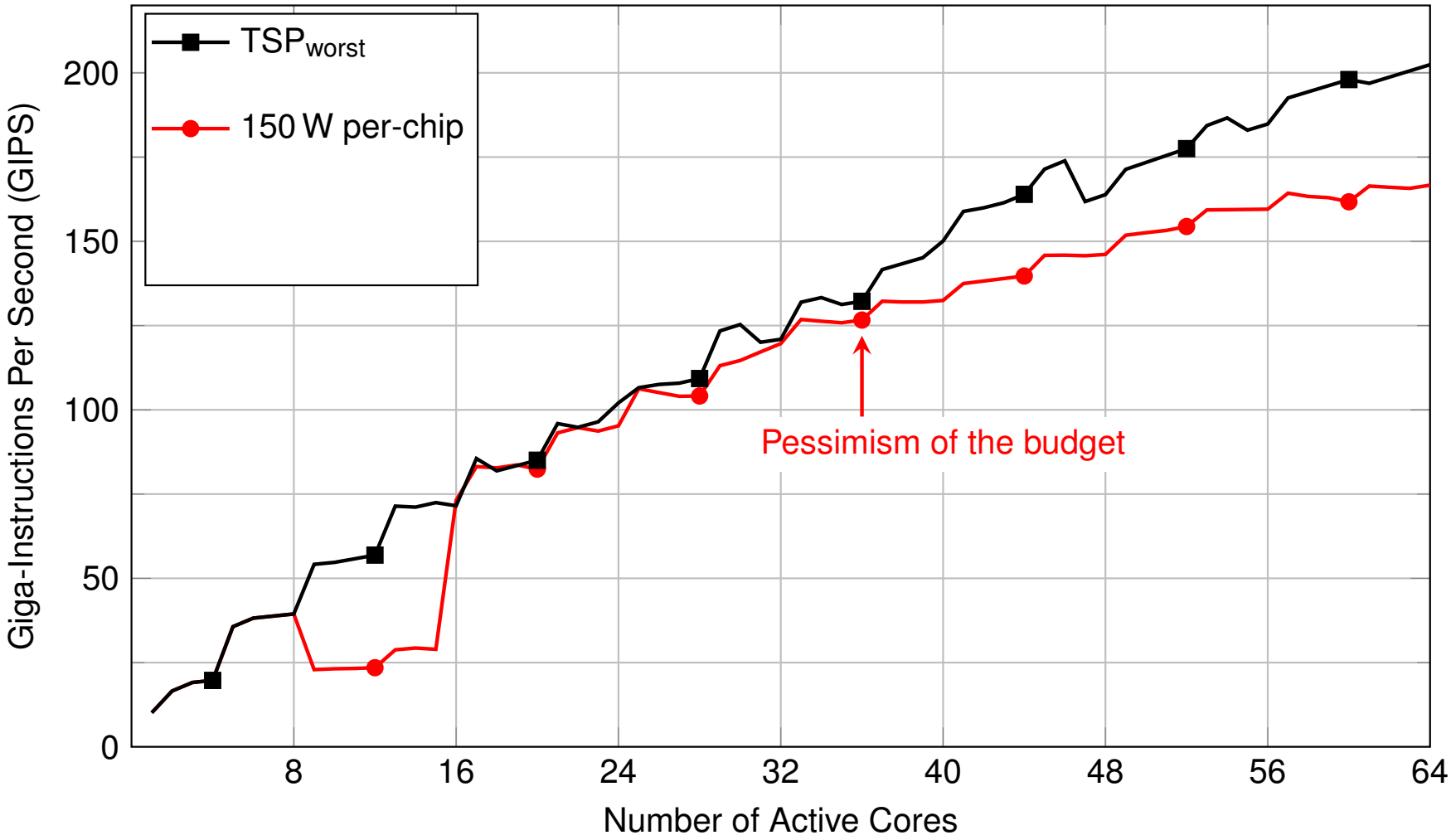

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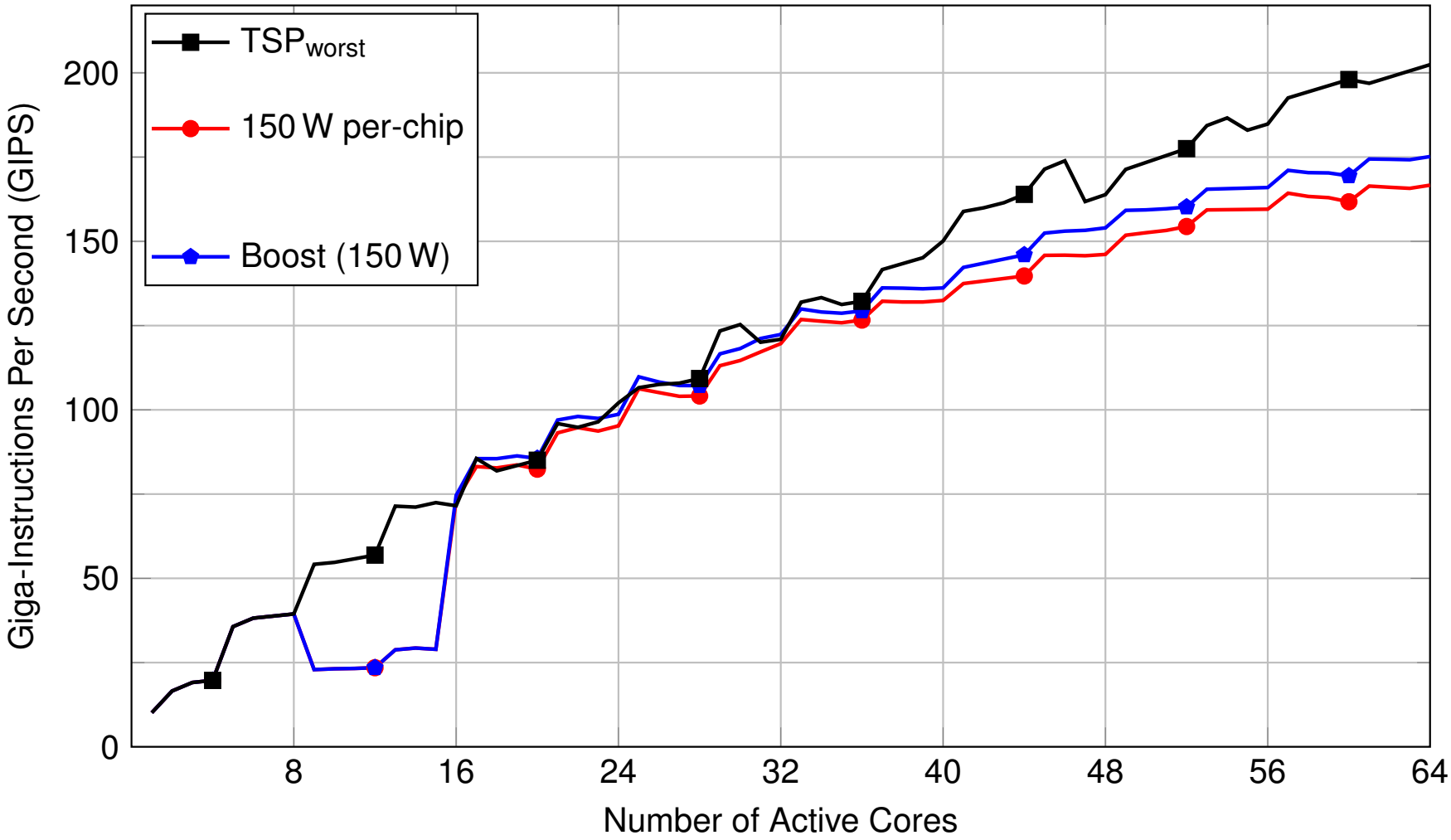

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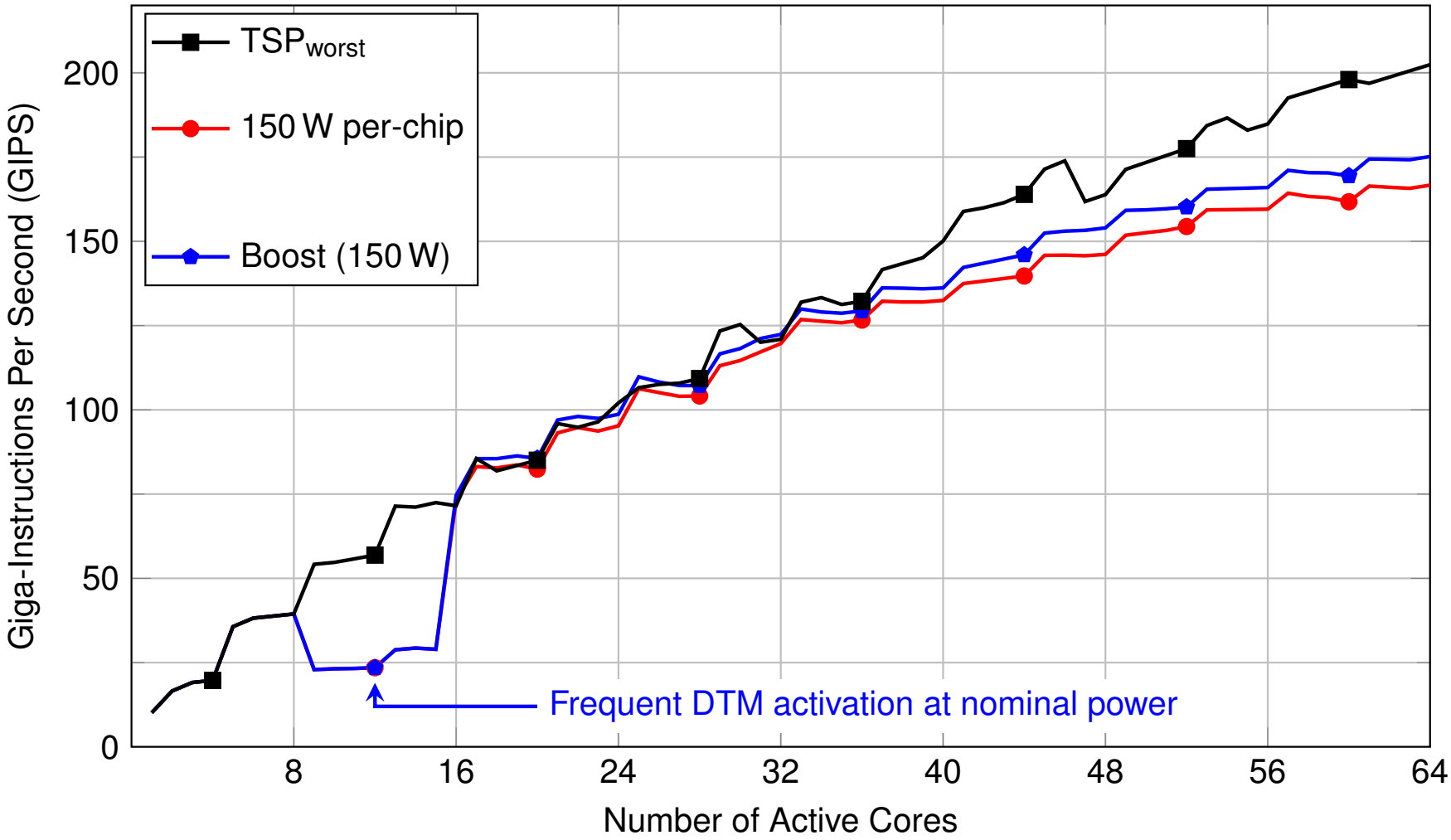

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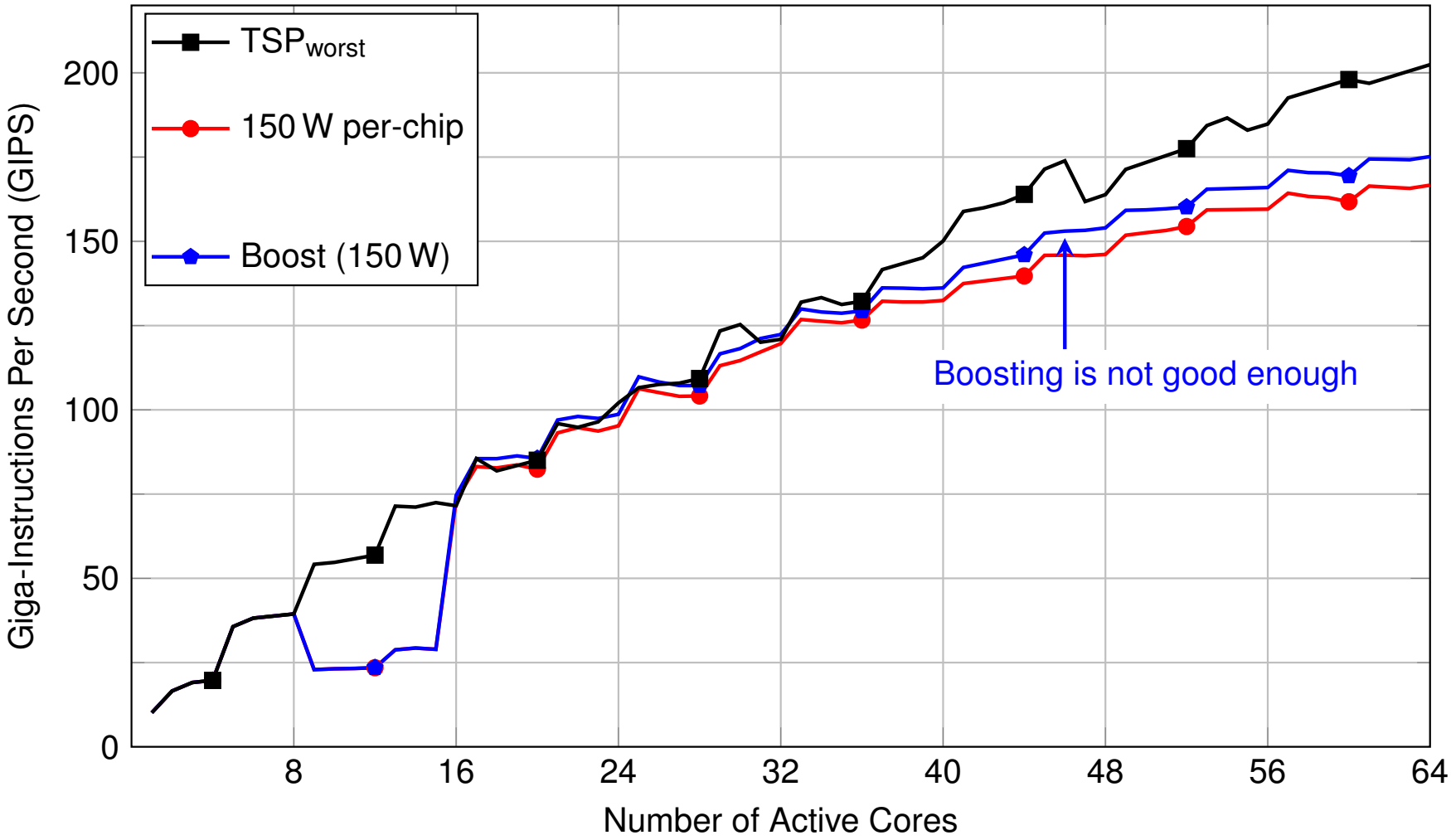

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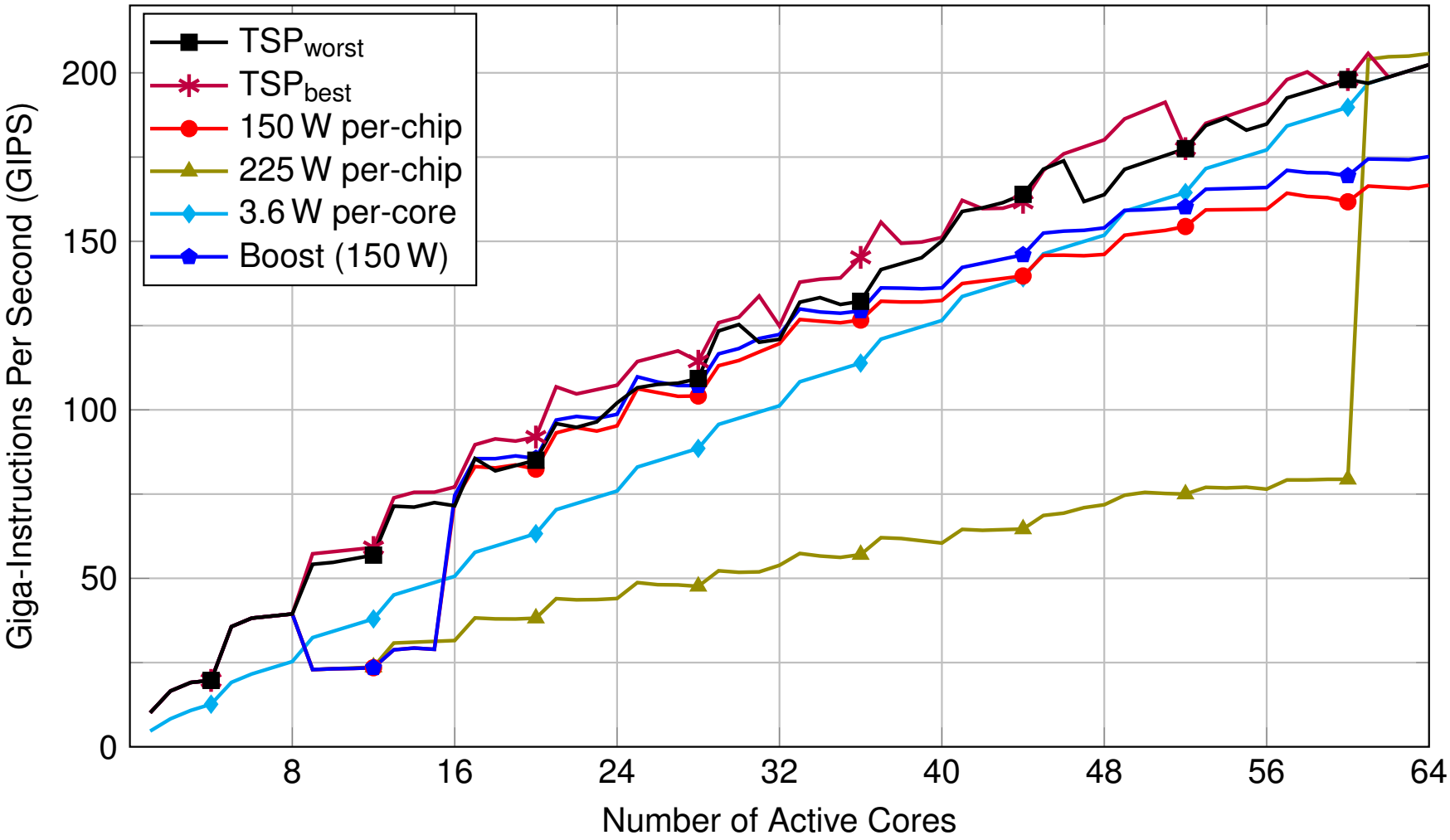

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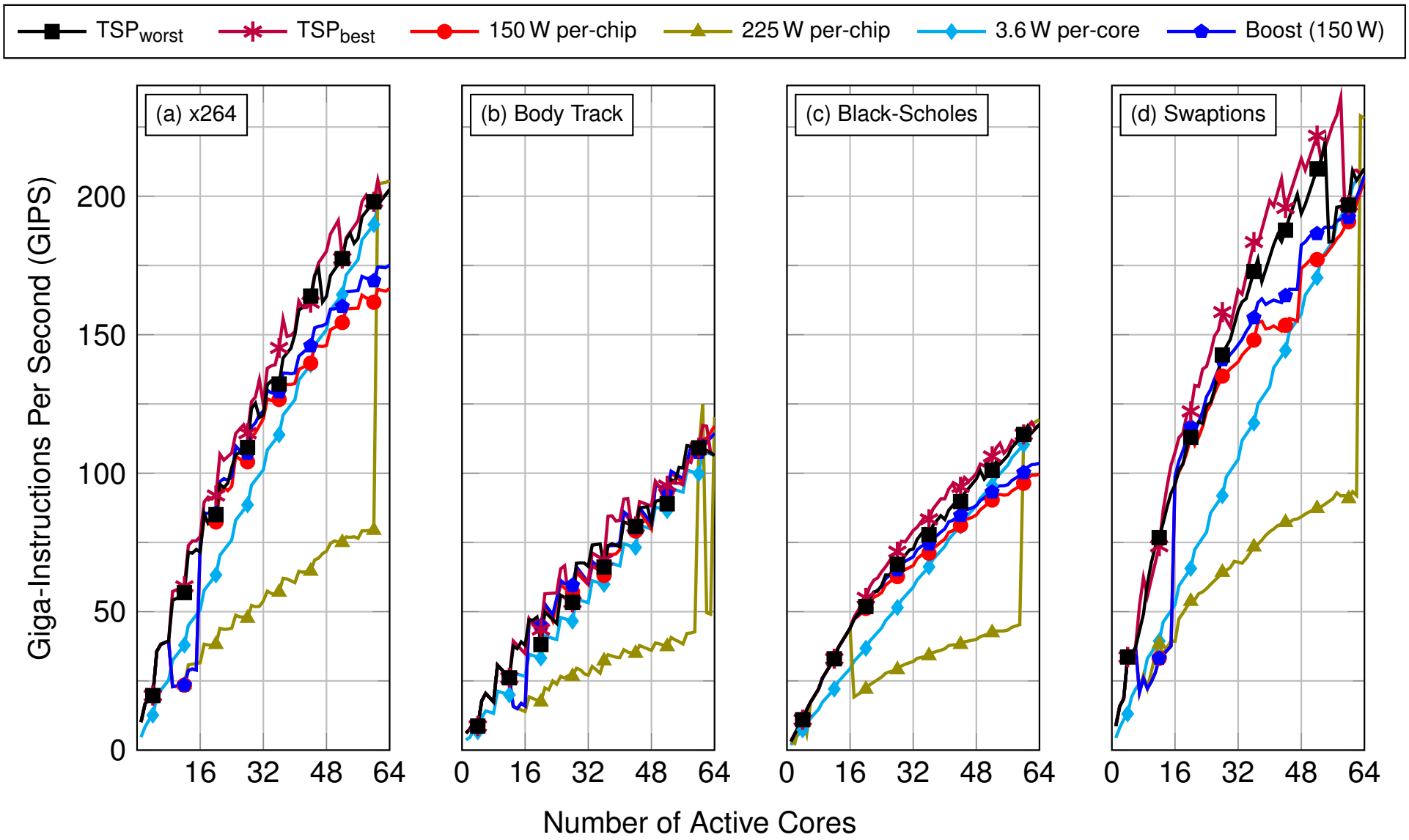

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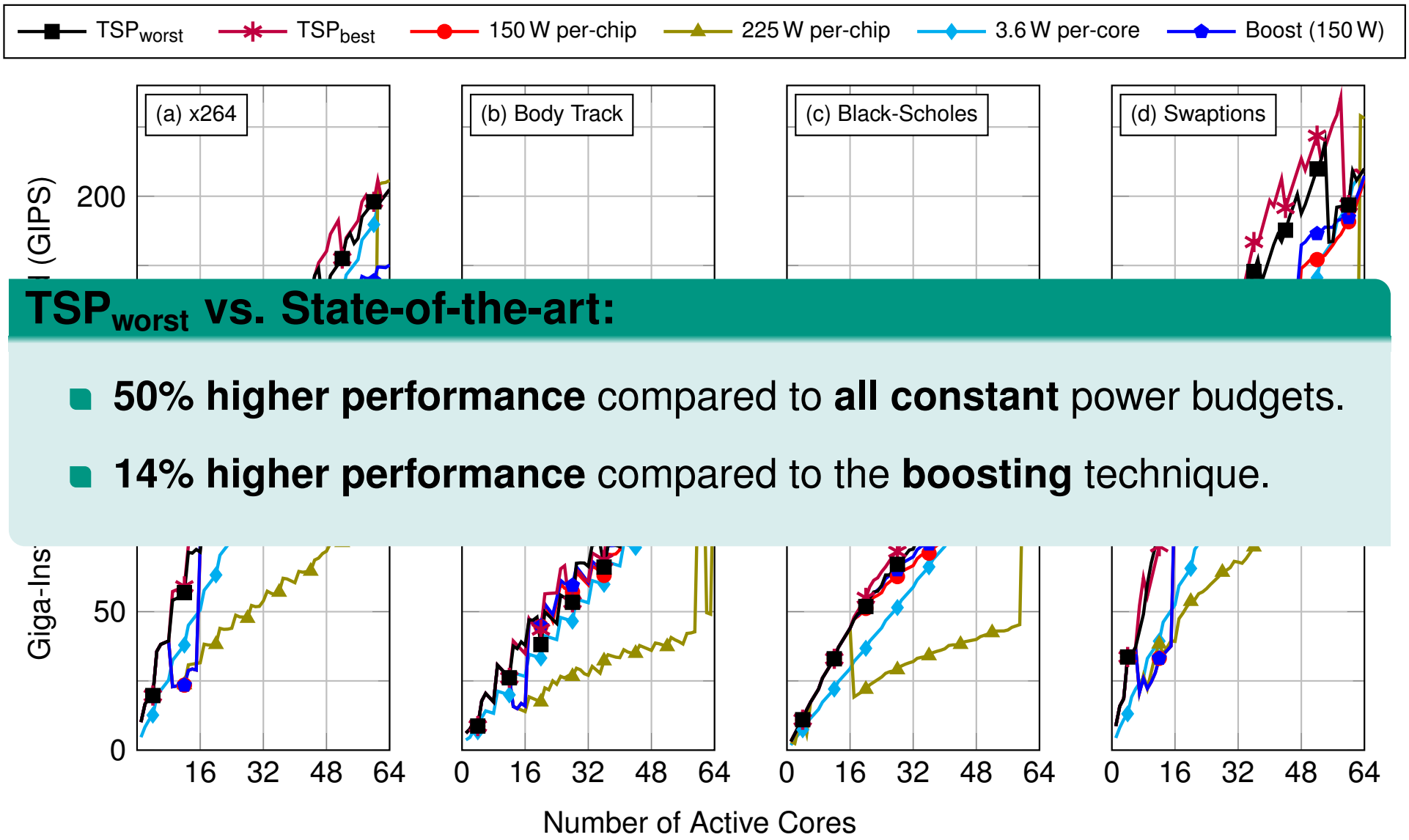

TSP_{worst} vs. State-of-the-art:

- **50% higher performance** compared to **all constant** power budgets.
- **14% higher performance** compared to the **boosting** technique.

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Conclusions

- *Single* and *constant* power budgets:
  - Thermally unsafe.
  - Pessimistic.
- *Boosting* techniques:
  - Do not solve the problem.
- Thermal Safe Power (TSP) $\rightarrow$ **Safe** and **efficient** power budget:
  - Given mappings $\rightarrow$ Online.
  - Worst-case TSP $\rightarrow$ Abstracts from mapping decisions.
- TSP $\rightarrow$ Fundamental new step in dark silicon:
  - Alleviates pessimistic estimations of TDP $\rightarrow$ **Less dark silicon**.
  - Enables **new performance improvements** compared to State-of-the-art.

Conclusions

- *Single* and *constant* power budgets:
  - Thermally unsafe.
  - Pessimistic.
- *Boosting* techniques:
  - Do not solve the problem.
- Thermal Safe Power (TSP) $\rightarrow$ **Safe** and **efficient** power budget:
  - Given mappings $\rightarrow$ Online.
  - Worst-case TSP $\rightarrow$ Abstracts from mapping decisions.
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Thank you!

Questions?

TSP source-code:

http://ces.itec.kit.edu/download

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Appendix

- Voltage/Frequency Settings
- Different Power Constraints per Core
- Best-Case Mapping for Uniform TSP
- Transient State Considerations

Appendix: Voltage/Frequency Settings

Frequency [GHz]	Voltage [V]
0.1	0.61
0.2	0.61
0.3	0.613
0.4	0.615
0.5	0.616
0.6	0.618
0.7	0.63
0.8	0.64
0.9	0.66
1.0	0.67
1.1	0.69
1.2	0.70
1.3	0.72
1.4	0.74
1.5	0.76
1.6	0.77
1.7	0.80
1.8	0.81
1.9	0.84
2.0	0.86

Frequency [GHz]	Voltage [V]
2.1	0.88
2.2	0.91
2.3	0.93
2.4	0.96
2.5	0.98
2.6	1.01
2.7	1.04
2.8	1.07
2.9	1.11
3.0	1.13
3.1	1.16
3.2	1.19
3.3	1.22
3.4	1.25
3.5	1.29
3.6	1.32
3.7	1.36
3.8	1.39
3.9	1.43
4.0	1.47

Appendix

- Voltage/Frequency Settings
- Different Power Constraints per Core
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Appendix: Different per-core Budgets

- **Objective:** Maximize the total power consumption for mapping **Q**.
- The problem can be formulated as a **linear programming**:

$$\text{Maximize} \quad \sum_{i=1}^{N} p_i^{\text{cores}}$$

such that:

$$\mathbf{BT} - \mathbf{P}^{\text{cores}} = \mathbf{P}^{\text{blocks}} + T_{\text{amb}}\mathbf{G}$$

$$\sum_{i=1}^{N} p_i^{\text{cores}} \leq P_{\max} - \sum_{i=1}^{N} p_i^{\text{blocks}}$$

$$T_i \leq T_{\text{DTM}} \qquad \text{for all } i \in \mathbf{K}$$

$$T_i \geq 0 \qquad \text{for all } i = 1, 2, \ldots, N$$

$$p_i^{\text{cores}} = 0 \qquad \text{for all } i \notin \mathbf{K}'$$

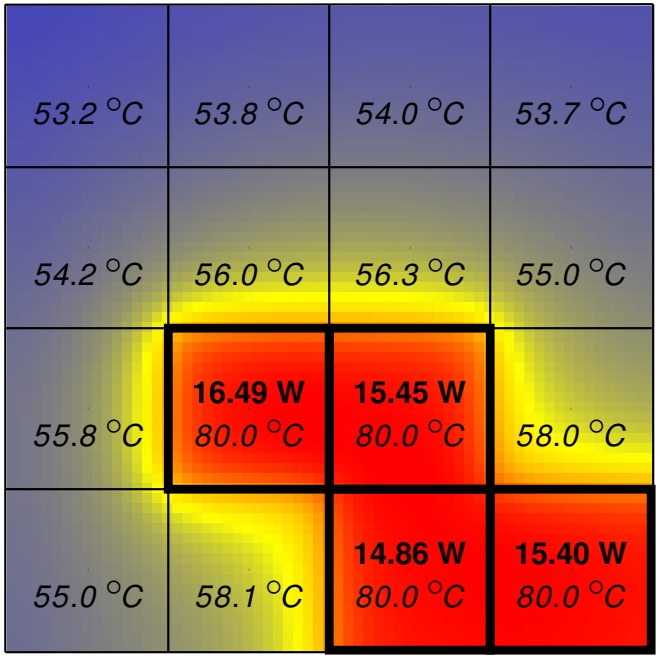
$$p_i^{\text{cores}} = P_{\text{inact}}^{\text{core}} \qquad \text{for all } i \in \mathbf{K}' \text{ and } q_i = 0$$

$$p_i^{\text{cores}} \geq P_{\text{min}}^{\text{core}} \qquad \text{for all } i \text{ in which } q_i = 1.$$

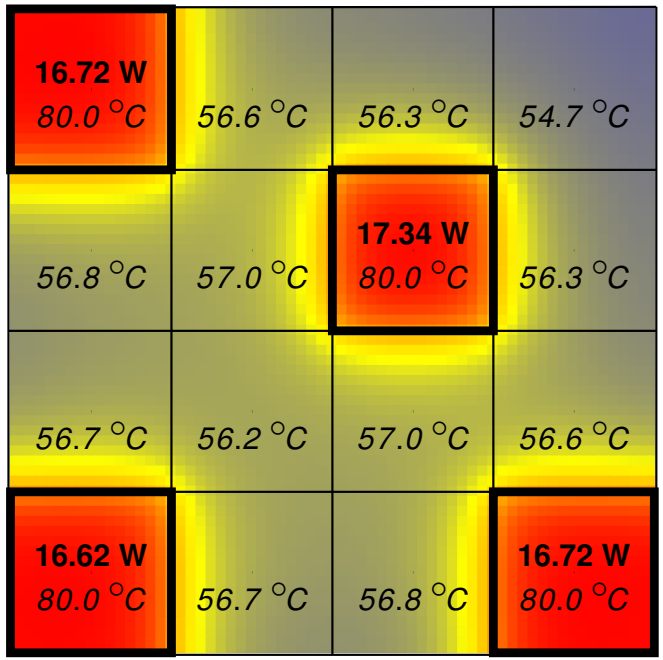
- **Result:** Vector with a different power constraint for each active core.

Appendix: Different per-core Budgets

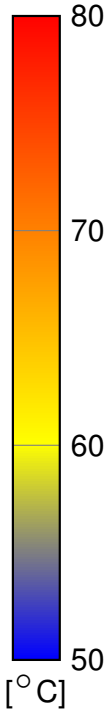
Example for 4 active cores:



(a) Total power: 62.2 Watts



(b) Total power: 67.4 Watts



Appendix

- Voltage/Frequency Settings
- Different Power Constraints per Core
- Best-Case Mapping for Uniform TSP
- Transient State Considerations

Appendix: Best-Case Mapping for TSP

- **Objective:** Find the best-case mapping for m active cores.
- The problem can be formulated as an **integer linear programming**:

$$\text{Maximize} \quad P_{\text{equal}}$$

such that:

$$T_i = P_{\text{equal}} \cdot \sum_{j=1}^{N} b^{-1}{}_{i,j} \cdot q_j + P_{\text{inact}}^{\text{core}} \cdot \sum_{\forall j \in \mathbf{K}'} b^{-1}{}_{i,j}(1-q_j) + \sum_{j=1}^{N} b^{-1}{}_{i,j} \left(p_j^{\text{blocks}} + T_{\text{amb}} \cdot g_j \right)$$

$$T_i \leq T_{\text{DTM}} \qquad \text{for all } i \in \mathbf{K}$$

$$\sum_{j=1}^{N} q_j = m$$

$$q_j = 0 \qquad \text{for all } j \notin \mathbf{K}'$$

- **Result:** Vector **Q** with the best-case mapping for m active cores.

Appendix

- Voltage/Frequency Settings
- Different Power Constraints per Core
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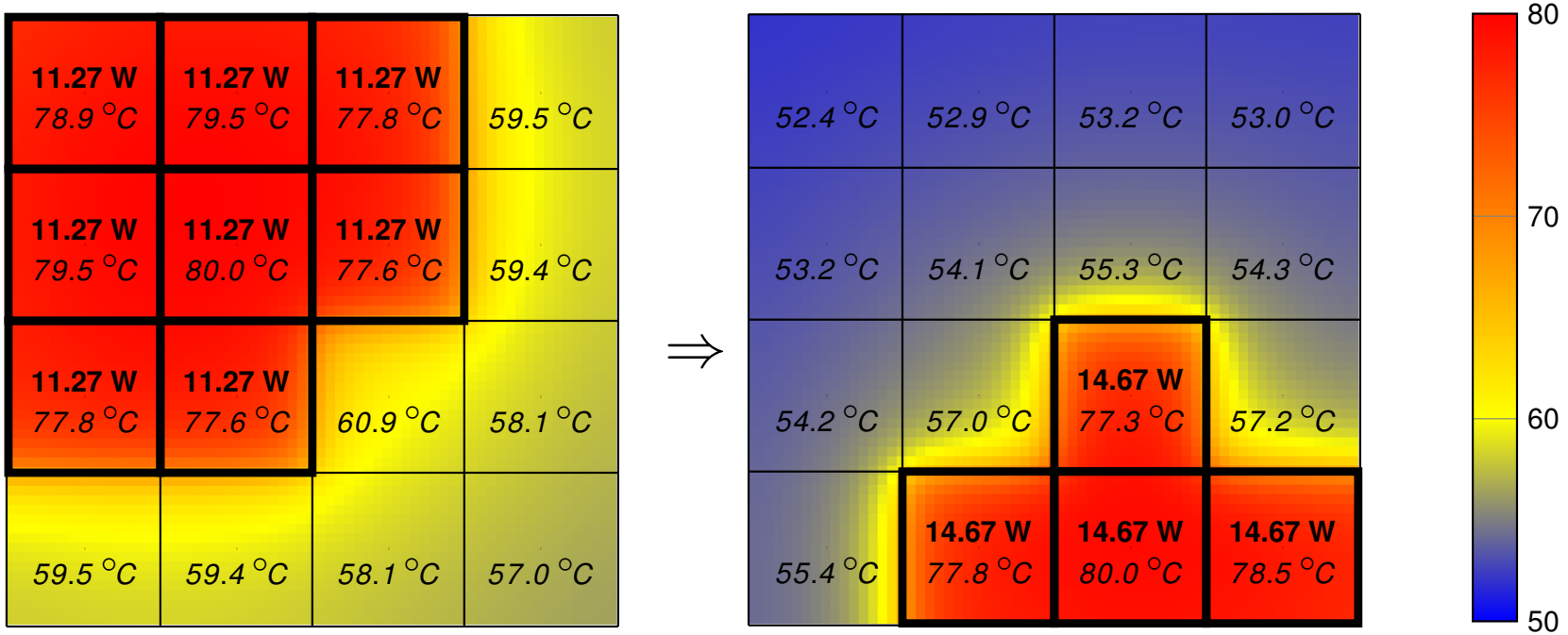
- Transient State Considerations

Appendix: Transient Considerations

- Consider a 16 chip with TDP $=$ 90 Watts.
- Consider a transition between two steady-states:

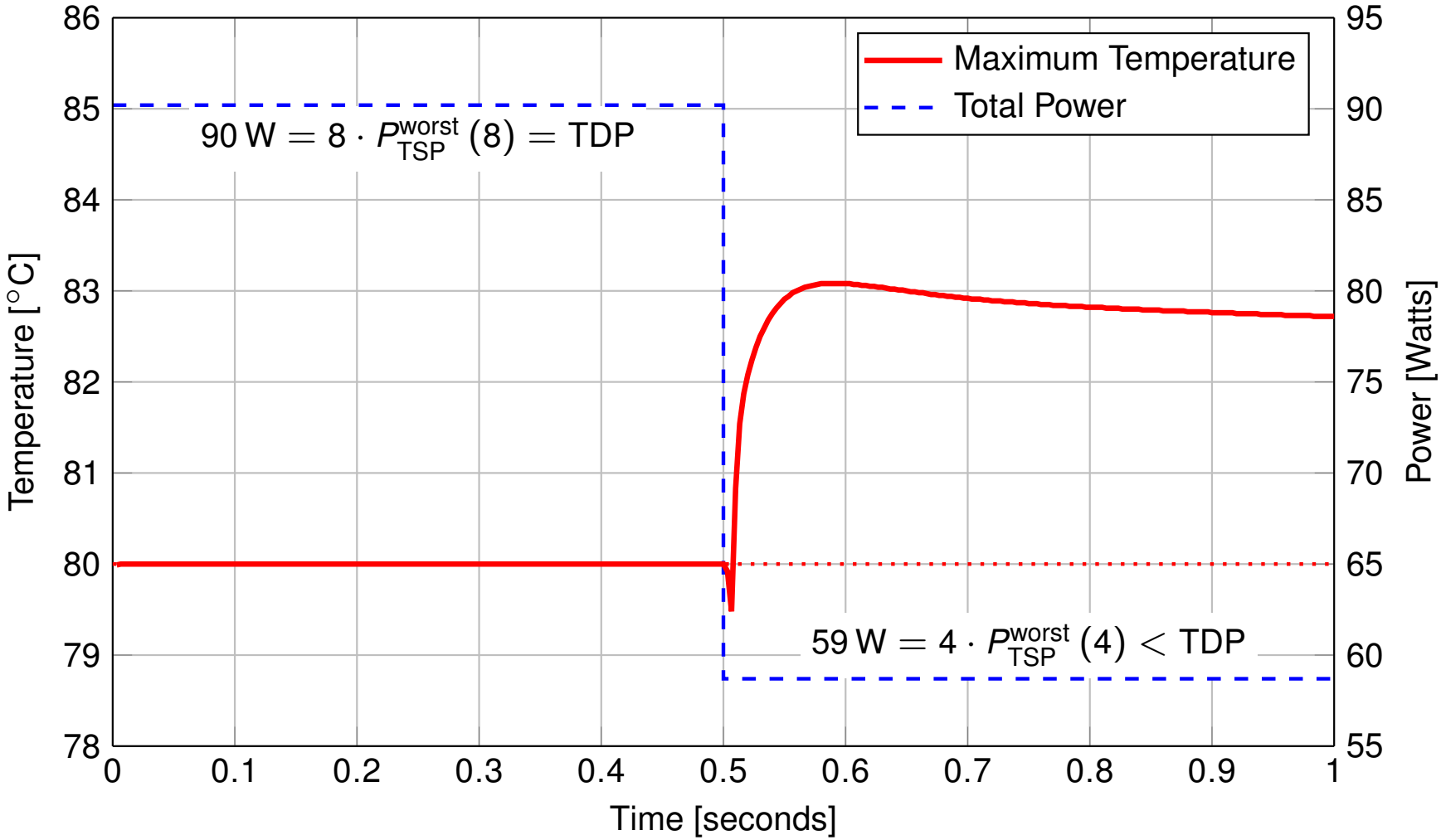


(a) 8 active cores: 90 W

(b) 4 active cores: 59 W

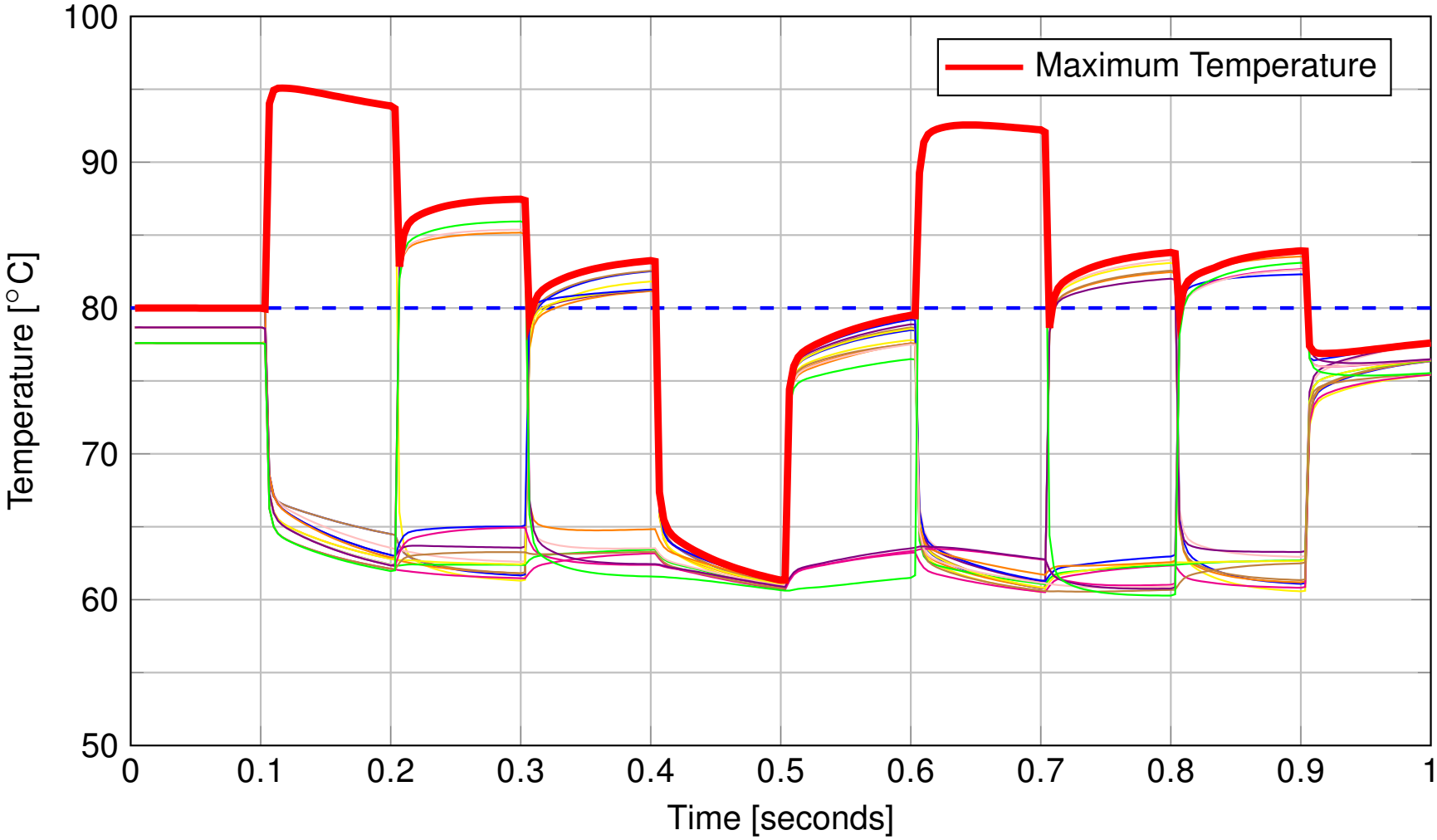
Appendix: Transient Considerations

Temperature during transition



Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 80.0°C



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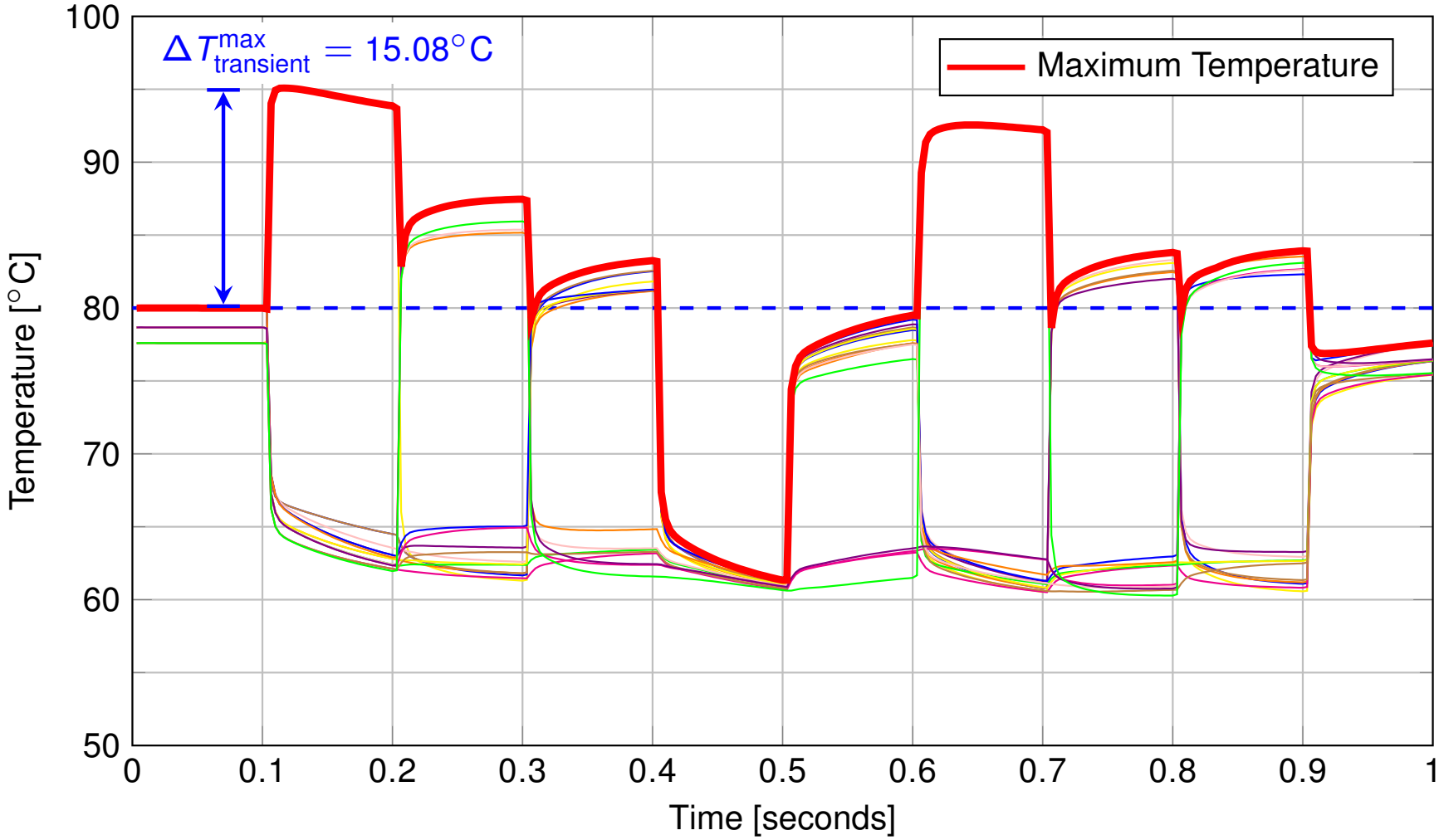
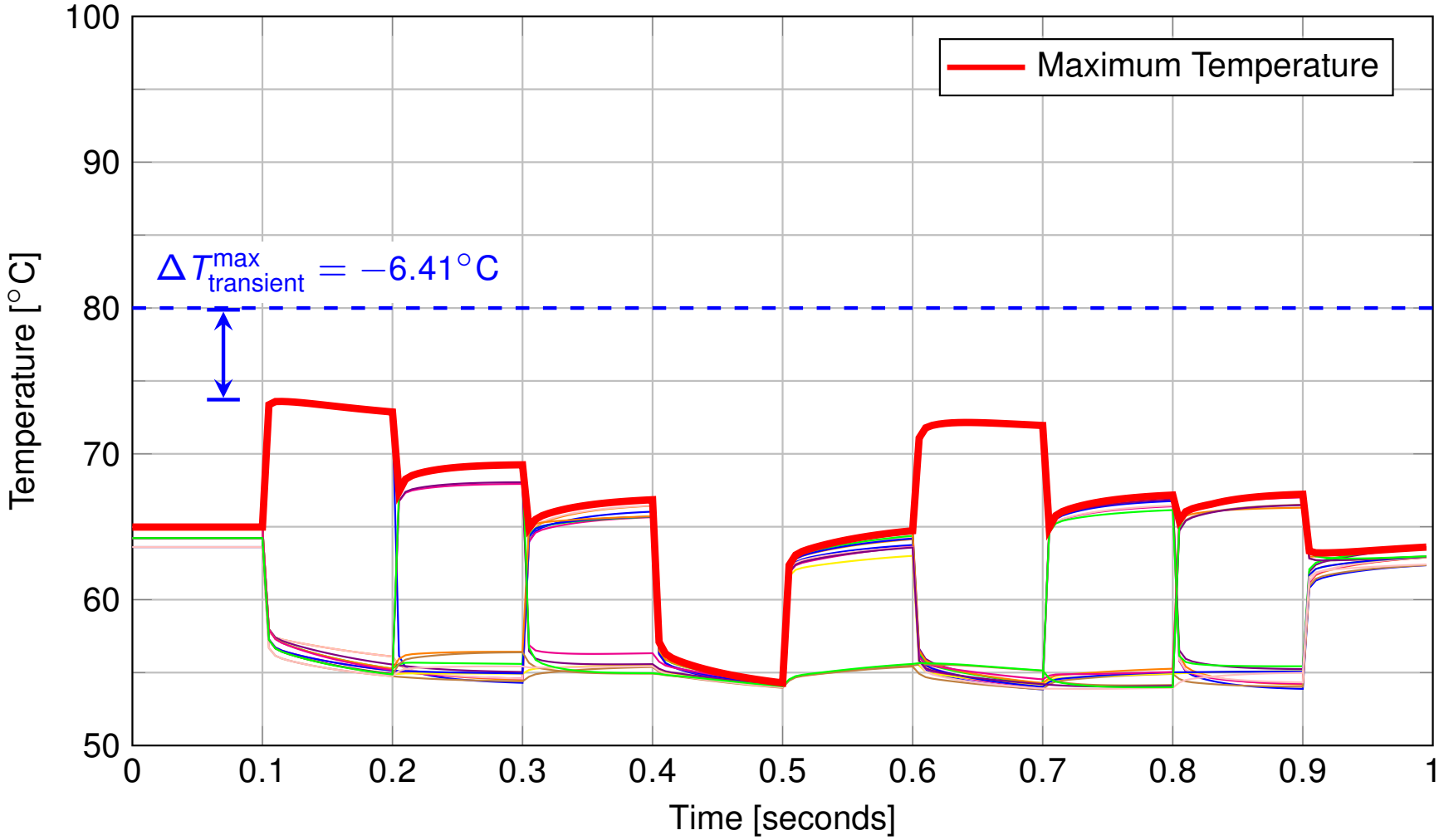


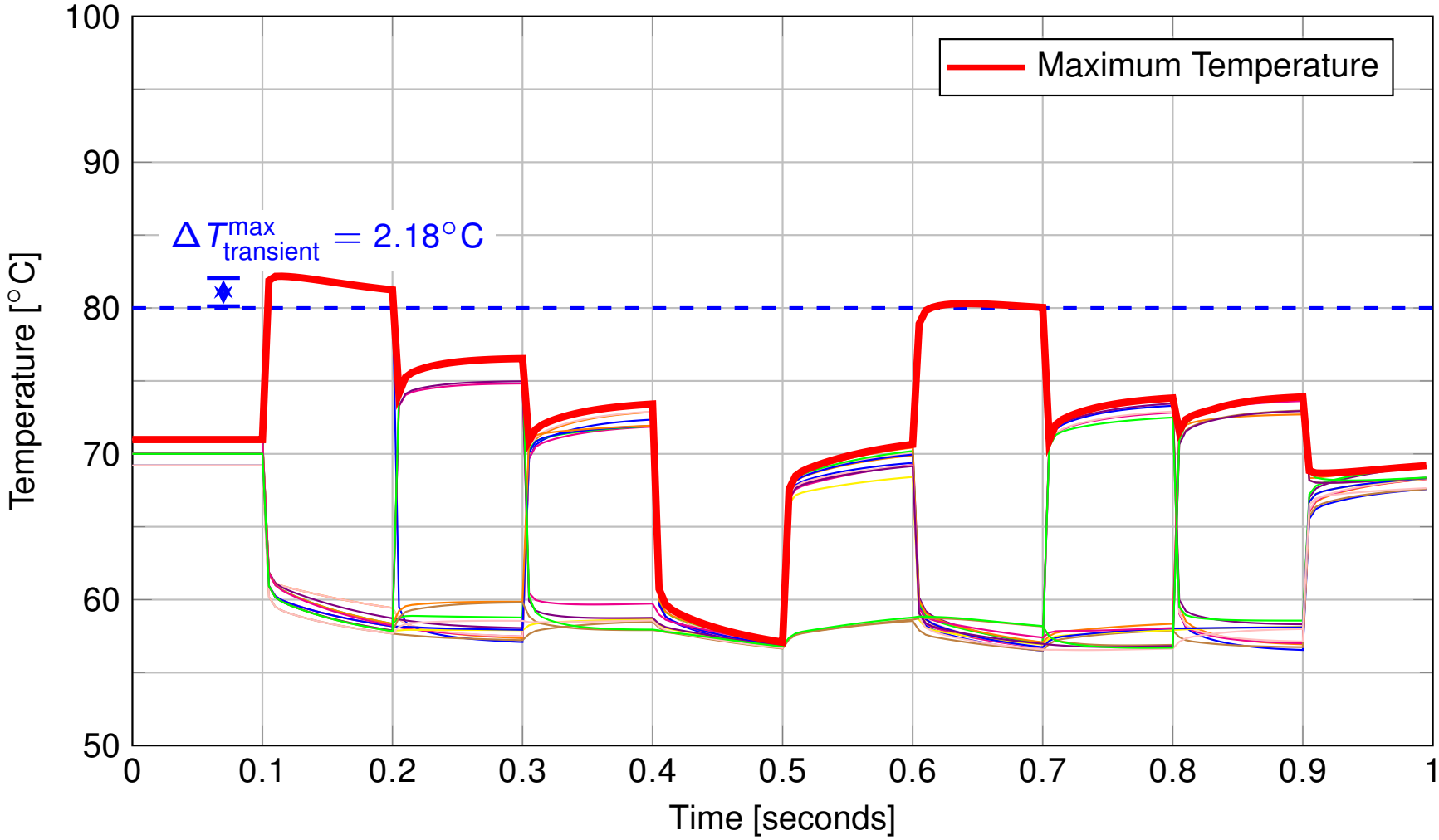
Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 65.0°C



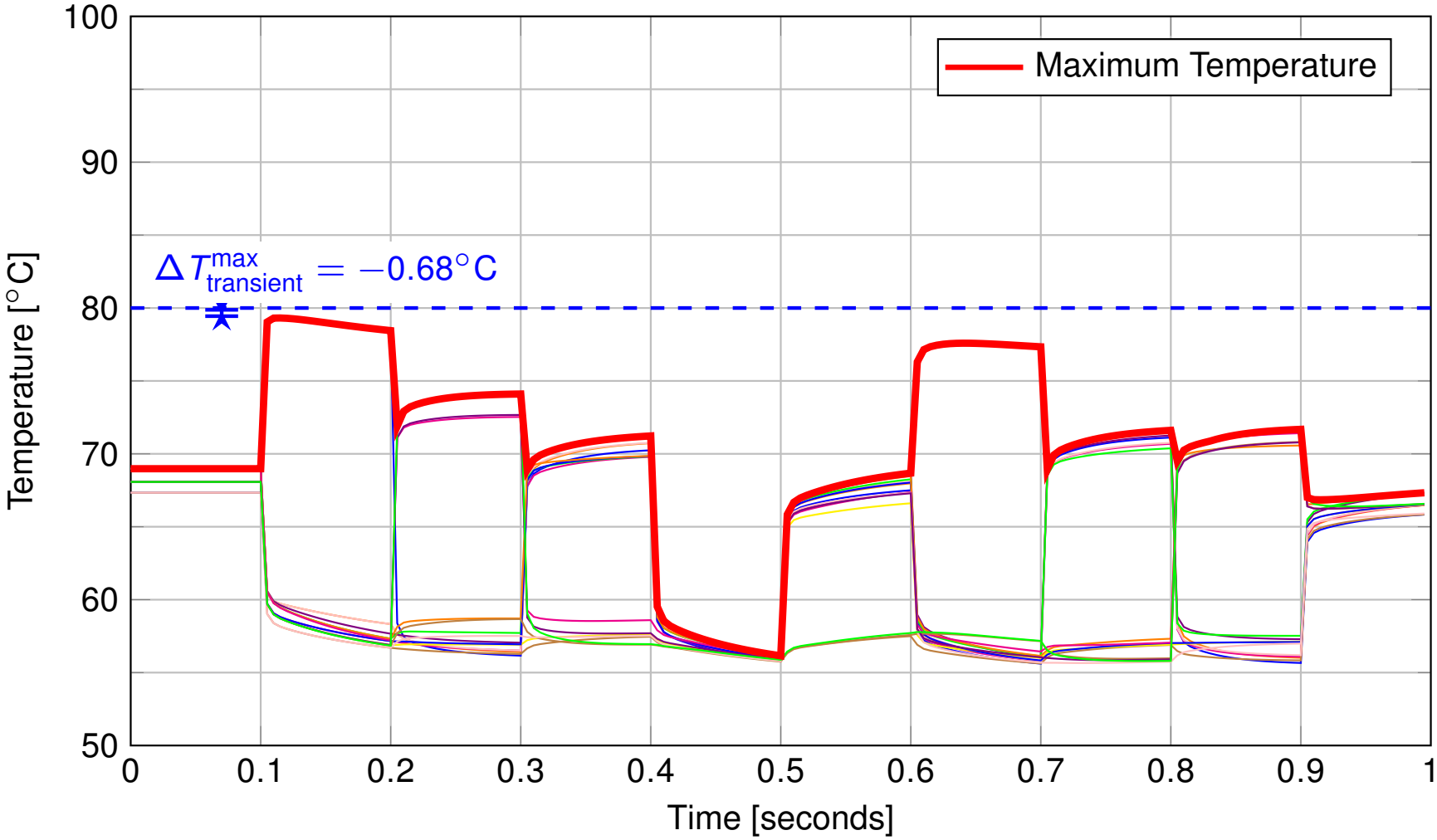
Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 71.0°C



Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 69.0°C



Appendix: Transient Considerations

Heuristic Solution Example: TSP computed for 69.5°C