# DISTINGUISHED SPEAKERS

### Wednesday Keynote I Speaker

**Gerd Teepe**
*Director Marketing for Europe, CMOS Platforms Business Unit*
*Globalfoundries*

***"FDSOI and FINFET for SoC developments"***

In his role as Director Marketing for Europe, Gerd Teepe is responsible for leading the CMOS Platforms marketing initiatives in this region, with focus on accelerating design wins in the IoT/Industrial and Automotive segments, as well as emerging markets. Prior to this, he was leading the Design Engineering Organization of GLOBALFOUNDRIES since 2009.

Before GLOBALFOUNDRIES, Gerd was with AMD, Motorola-Semiconductors, and NEC, Japan in Leadership R&D, Design, Product Management and Marketing roles.

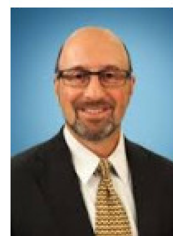
Gerd holds a Master's Degree and a PhD from Aachen University, Germany.

*Abstract:* FDSOI and FINFet use the same electrostatic principles for their transistor architectures: the conduction properties of a thin layer of undoped semiconductor material are influenced by an isolated gate. For the same layer thickness, FINFET has more drive current and higher packing densities and FDSOI, due to a buried back-gate, shows more design flexibility, can handle extremely low supply voltages and is more cost effective due to its planar structure.
While FINFet enables a continuation of Moore's Law for performance applications like Computing and Network-Switching, FDSOI shows excellent results for applications in the Internet-of-Things-domain. GLOBALFOUNDRIES has presented a dual roadmap based on FINFet and on FDSOI. On the FINFet-side it has a 14nm-technology in production and a 7nm-technology in development. Also, GLOBALFOUNDRIES has the FDSOI-based 22FDX™-Technology in production, and 12FDX™ in development.
The talk will outline the application areas for FINFet and FDSOI and give examples on how to use the back-gate bias for maximum design flexibility.

### Wednesday Keynote II Speaker

**Ron Martino**
*Vice President, i.MX Application Processor Product Line*
*S&C Business Unit, NXP Semiconductor Corporation, Austin, TX, USA*

***"Advanced Technology for Automotive Cockpits, Industrial Human-Machine-Interface and IoT Systems – Optimization of Technology – Architecture – Design"***



Ron Martino is the Vice President and General Manager of i.MX Application Processor Product Line and Advanced Technology Adoption in NXP's MICR Buisness line. He is responsible for driving the broad adoption and rapid growth of the i.MX application processor business across automotive and industrial applications. Mr. Martino is also responsible for selection and adoption of advanced technologies which differentiate the MICR teams product offerings.
Ron was the executive leader of Freescale's global microcontroller R&D organization from Feb 2008 to June 2014 developing products for multiple applications across consumer, industrial and automotive segments. Responsibilities also included non-volatile memory process technology and IP module development. In addition, Mr. Martino was responsible for Freescale's joint development partnership for automotive MCUs with ST Microelectronics. Prior responsibilities at Freescale included his role as Vice Chairman of the FSQX IC Design Company based in Tianjin China.
Ron joined Freescale in February 2008 from IBM, where he was Director of Power Architecture MPU Business. He worked at IBM for 20 years with focus on high performance computing, networking, RF communication, and gaming microelectronics. Ron also served as Director of IBM's ASIC and Core IP development organization, manager of IBM's RF product introduction organization, and manager of an advanced technology support team.

*Abstract:* Electronic innovation is becoming increasingly important in the evolution of our society. Noble goals of extending lives with improved medical capabilities, eliminating auto fatalities, and creating a connected infrastructure around the "Internet of Things" all center on electronic innovation. These goals are being driven by both legislation and consumer demand, which is leading to accelerated system challenges. New system solutions are requiring the integration of disparate functional blocks, high levels of optimization for energy efficiency and scaling across a large dynamic range of performance.
A central focus in this evolution is the enhancements to the human-machine-interface (HMI), enabling seamless interactions between humans and machines. Multimedia applications processors are playing a critical role in introducing solutions with multisensory capabilities such as natural language recognition, vision detection and augmentation of reality through enhanced display functionality.
We will explore HMI trends in multiple applications and discuss how FD-SOI technology, novel applications processor architectures, integrated circuit module development and system-on-chip integration create safe and secure systems.

### Thursday Keynote I Speaker

**Jörg Henkel**
*Chair for Embedded Systems CES*
*Karlsruhe Institute of Technology (KIT), Germany*

***"The triangle of Power Density, Circuit Degradation and Reliability"***

Jörg Henkel (M'95-SM'01-F'15) received the master's and PhD (Summa cum laude) degrees from the Technical University of Braunschweig, Germany. He is with the Karlsruhe Institute of Technology (KIT), Germany. Before he worked at the NEC Laboratories, Princeton, NJ. His current research interests include design and architectures for embedded systems with focus on low power and reliability. He has received various research awards, among them the 2008 DATE Best Paper Award, the 2009 IEEE/ACM William J. Mc Calla ICCAD Best Paper Award, the CODES+ISSS 2011, 2014 and 2015 Best Paper Awards. He was the general chair of major CAD events incl. ICCAD and ESWeek. He is the chairman of the IEEE Computer Society, Germany Section, and was the editor-in-chief of the ACM Transactions on Embedded Computing Systems for two terms. He is currently the editor-in-chief of the IEEE Design and Test Magazine. He is also an Initiator and Spokesperson of the national priority program on Dependable Embedded Systems of the German Science Foundation and the site coordinator (Karlsruhe site) of the three-university collaborative research center on invasive computing. He is a Fellow of the IEEE and holds ten US patents.

*Abstract:* Power density will stay a major challenge for the foreseeable future. Despite orders-of-magnitude-improved efficiency, power consumption per area is sharply rising, mainly due to the limits of voltage scaling. To investigate the physical implications of high power densities, we must distinguish between peak and average temperatures and temporal and spatial thermal gradients because they trigger circuit-aging mechanisms and eventually jeopardize the reliability of an on-chip system.

The talk starts by presenting some basic interdependencies in the triangle of power density, circuit degradation and reliability and continues with some solutions to mitigate the problem via, among others, power density-aware resource management and efficient power budgeting.

### Thursday Keynote II Speaker

**Josef Hausner**
*Division Vice President R&D IP Strategy,*
*Intel Mobile Communications, Germany*

***"The Path to Global Connectivity – Wireless Communication enters the Next Generation"***

Josef Hausner is responsible for the architecture evolution of Intel's cellular modems covering wireless standards ranging from GSM, 3G, LTE, Cellular IoT standards like NB-IOT, to 5G. Josef joined Intel in 2011 with the acquisition of Infineon's Wireless division where he was Vice President Concept Engineering defining cellular and connectivity products including algorithms, chip architectures, as well as complete SoCs and platforms. In 2004 Josef became a Full Professor for Integrated Systems at Ruhr-Universität-Bochum, researching on Integrated Systems and Circuits for Multi-Standard Wireless Communications, speaking and chairing sessions and symposia at conferences as well as at technical and industrial fora.

Josef holds a Dr.-Ing. Degree in the field of microwave technology from the Technische Universität in Munich. He is a member of the IEEE, VDE, and the Informationstechnische Gesellschaft (ITG), serves as curator of the Fraunhofer Heinrich Hertz Institute (HHI) and is elected board member of the ITG Germany.

*Abstract:*As mobile broadband (MBB) technologies evolve, devices need to support increasing bandwidth with multiple frequencies and dramatically exploding data rates. New air interfaces in 5G will show once again the gain in data rates as we have seen from 2G, to 3G to HSPA, to LTE and LTE advanced. These technologies in a single device provide the best possible services with great user experience to all people no matter where they are. Developing the next generation takes advantage of higher density in analog and digital silicon circuitry to enable low cost high performance solutions.
Next to those MBB systems, massive and reliable machine-type communications – also known as the Internet of Things – will get developed under the umbrella of 5G technologies. This talk will elaborate on challenges of related radio and semiconductor technologies, and highlight architectural breakthroughs to enable next generation solutions for global connectivity.

### Friday Plenary Speaker

**Norbert Wehn**
*Chair for Microelectronic System Design,*
*University of Kaiserslautern, Germany*

***"The Memory Challenge in Computing Systems: a Survey"***

Norbert Wehn holds the chair for Microelectronic System Design in the department of Electrical Engineering and Information Technology at the University of Kaiserslautern. He has more than 300 publications in various fields of microelectronic system design and holds several patents. Two start-ups spinout of his research group. In 2003 he served as program chair for DATE 2003 and as general chair for DATE 2005 respectively. In 2014 he was general Co-Chair of FPL 2015. His special research interests are VLSI-architectures for mobile communication, forward error correction techniques, low-power techniques, advanced SoC architectures, 3D integration, memory subsystems, reliability issues in SoC and hardware accelerators for financial mathematics and big data applications

*Abstract:* It is well known that DRAM memory performance cannot keep pace with the performance of today's multicore compute systems. In addition to the memory bandwidth problem, there is another major challenge, namely, the power/energy challenge. DRAMs are largely contributing to the overall power consumption. Thus, there is a need for power and bandwidth optimization of the DRAM memory subsystems. Moreover, new memory architectures are emerging like HBM, HMC and Wide I/O DRAMs to cope with the increasing bandwidth requirements. In this talk, we will give an overview on these new architectures and present various optimization techniques to optimize bandwidth and energy consumption in DRAM based memory systems.

### Banquet Speaker

*to be announced*

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