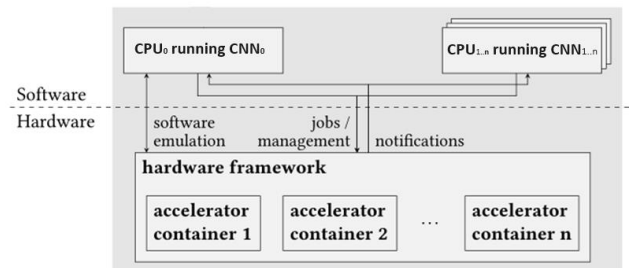# Master Thesis
Porting Reconfigurable Framework to RISC-V

The thesis aims at porting a dynamically reconfigurable framework from using embedded ARM cores on Zynq FPGA chips to a generic FPGA with RISC-V processors. With the rise of RISC-V, an open and extensible instruction set architecture (ISA), there is a growing interest in exploring its potential for high-performance, reconfigurable computing.

The existing framework on Zynq FPGA chips integrates ARM Cortex cores, providing a seamless combination of software programmability and hardware reconfigurability. This setup leverages ARM's extensive toolchain and ecosystem, ensuring efficient development and deployment of applications. The ARM cores handle the control and computational tasks while the FPGA fabric is dynamically reconfigured to accelerate specific functions, optimizing performance for a variety of workloads. This hybrid approach benefits from the powerful processing capabilities of ARM CPUs, combined with the versatility of FPGA, making it suitable for applications demanding high computational throughput and flexibility.

Transitioning to a generic FPGA with RISC-V processors involves re-architecting the framework to replace ARM cores with RISC-V equivalents. The desired final setup envisions utilizing RISC-V's open-source nature to create a customizable and scalable solution. This new configuration will support a modular approach, allowing developers to tailor the processor and system peripherals to their specific needs. Additionally, the use of a generic FPGA platform will enhance portability and reduce dependency on proprietary solutions. The combination of RISC-V processors and a reconfigurable FPGA fabric aims to deliver a high-performance, adaptable framework, driving innova-

tion in edge computing, AI acceleration, and custom hardware design. This shift promises to expand the potential applications and reduce costs, leveraging the growing ecosystem of RISC-V tools and resources.

Tasks of the Student
The tasks can include but are not limited to:
- Choosing the open source RISC-V implementation
- Creating the multi-core RISC-V Setup
- Connecting the multi-core RISC-V to the accelerator framework

Skills required/beneficial for the thesis
- Programming skills (C++, Python)
- Experience with (V)HDL or FPGA is preferred but not compulsory

Skills acquired within the thesis
- Apply your programming experience to research on real hardware
- Work in a research environment
- Experience of dynamic partial reconfiguration

Language
- The collaboration can be in English or German.

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