Multiple Bachelor & Master Theses

Topic Areas: Security, Predictability, and Performance for Run-Time Reconfigurable Processors

The i-Core is a run-time adaptive reconfigurable processor. It has containers that can be reconfigured (like in FPGAs) and that are used to load hardware accelerators at runtime, i.e. while the application is running. These accelerators are used to execute so-called Special Instructions (SIs). The SIs improve the overall execution time of the processor. Moreover, in contrast to complex out-of-order CPUs, the i-Core can provide an upper bound for the worst-case execution time. Therefore, it can be used with hard real-time requirements.

The i-Core can be further improved. In particular, we want to investigate aspects of security and predictability.

Possible Thesis Topics/Areas
- Information Leakage Protection for the i-Core
- Encryption SIs for the i-Core
- Increasing predictability of the i-Core execution
- Enhancing the performance of the implemented SIs
- Machine Learning Accelerators for the i-Core

Tasks of the student
Tasks will vary according to the thesis topic. Mainly hardware development will be performed, using our in-house i-Core prototype (based on an FPGA). However, software development is also possible. Especially when using our in-house i-Core simulator or when working on the tool side (compilation, assembly, execution-time analysis etc.).

Skills beneficial for the thesis
- Programming Skills (C, C++, Python)
- Knowledge of VHDL
- Background on Processor Architecture and/or reconfigurable computing (FPGAs)

Skills acquired with the Thesis
- Work in a research environment
- In depth knowledge of adaptive reconfigurable processors

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