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CES Chair for Embedded Systems
Prof. Dr. J. Henkel

Bachelor Thesis

Hardware Implementation of a Machine Learning Algorithm

Convolutional neural networks have achieved great success in challenging tasks such as image classification and object detection.
A convolution layer within CNNs consists of the convolution of the input feature map (IFM) with filter weights (FW) to compute the output feature map (OFM). These layers require a large amount of on-chip storage in order to store their data.
Limited on-chip storage of the embedded systems makes deployment of CNNs on embedded devices a challenging task. Because of the high data volume of the convolution layers, the data need to be shuttled between on-chip memory and off-chip memory in the form of tiles of data chunks.
The off-chip memory access volume depends on the data-reuse strategies and size of the tiles. **Data reuse strategies** mean the decisions for the order in which the IFM, FW, OFM are accessed, the **order of the computation,** and also the way for **storing** these data on the on-chip memory. Different data reuse strategies have been proposed to be used in these systems.

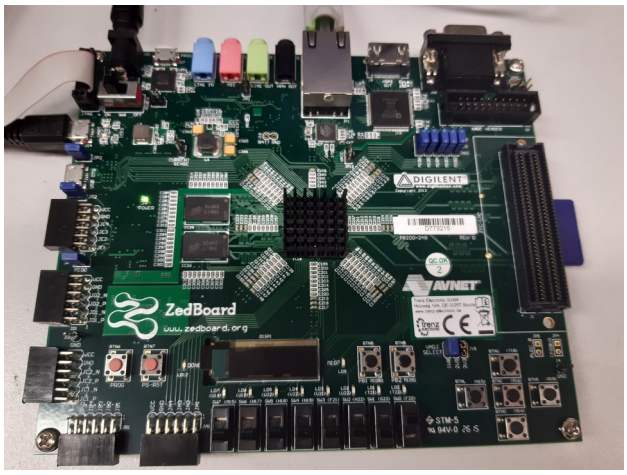
In this project, we aim to implement three of these different data reuse strategies in VHDL or Verilog on **FPGA**.

Helpful Knowledge

- Experience with FPGAs
- Knowledge of a hardware description language

Skills acquired with the thesis

- Good understanding of architecture of the convolutional neural networks
- Working with FPGAs



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